## 1.Features

- CMOS Hybrid Digital-Analog ASIC
- Independent high-input impedance operational amplifier, can match with a variety of sensors for signal processing
- Package: DIP16, SOP16
- Built-in delay timer and block timer, novel, stable and reliable structure, wide adjustment range
- Built-in reference voltage
- Operating voltage range 3.0~5.0V

## 2.Pinning Information

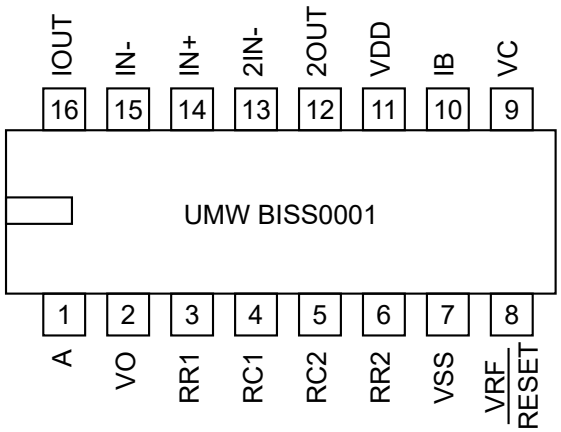



Fig.1 BISS0001 Outer Lead Connection Diagram

## 3.Absolute Maximum Ratings

| Project | Parameter | Symbol | Range | Unit |
|---|---|---|---|---|
| Voltage | Input Positive Voltage | $V_{DD}$ | 6 | V |
| | Input Negative Voltage | $-V_{DD}$ | -0.5 | V |
| Current | MaximumCurrent at Each Pin | Imax | 10 | mA |
| Temperature | Operating Temperature Range | $T_W$ | -10 to 70 | °C |
| | Storage Temperature Range | $T_C$ | -65 to 150 | °C |

## 4.Electrical characteristics ($T_A$=25°C, $V_{SS}$=0V)

| Parameter | Symbol | Conditions | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{DD}$ | | | 3 | 5 | V |
| Operating Current | $I_{DD}$ | Output | $V_{DD}$=3V | | 50 | μA |
| | | No Load | $V_{DD}$=5V | | 100 | μA |
| Input Offset Voltage | $V_{OS}$ | $V_{DD}$=5V | | | 50 | mV |
| Input Offset Current | $I_{OS}$ | $V_{DD}$=5V | | | 50 | nA |
| Open-Loop Voltage Gain | $A_{VO}$ | $V_{DD}$=5V | | 60 | | dB |
| Common Mode Rejection Ratio | CMRR | $V_{DD}$=5V | | 60 | | dB |
| Op Amp Output High Level | $V_{YH}$ | $V_{DD}$=5V | | 4.25 | | V |
| Op Amp Output Low Level | $V_{YL}$ | | | | 0.75 | V |
| Vc terminal high-level input | $V_{RH}$ | $V_{DD}$=5V | | 1.1 | | V |
| Vc terminal low-level input | $V_{RL}$ | | | | 0.9 | V |
| Vo terminal high-level output | $V_{OH}$ | $V_{DD}$=5V | | 4 | | V |
| Vo terminal low-level output | $V_{OL}$ | $V_{DD}$=5V | | | 0.4 | V |
| Terminal A input high level | $V_{AH}$ | $V_{DD}$=5V | | 3.5 | | V |
| Terminal A input low level | $V_{AL}$ | $V_{DD}$=5V | | | 1.5 | V |

## 5.Schematic Block Diagram

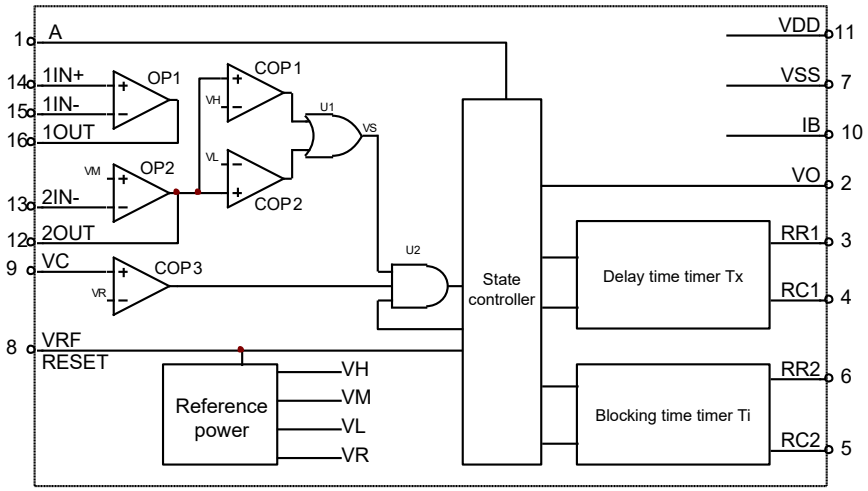



Figure 2. BISS0001 Schematic Block Diagram

Fig. 2 is a schematic block diagram of a BIS0001 infrared sensor signal processor. External components are selected by users according to their needs. As can be seen from the figure, BISS0001 is a digital-analog hybrid ASIC composed of operational amplifier, voltage comparator and state controller, delay time timer, block time timer and reference voltage source. It can be widely used in a variety of sensors and delay controllers.

The definitions and functions of each pin are as follows:

- VDD-the positive end of the working power supply. With a range of 3 ~ 5V.
- Vss-Negative end of working power supply. Generally connected to 0V.
- IB-Operational Amplifier Bias Current Setting Terminal. The RB is connected to the VSS terminal, and the RB value is about 1M.
- IIN-The inverted input of the first stage operational amplifier.
- IIN +-The in-phase input of the first stage operational amplifier.
- IOUT-Output of the first operational amplifier.
- 2IN-Inverse output of the second operational amplifier.
- 2OUT-Output of the second operational amplifier.
- Vc-Triggers the forbidden end. Prohibit triggering when Vc < VR; Allows triggering when Vc > VR. VR ≈ 0.2 VDD.
- VRF-reference voltage and reset input. Generally connected to VDD. The timer can be reset when "0" is connected.

■ A-Repeatable and non-repeatable triggering control terminals. Repeated triggers are allowed when A = "1". When A = "0", it cannot be triggered repeatedly. VO-Control signal output. It is an effective trigger when the VO is hopped from a low level to a high level by the hopping edge trigger of Vs. At the output delay Tx VO is in a low state when VO is outside and without VS up-hopping.

RR1RC1 — Adjustment pin for output delay time Tx. Tx ≈ 67025R1*C1.

RR2RC2 — Adjustment pin for trigger lockout time Ti. Ti≈60R2*C2

Let's first use the waveforms at various points in the non-repeatable trigger mode shown in Figure 3 to illustrate the operation of the BISS0001:

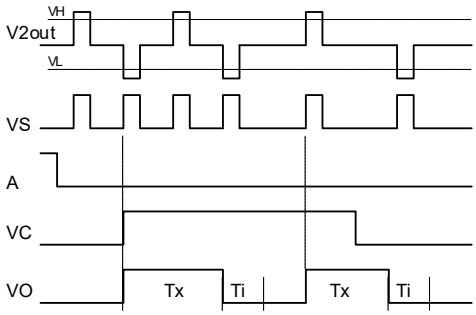



Figure 3. Waveforms at various points in non-repeatable trigger working mode

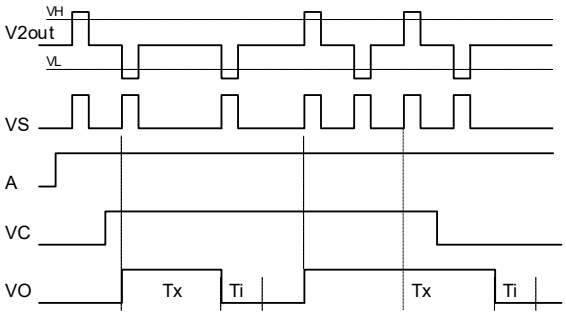



Figure 4. Waveforms at various points in repeatable trigger working mode

First of all, according to the actual needs, the user uses the operational amplifier OP1 to form a sensing signal preprocessing circuit to amplify the signal. And then Coupled to the operational amplifier OP2, and then perform the second stage of amplification. At the same time, the DC potential is raised to VM (≈ 0. 5 VDD), and then sent to the comparator COP1 The bidirectional amplitude discriminator composed of COP2 and COP2 detects the effective trigger signal VS. Since VH ≈ 0.7 VDD, VL ≈ 0.3 VDD, all, when VDD = 5V, It can effectively suppress ± 1 V noise interference and improve the reliability of the system. COP3 is a conditional comparator. Input voltage VC < VR (≈ 0. 2 VDD) When the COP3 output is high, open the AND gate U2, if there is a trigger signal VS transmitted to the lower level at this time: and when VC > VR, COP3; The output is high level, and the AND gate U2 is opened. At this time, if the jump-up edge of the trigger signal Vs comes, the delay time timer can be started. At the same time,

the output of the Vo terminal is high level, and the delay period is entered. When A terminates the "0" level, any change in V2 in the Tx time is ignored until the end of the Tx time, Vo jumps back to the low level, and at the same time starts the blockade time timer and enters the blockade period Ti. During the Ti period, no change in V2 can make Vo an effective state. The setting of this function can effectively suppress various disturbances generated during load switching.

The waveforms at various points in the retriggerable mode shown in Figure 4 illustrate the operation of the BISS0001 in this state. When Vc = "0" and A = "0", Vs cannot trigger Vo, effectively enabling it. When Vc = "1" and A = "1", Vs can trigger Vo repeatedly. is in the active state and remains active throughout the Tx cycle. During the Tx time, as long as Vs transitions upward, Vo will be extended by one Tx cycle from the moment Vs transitions upward. If Vs remains in the "1" state, Vo remains active. If Vs remains in the "0" state, Vo returns to the inactive state after the Tx cycle ends. During the block time Ti, any change in Vs cannot trigger Vo to the active state.

Through the above analysis, we have a comprehensive understanding of the circuit structure and operation of the BISS0001. It can be seen that this device has a novel structural design, powerful functions, and can be applied in a wide range of fields.

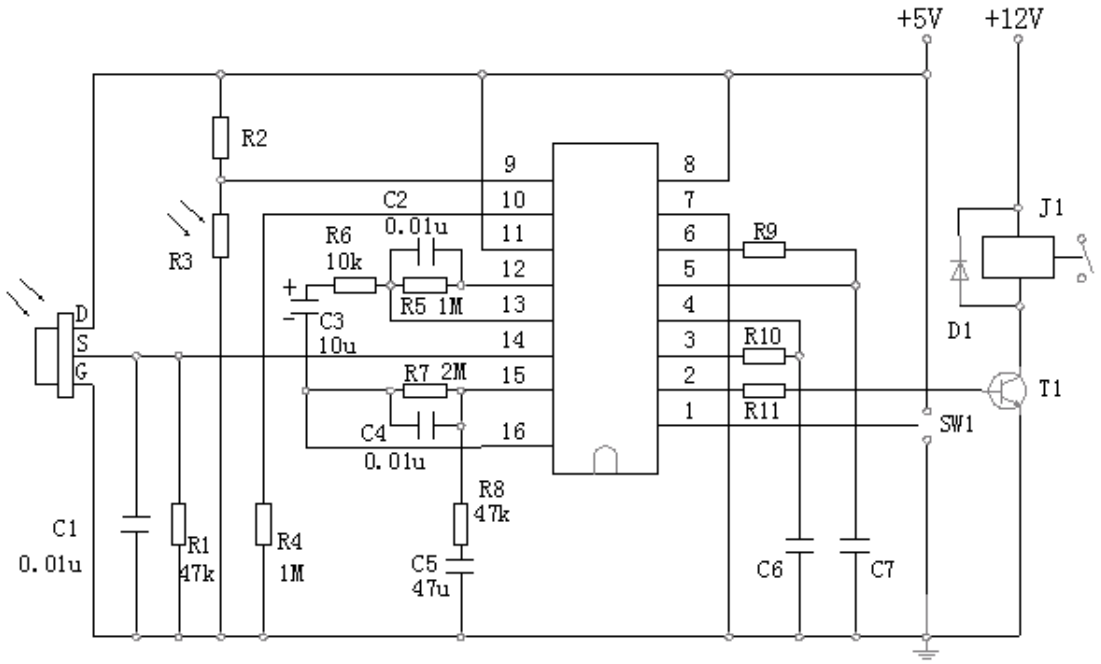



Figure 5. BISS0001 Typical Application Diagram

## 6.Application

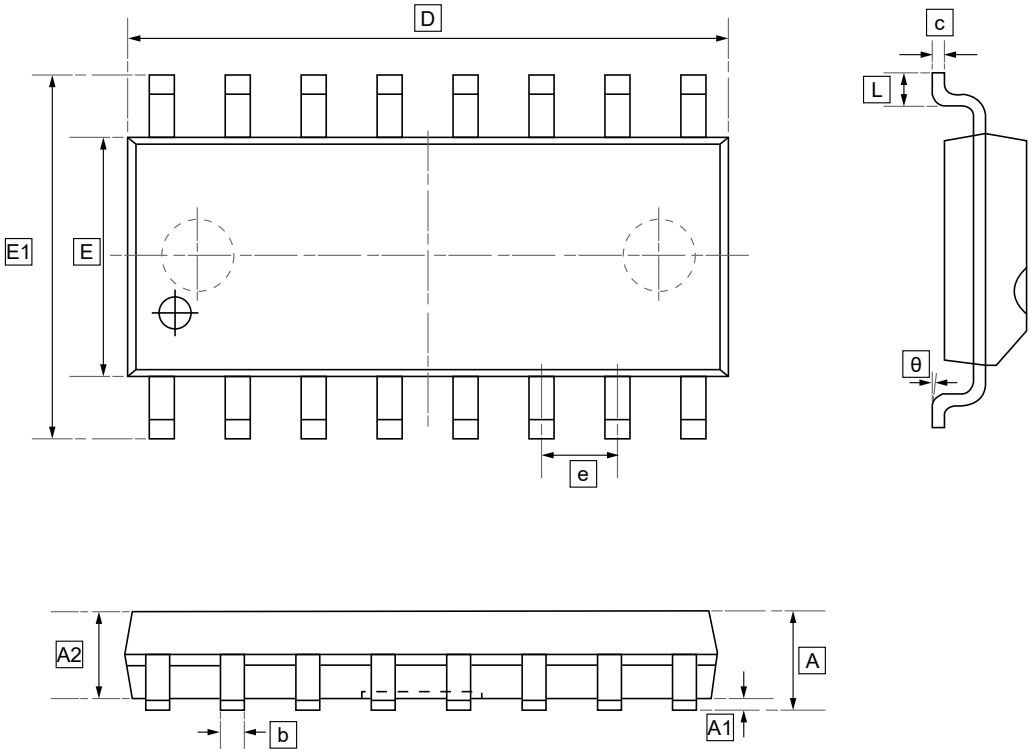
Figure 5 shows the circuit schematic diagram of BISS0001 applied to pyroelectric infrared switch

Pyroelectric infrared switch is a passive infrared switch composed of BISS0001 with pyroelectric infrared sensor and a few external components. It can automatically and quickly open all kinds of incandescent lamps, fluorescent lamps, buzzers, automatic doors, electric fans, dryers and automatic washing machines, etc. It is a high-tech product. It is especially suitable for enterprises, hotels, shopping malls, warehouses and sensitive areas such as aisles and corridors of families, or for automatic lighting, lighting and alarm systems in safe areas.

Pyroelectric infrared sensor is a new type of sensitive element, which is composed of high thermoelectric coefficient material, filter lens and impedance matching field effect transistor. It can detect infrared radiation from the human body in a non-contact manner, convert it into electrical signal output, and effectively suppress external interference radiation beyond the radiation wavelength of the human body, such as sunlight, light, and its reflected light.

In this example, the operational amplifier OP1 of BISS0001 is used as the preamplifier of the pyroelectric infrared sensor. C3 is coupled to the operational amplifier OP2 for second stage amplification. After being processed by a bidirectional amplitude discriminator composed of voltage comparators COP1 and COP2, an effective trigger signal is detected to start the delay time timer. The output signal passes through the transistor T1 and the drive relay to turn on the load. R3 is a photoresistor used to detect ambient illumination. When used as lighting control, if the environment is brighter, the resistance value of R3 will be reduced, so that the 9-pin input is at a low level and the trigger signal is blocked, saving lighting electricity. If it is applied to other aspects, it can be covered with a shade without being affected by the environment. SW1 is a working mode selection switch. When SW1 is connected with terminal 1, the infrared switch is in a repeatable triggering working mode; When SW1 is connected with terminal 2, the infrared switch is in a non-repeatable trigger working mode.

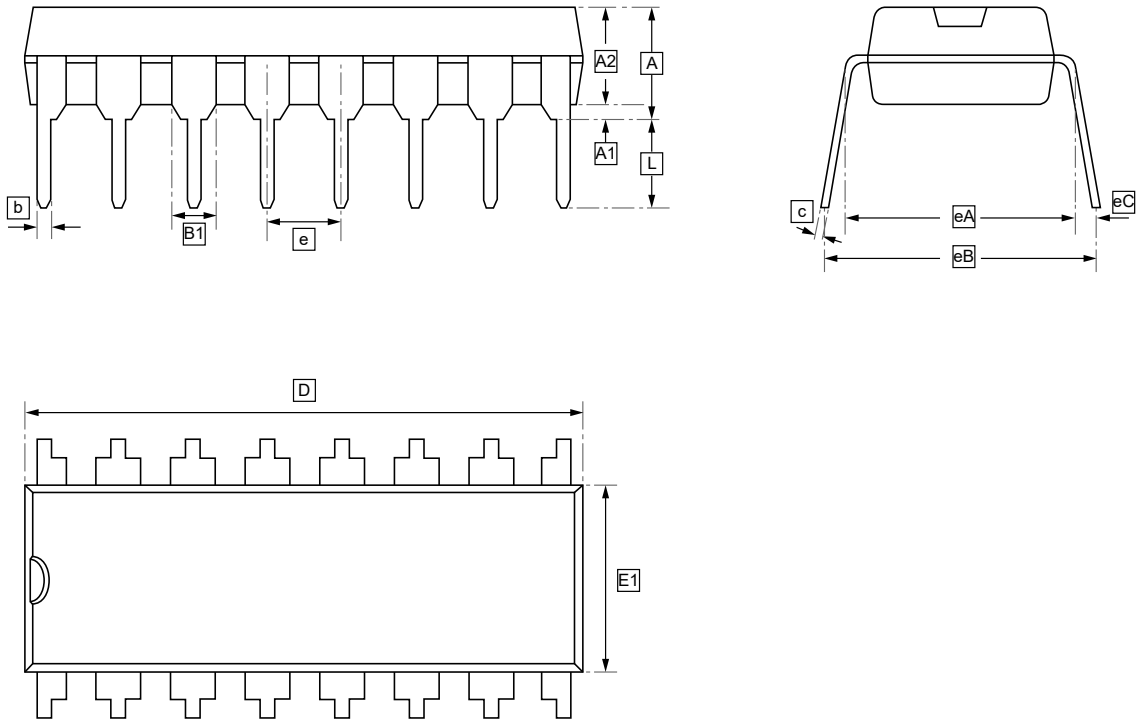
## 7.1 SOP-16 Package Outline Dimensions




**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | b | c | D | E | E1 | e | L | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Min** | 1.350 | 0 | 1.350 | 0.330 | 0.170 | 9.800 | 3.800 | 5.800 | 1.270 | 0.400 | 0° |
| **Max** | 1.750 | 0.100 | 1.550 | 0.510 | 0.250 | 10.200 | 4.000 | 6.200 | BSC | 1.270 | 8° |

## 7.2 DIP-16 Package Outline Dimensions




**DIMENSIONS (mm are the original dimensions)**

| Symbol | A | A1 | A2 | b | B1 | c | D | E1 | e | eA | eB | eC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | - | 0.50 | 3.20 | 0.38 | 1.52 | 0.20 | 18.90 | 6.15 | 2.54 | 7.62 | 7.62 | 0 |
| Max | 4.45 | - | 3.70 | 0.54 | BSC | 0.35 | 19.45 | 6.60 | BSC | BSC | 9.30 | 1.52 |

| Symbol | L |
|---|---|
| Min | 3.00 |
| Max | - |

## 8.Ordering Information


yy: Year Code
ww: Week Code

| Order Code | Marking | Package | Base QTY | Delivery Mode |
|---|---|---|---|---|
| UMW BISS0001 | BISS0001 | SOP-16 | 2500 | Tape and reel |
| UMW BISS0001N | BISS0001N | DIP-16 | 1000 | Tube and box |

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