UMW IRF4905STRLP

-55V P-Channel MOSFET

1.Description

Features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating.

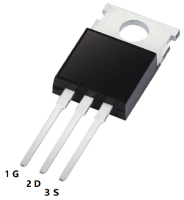
2.Features

- $V_{DS\ (V)}$=-55V
- I_D=-42A
- $R_{DS(ON)}$<20mΩ(V_{GS}=-10V)

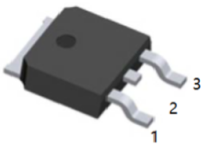
3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

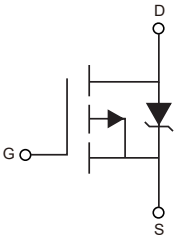
TO-263



TO-220



TO-252



4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V(Silicon Limited)	T_C=25°C	I_D	-70	A
Continuous Drain Current, V_{GS}=10V(See Fig. 9)	T_C=100°C		-44	A
Continuous Drain Current, V_{GS}=10V(Package Limited)	T_C=25°C		-42	A
Pulsed Drain Current ①		I_{DM}	-280	A
Maximum Power Dissipation	T_C=25°C	P_D	170	W
Linear Derating Factor			1.3	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Single Pulse Avalanche Energy ②		E_{AS}	140	mJ
Single Pulse Avalanche Energy Tested Value ⑥		$E_{AS(tested)}$	790	mJ
Avalanche Current ①		I_{AR}	See Fig.12a,	A
Repetitive Avalanche Energy ⑤		E_{AR}	12b,15,16	mJ
Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Soldering Temperature, for 10 seconds			300(1.6mm from case)	°C
Mounting torque, 6-32 or M3 screw ⑦			10 lbf•in (1.1N•m)	

5.Thermal Resistance Rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case ⑧	$R_{\theta JC}$		0.75	°C/W
Junction-to-Ambient (PCB Mount, steady state)⑦⑧	$R_{\theta JA}$		40	°C/W

6.Specifications (T_J= 25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-250μA, V_{GS}=0V	-55			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C,I_D=-1mA		-0.054		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-42A ③			20	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.1	-1.8	-2.5	V
Forward Transconductance	g_{FS}	V_{DS}=-25V, I_D=-42A		19		S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=-55V, V_{GS}=0V			-25	μA
		V_{DS}=-44V, V_{GS}=0V, T_J=125°C			-200	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=-20V			-100	nA
Gate-to-Source Reverse Leakage		V_{GS}=20V			100	nA
Total Gate Charge	Q_g	I_D=-42A,V_{DS}=-44V V_{GS}=-10V ③		120	180	nC
Gate-to-Source Charge	Q_{gs}			32		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			53		nC
Tum-On Delay Time	$t_{D(on)}$	V_{DD}=-28V, I_D=-42A R_G=2.6Ω, V_{GS}=-10V ③		20		ns
Rise Time	t_r			99		ns
Turn-Off Delay Time	$t_{D(off)}$			51		ns
Fall Time	t_f			64		ns
Internal Source Inductance	L_S	Between lead, and center of die contact		7.5		nH
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-25V, f=1MHz		3500		pF
Output Capacitance	C_{oss}			1250		pF
Reverse Transfer Capacitance	C_{rss}			450		pF
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=-1V, f=1MHz		4620		pF
Output Capacitance	C_{oss}	V_{GS}=0V, V_{DS}=-44V, f=1MHz		940		pF
Effective Output Capacitance	C_{oss}eff.	V_{GS}=0V, V_{DS}=0V to -44V ④		1530		pF

Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			-42	A
Pulsed Source Current (Body Diode) ①	I_{SM}				-280	A
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=-42A,V_{GS}=0V③			-1.3	V
Reverse Recovery Time	t_{rr}	T_J=25°C,I_F=-42A,V_{DD}=-28V di/dt=-100A/μs ③		61	92	ns
Reverse Recovery Charge	Q_{rr}			150	220	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J=25°C, L=0.16mH, R_G=25Ω, I_{AS}=-42A, V_{GS}=-10V. Part not recommended for use above this value.

③ Pulse width ≤ 1ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

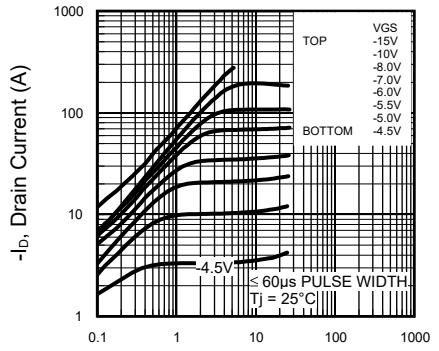
⑤ Limited by TJmax , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ This is applied to D2Pak, when mounted on 1" square PCB (FR- 4 or G-10 Material).

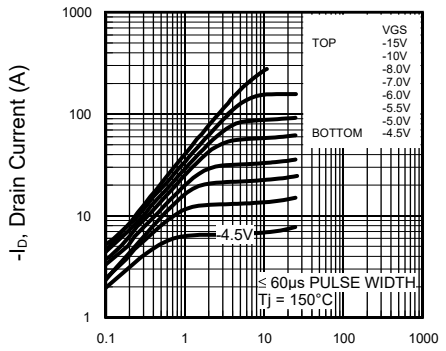
⑧ R_θ is measured at T_J approximately 90°C.

7.1Typical Characterisitics



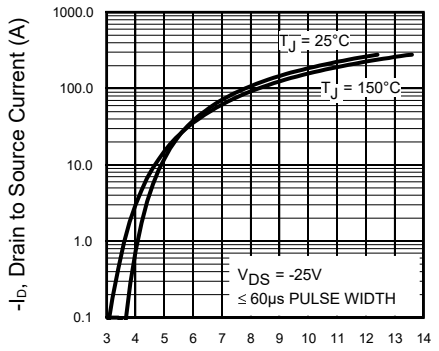
-V_{DS},Drain to Source Voltage (V)

Figure 1: Typical Output Characteristics



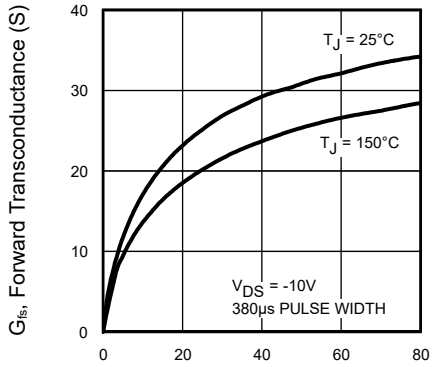
-V_{DS},Drain to Source Voltage (V)

Figure 2: Typical Output Characteristics



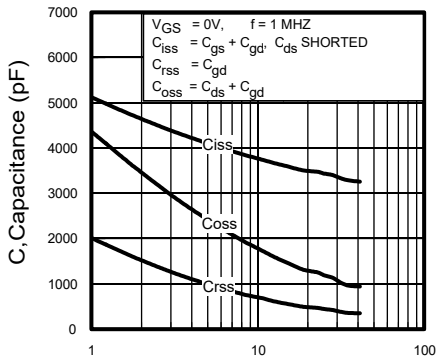
-V_{GS},Gate to Source Voltage (V)

Figure 3: Typical Transfer Characteristics



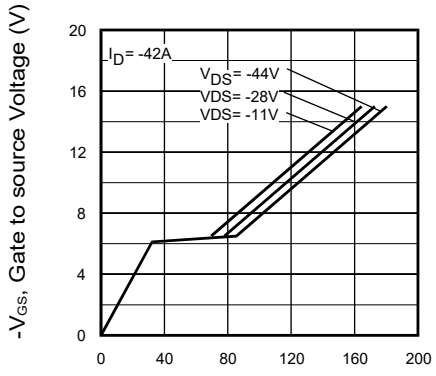
-I_D, Drain to Source Current (A)

Figure 4: Typical Forward Transconductance vs. Drain Current



-V_{DS},Drain to Source Voltage (V)

Figure 5: Typical Capacitance vs. Drain-to-Source Voltage



Q_G, Total Gate Charge (nC)

Figure 6: Typical Gate Charge vs. Gate-to-Source Voltage

7.2Typical Characterisitics

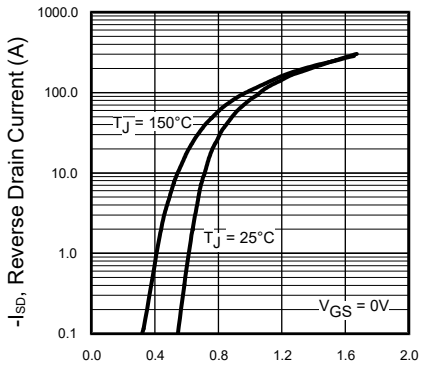


Figure 7: Typical Source-Drain Diode Forward Voltage

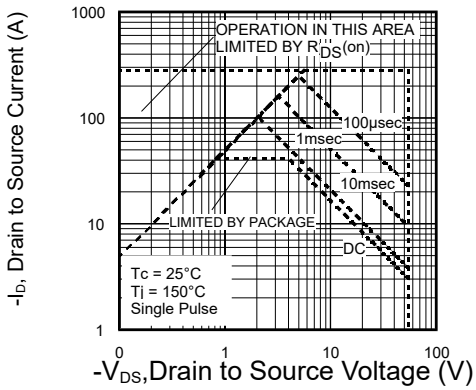


Figure 8: Maximum Safe Operating Area

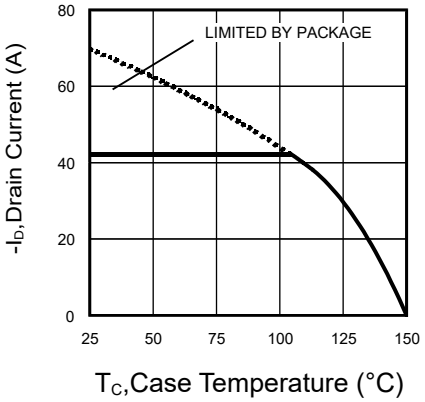


Figure 9: Maximum Drain Current vs. Case Temperature

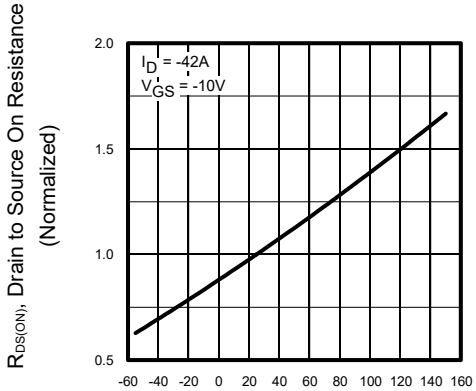


Figure 10: Drain-to-Source Breakdown Voltage

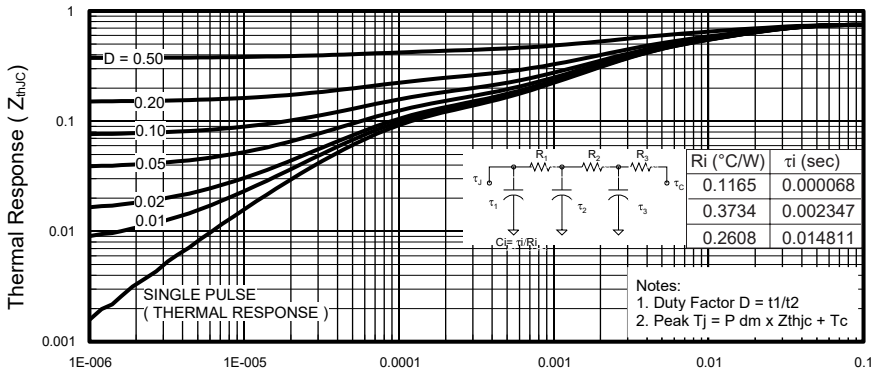


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

7.3Typical Characterisitics

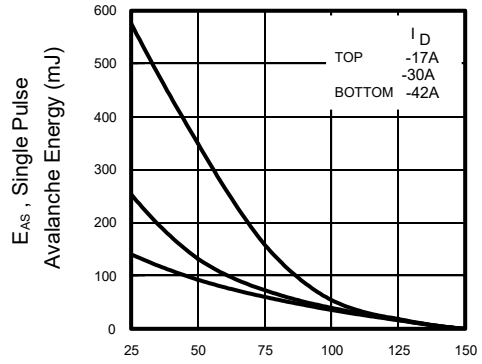


Figure 12c: Maximum Avalanche Energy vs. Drain Current

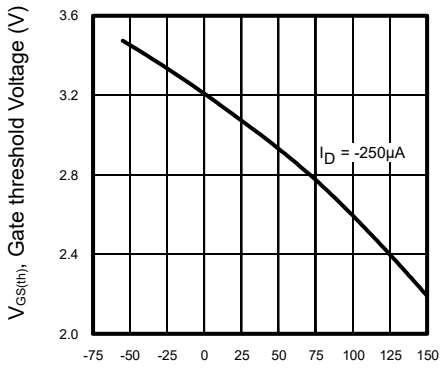


Figure 14:Threshold Voltage vs. Temperature

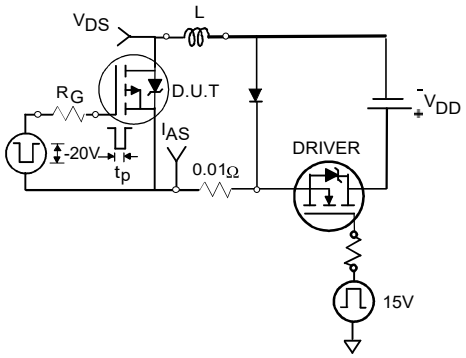


Figure 12a: Unclamped Inductive Test Circuit

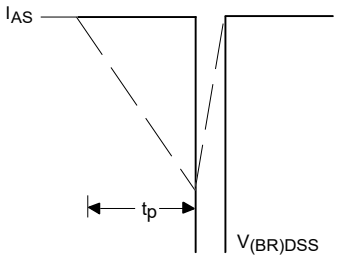


Figure 12b: Unclamped Inductive Waveforms

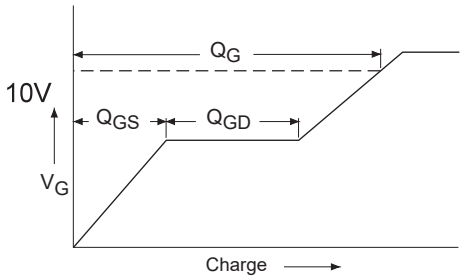


Figure 13a: Basic Gate Charge Waveform

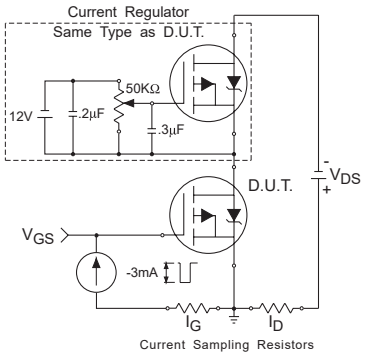


Figure 13b: Gate Charge Test Circuit

7.4Typical Characterisitics

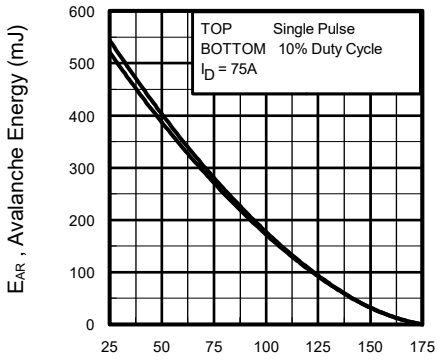


Figure 15: Maximum Avalanche Energy Vs. Temperature

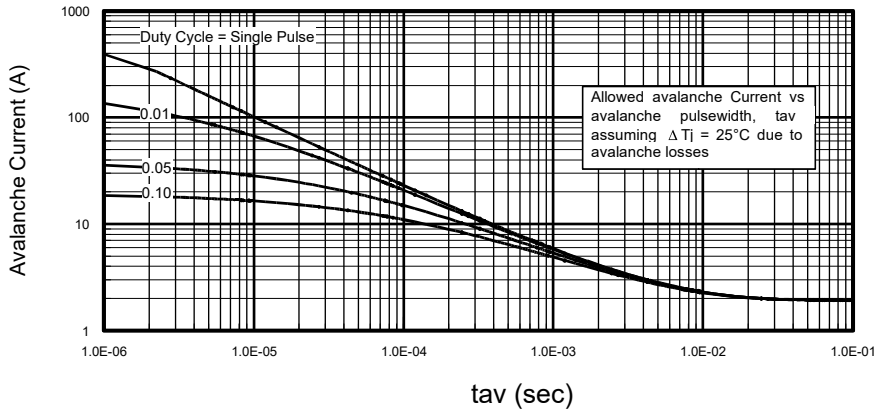


Figure 16: Typical Avalanche Current Vs.Pulsewidth

Notes on Repetitive Avalanche Curves , Figures 15, 16:

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15,16).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

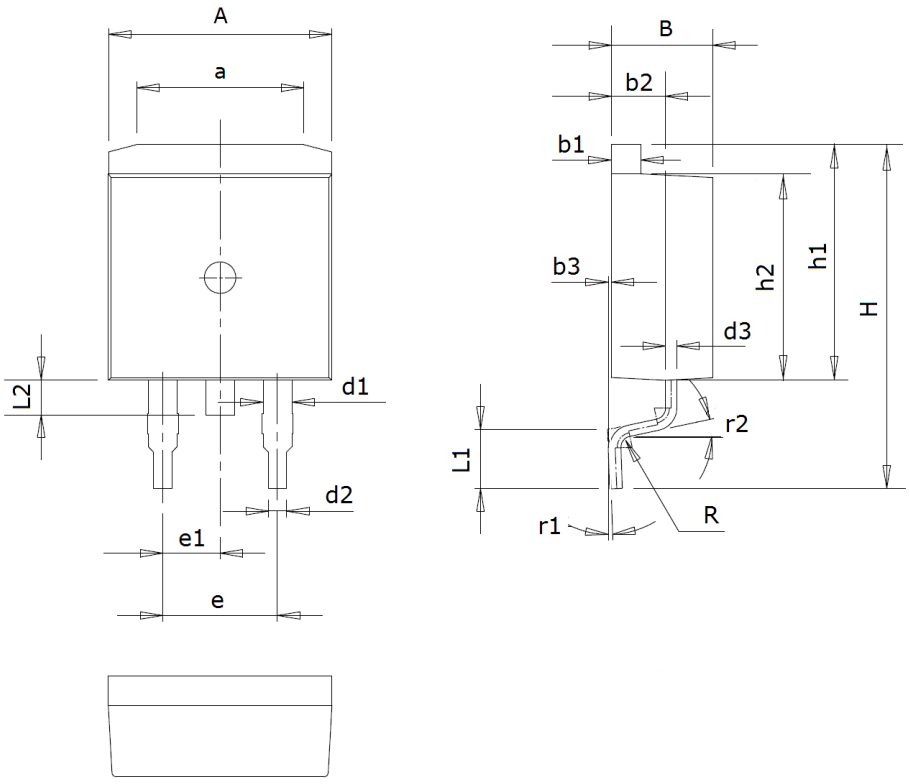
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11).

$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

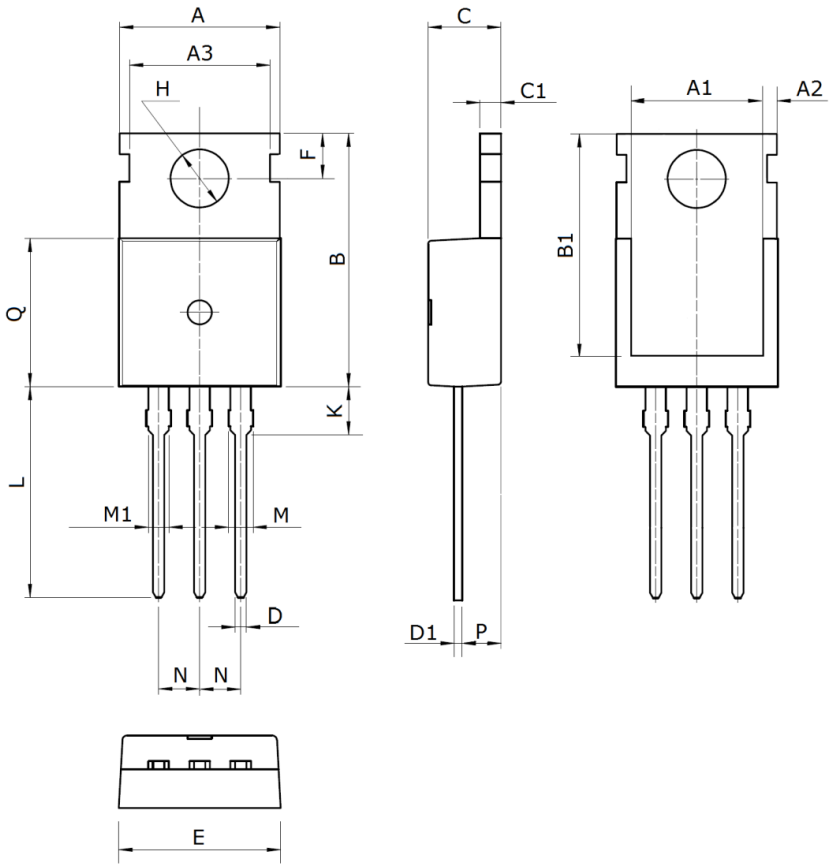
8.1TO-263 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	Dimensions(mm)	Symbol	Dimensions(mm)	Symbol	Dimensions(mm)
A	9.7~10.3	d2	0.7~0.9	L1	2.4~2.9
a	7.0~7.8	d3	0.4~0.6	L2	1.3~1.8
B	4.3~4.7	e	5.08(typ)	R	0.5(typ)
b1	1.25~1.35	e1	2.54(typ)	r1	0~8°
b2	2.2~2.6	H	14.8~15.6	r2	12°(typ)
b3	0~0.2	h1	10.2~10.7		
d1	1.2~1.4	h2	8.9~9.4		

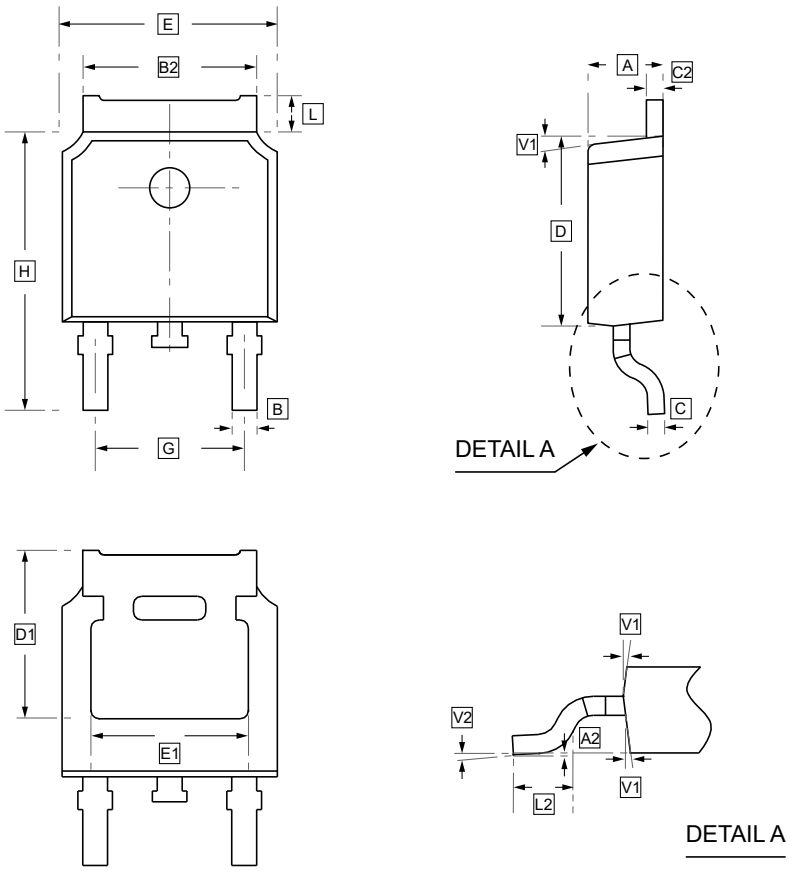
8.2Package Mechanical Data TO-220



DIMENSIONS (mm are the original dimensions)

Symbol	Dimensions(mm)	Symbol	Dimensions(mm)	Symbol	Dimensions(mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	2.8±0.1	P	2.4±0.3
B1	13.2±0.2	H	3.6±0.1	Q	9.15±0.25
C	4.5±0.2	K	3.1±0.2		

8.3TO-252 PACKAGE OUTLINE DIMENSIONS

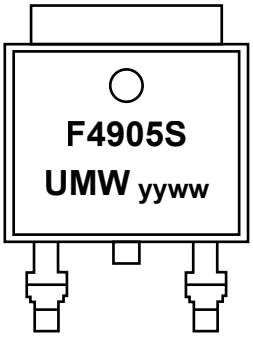


DIMENSIONS (mm are the original dimensions)

Symbol	A	A2	B	B2	C	C2	D	D1	E	E1	G	H	L	L2	V1	V2
Min	2.10	0	0.66	5.18	0.40	0.44	5.90	5.30	6.40	4.63	4.47	9.50	1.09	1.35		0°
Max	2.50	0.10	0.86	5.48	0.60	0.58	6.30	REF	6.80		4.67	10.70	1.21	1.65		6°

9.Ordering information

TO-252



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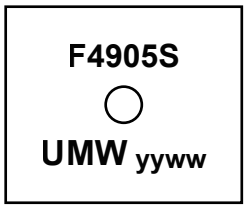
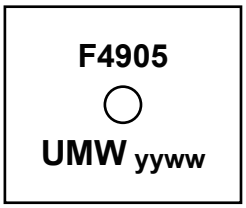


TO-220



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW IRF4905STRL	F4905S	TO-252	2500	Tape and reel
UMW IRF4905STRLP	F4905S	TO-263	800	Tape and reel
UMW IRF4905	F4905S	TO-220	1000	Tube and Box

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