

1.Description

The AO4405 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications.

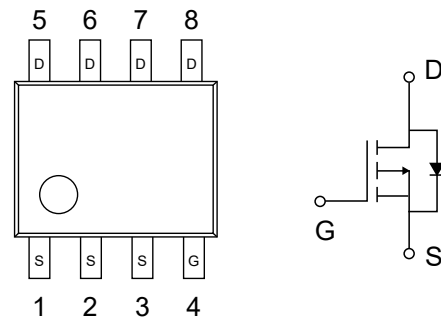
2.Features

- $V_{DS} = -30V$
- $I_D = -6A$
- $R_{DS(ON)} < 45m\Omega (V_{GS} = 10V)$

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25^\circ C$	I_D	-6	A
	$T_A = 70^\circ C$		-5.1	
Pulsed Drain Current ^C		I_{DM}	-30	
Avalanche Current ^C		I_{AS}, I_{AR}	17	A
Avalanche energy $L = 0.1mH$ ^C		E_{AS}, E_{AR}	14	mJ
V_{DS} Spike	10 μs	V_{SPIKE}	-36	V
Power Dissipation ^B	$T_A = 25^\circ C$	P_D	3.1	W
	$T_A = 70^\circ C$		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$



5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	t ≤ 10s	R _{θJA}	31	40	°C/W
Maximum Junction-to-Ambient ^{AD}	Steady-State		59	75	°C/W
Maximum Junction-to-Lead	Steady-State	R _{θJL}	16	24	°C/W



6. Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =-250μA, V _{GS} =0V	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	μA
		T _J =55°C			-5	
Gate-Body leakage current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.5	-2.5	V
On state drain current	I _{D(ON)}	V _{GS} =-10V, V _{DS} =-5V	-30			A
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-6A		33	45	mΩ
		V _{GS} =-4.5V, I _D =-5A		53	75	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-6A		14		S
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V		-0.8	-1	V
Maximum Body-Diode Continuous Current	I _S				-3.5	A
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-15V, f=1MHz		520		pF
Output Capacitance	C _{oss}			100		pF
Reverse Transfer Capacitance	C _{rss}			65		pF
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	3.5	7.5	11.5	Ω
Total Gate Charge	Q _g (10V)	V _{GS} =-10V, V _{DS} =-15V I _D =-6A		9.2	11	nC
Total Gate Charge	Q _g (4.5V)			4.6	6	nC
Gate Source Charge	Q _{gs}			1.6		nC
Gate Drain Charge	Q _{gd}			2.2		nC
Turn-On DelayTime	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V R _L =2.5Ω, R _{GEN} =3Ω		7.5		ns
Turn-On Rise Time	t _r			5.5		ns
Turn-Off DelayTime	t _{D(off)}			19		ns
Turn-Off Fall Time	t _f			7		ns
Body Diode Reverse Recovery Time	t _{rr}	I _F =-6A, dI/dt=100A/μs		11		ns
Body Diode Reverse Recovery Charge	Q _{rr}	I _F =-6A, dI/dt=100A/μs		5.3		nC



- A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on $T_{J(\text{MAX})} = 150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.
- C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})} = 150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^\circ\text{C}$.
- D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using $< 300\mu\text{s}$ pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(\text{MAX})} = 150^\circ\text{C}$. The SOA curve provides a single pulse rating



7.1 Typical characteristic

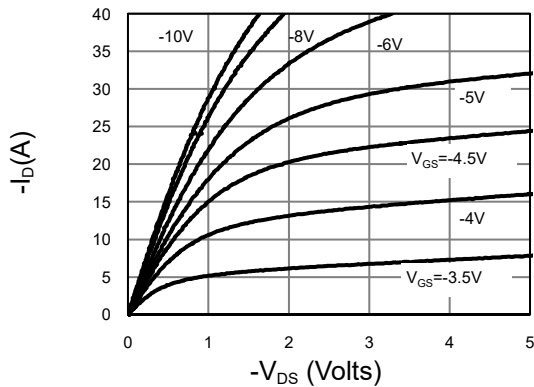


Fig 1: On-Region Characteristics (Note E)

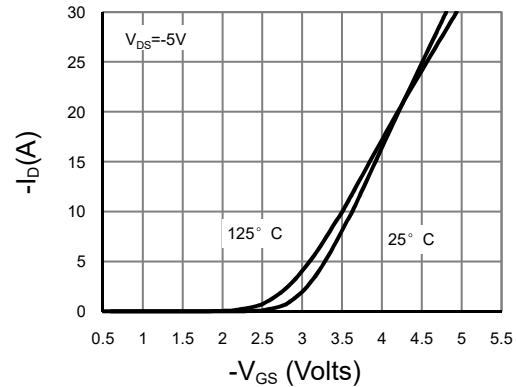


Figure 2: Transfer Characteristics (Note E)

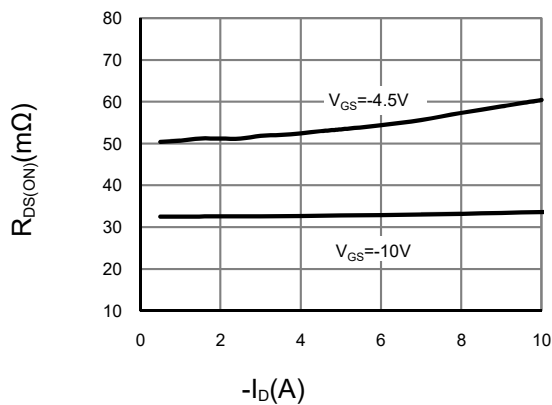


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

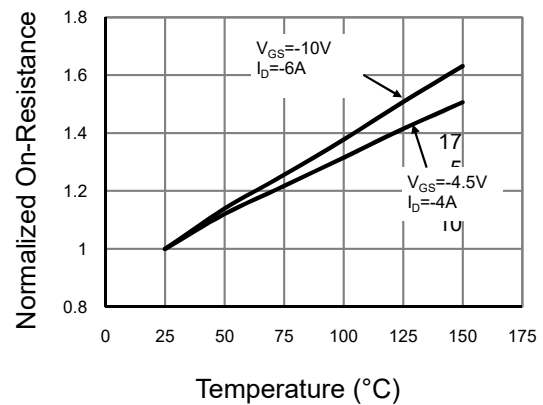


Figure 4: On-Resistance vs. Junction Temperature (Note E)

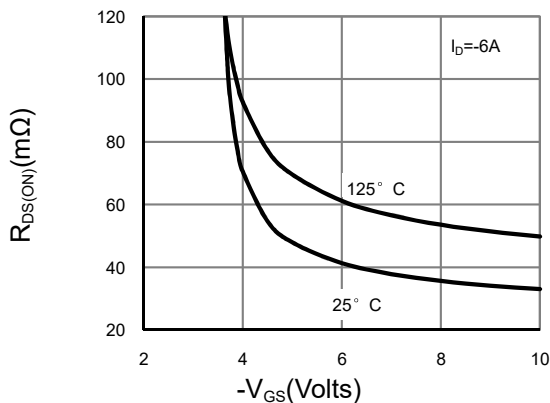


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

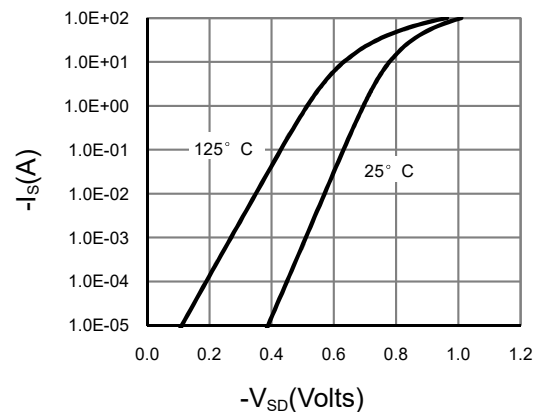


Figure 6: Body-Diode Characteristics (Note E)



7.2 Typical characteristic

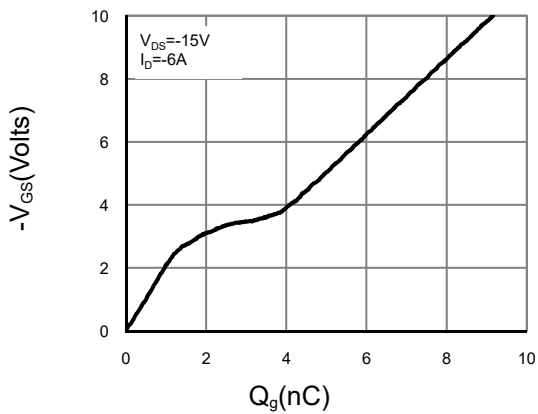


Figure 7: Gate-Charge Characteristics

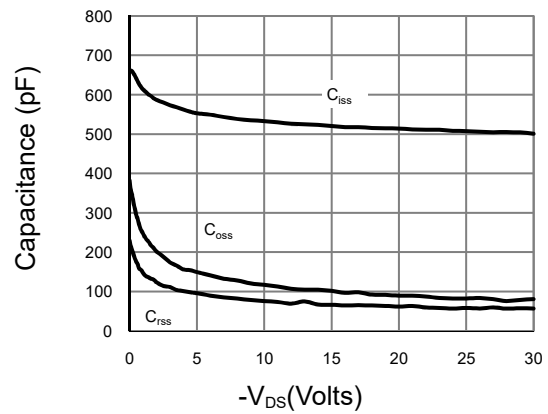


Figure 8: Capacitance Characteristics

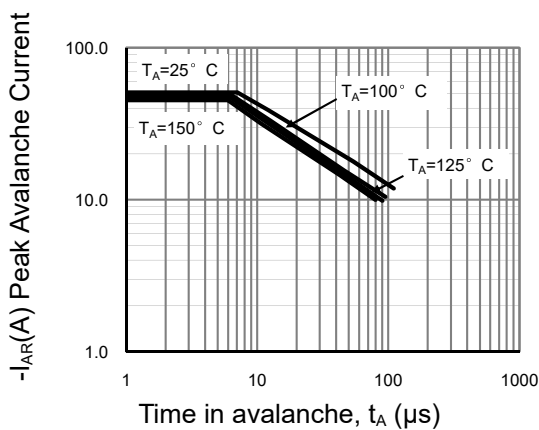


Figure 9: Single Pulse Avalanche capability (Note C)

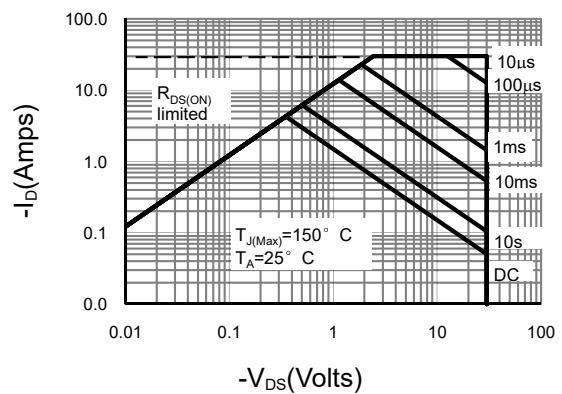


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

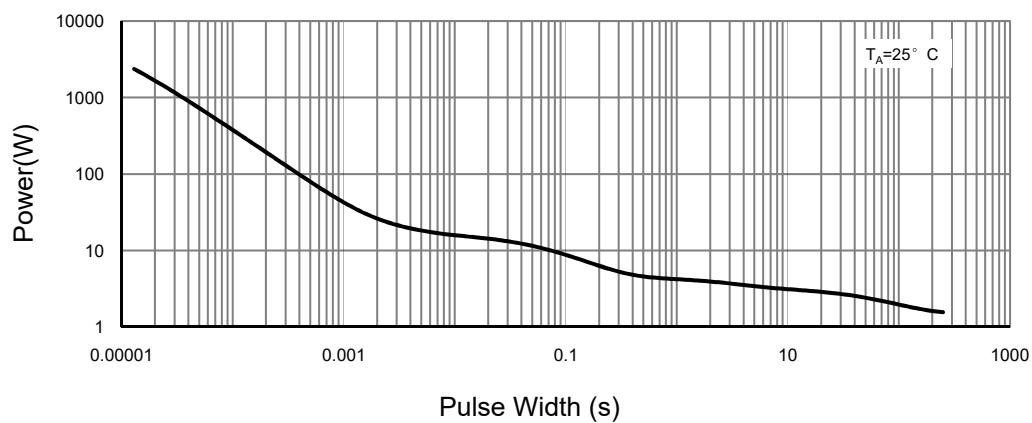
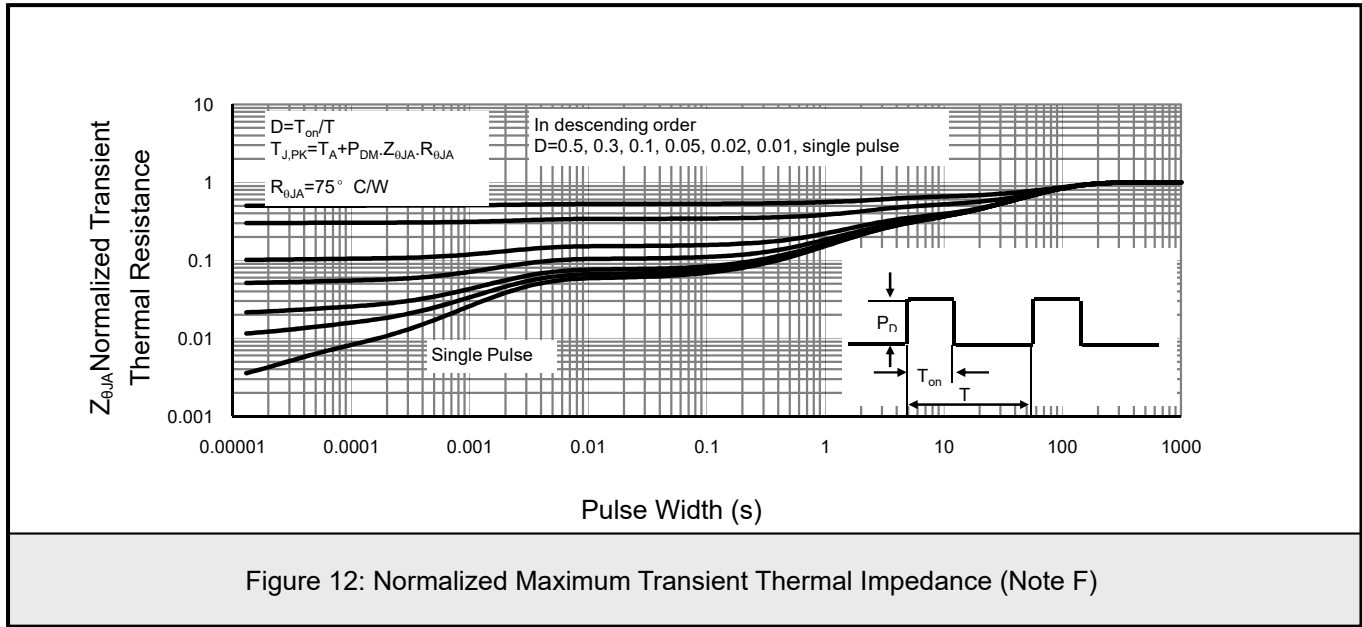


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

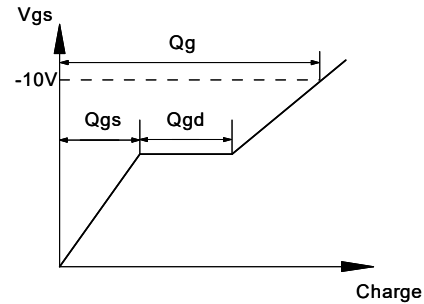
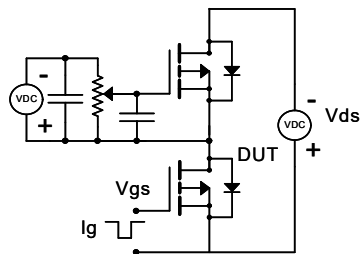


7.3Typical characteristic

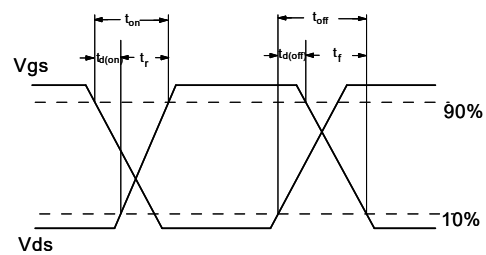
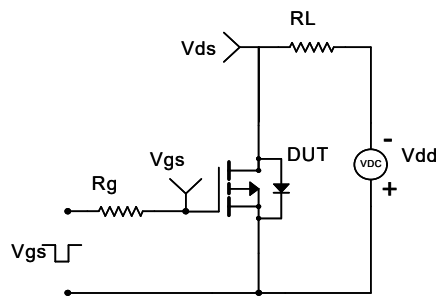




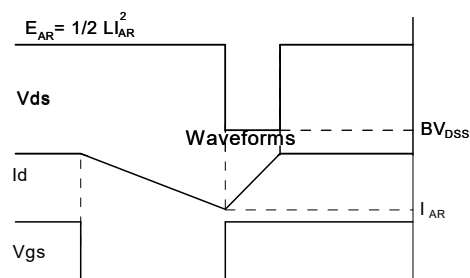
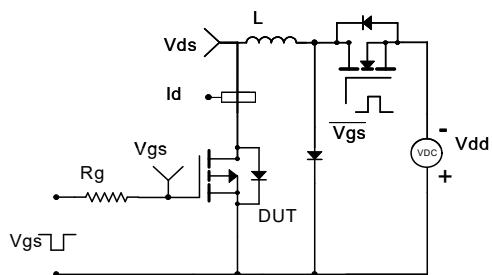
Gate Charge Test Circuit & Waveform



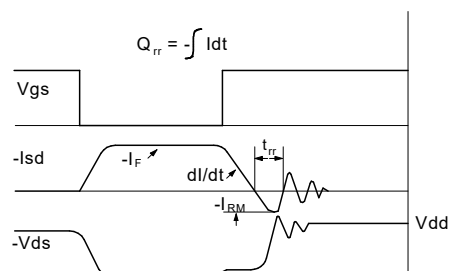
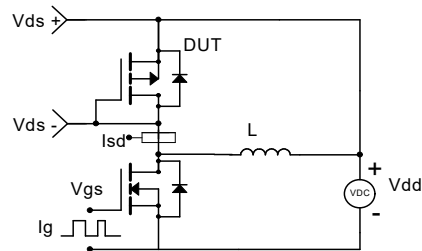
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

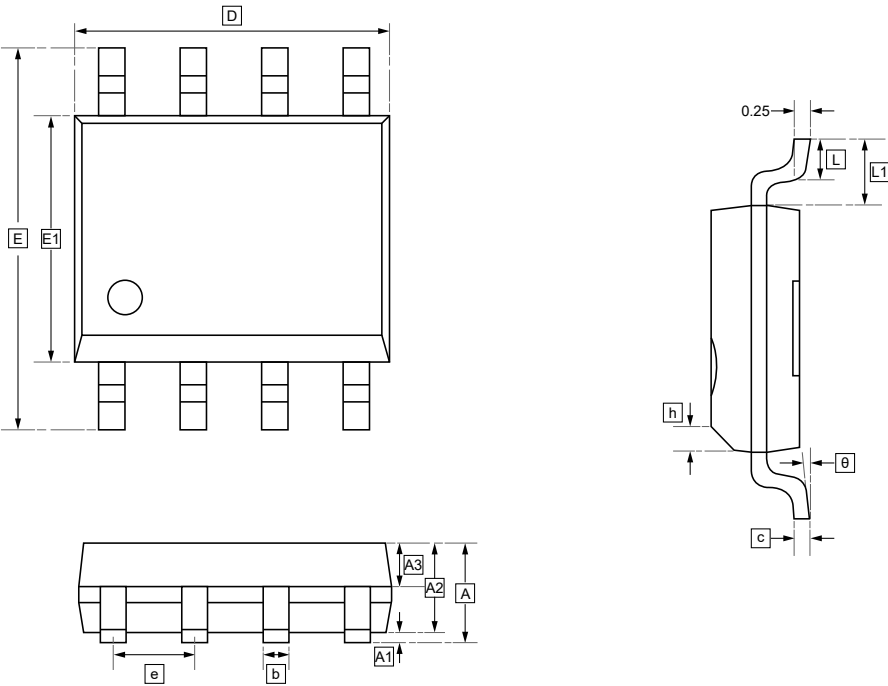


Diode Recovery Test Circuit & Waveforms





8.SOP-8 Package Outline Dimensions



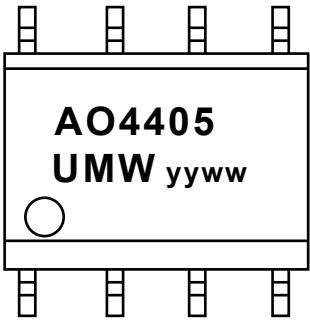
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4405	SOP-8	3000	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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