

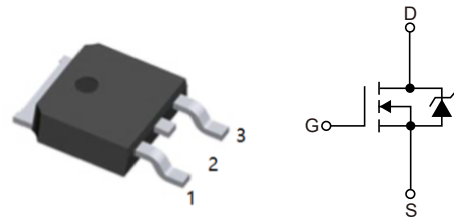
1.Features

- $V_{DS(V)}=60V$
- $R_{DS(ON)}<47m\Omega(V_{GS}=5V)$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drives
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits

2.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view



3.Absolute Maximum Ratings $T_c=25^{\circ}C$

Parameter	Symbol	Rating	Units
Drain to Source Voltage (Note 1)	V_{DS}	60	V
Drain to Gate Voltage ($R_{GS}=20k\Omega$)(Note 1)	V_{DGR}	60	V
Continuous Drain Current	I_D	16	A
Pulsed Drain Current (Note 3)	I_{DM}	45	A
Gate to Source Voltage	V_{GS}	± 10	V
Maximum Power Dissipation	P_D	60	W
Derate Above $25^{\circ}C$		0.48	W/ $^{\circ}C$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	$^{\circ}C$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	$^{\circ}C$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	$^{\circ}C$

Notes:

1. $T_J=25^{\circ}C$ to $125^{\circ}C$.



4. Electrical Characteristic ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D=250mA$, $V_{GS}=0V$, Figure 10		60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250mA$,Figure 9		1		2	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V$, $V_{GS}=0V$				1	μA
		$V_{DS}=40V$, $V_{GS}=0V$, $T_C=150^{\circ}C$				50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS}=\pm 10V$, $V_{DS}=0V$				± 100	nA
Drain to Source On Resistance (Note 2)	$R_{DS(ON)}$	$I_D=16A$, $V_{GS}=5V$				47	m Ω
		$I_D=16A$, $V_{GS}=4V$				56	m Ω
Turn-On Time	$t_{(on)}$	$V_{DD}=25V$, $I_D=8A$ $V_{GS}=5V$, $R_{GS}=12.5\Omega$ Figures 15, 16				60	ns
Turn-On Delay Time	$t_{D(on)}$				14		ns
Rise Time	t_r				30		ns
Turn-Off Delay Time	$t_{D(off)}$				42		ns
Fall Time	t_f				14		ns
Turn-Off Time	$t_{(off)}$					100	ns
Total Gate Charge	$Q_{g(tot)}$	$V_{GS}=0V$ to 10V	$V_{DD}=40V$, $I_D=16A$ $R_L=2.5\Omega$ Figures 17, 18			80	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS}=0V$ to 5V				45	nC
Threshold Gate Charge	$Q_{g(th)}$	$V_{GS}=0V$ to 1V				3	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$					2.083	$^{\circ}C/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$					100	$^{\circ}C/W$
Source to Drain Diode Specifications							
Source to Drain Diode Voltage	V_{SD}	$I_{SD}=16A$				1.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD}=16A$, $dI_{SD}/dt=100A/\mu s$				125	ns

Notes:

- Pulse Test: Pulse Width $\leq 300\text{ms}$, Duty Cycle $\leq 2\%$.
- Repetitive Rating: Pulse Width limited by max junction temperature.



5.1 Typical characteristic

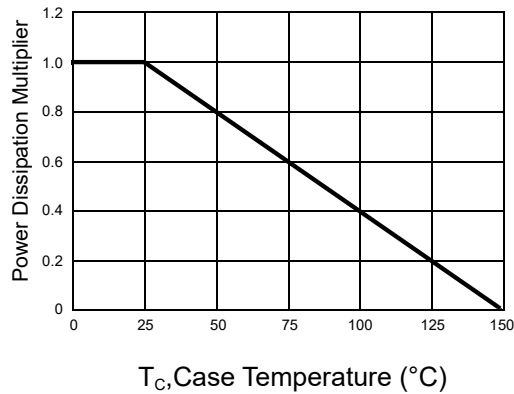


Figure 1: Normalized Power Dissipation Vs Case Temperature

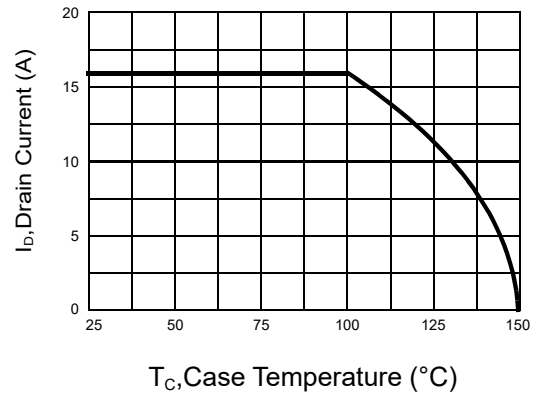


Figure 2: Maximum Continuous Drain Current Vs Temperature

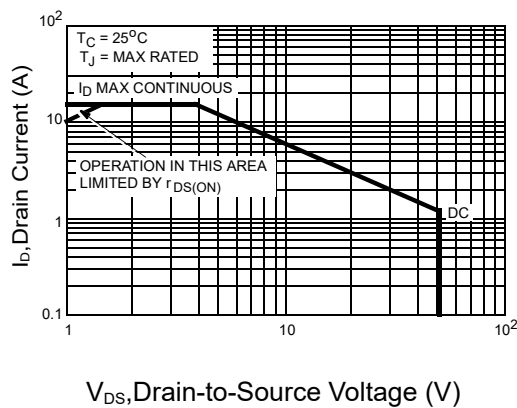


Figure 3: Forward Bias Safe Operating Area

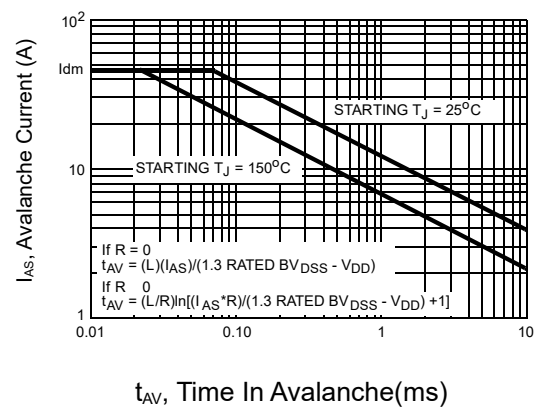


Figure 4: Unclamped Inductive Switching Soa (Single Pulse Uis Soa)

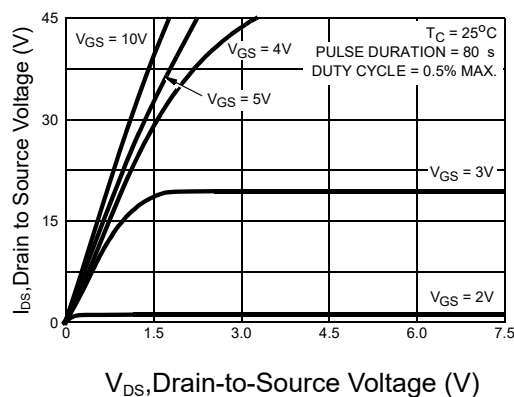


Figure 5: Saturation Characteristics

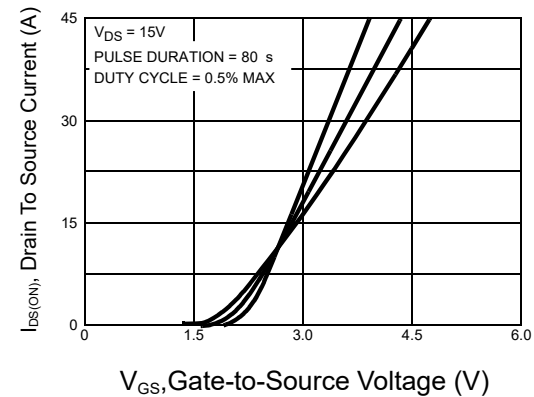


Figure 6: Transfer Characteristics



5.2 Typical characteristic

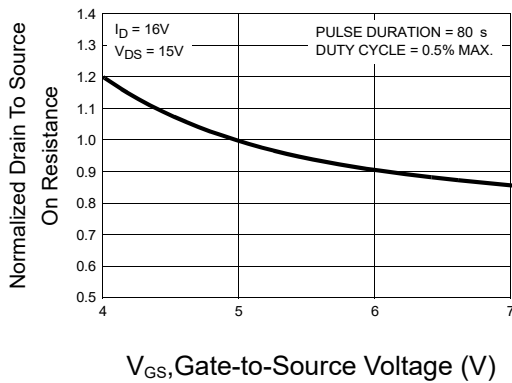


Figure 7: Drain To Source On Resistance Vs Gate Voltage And Drain Current

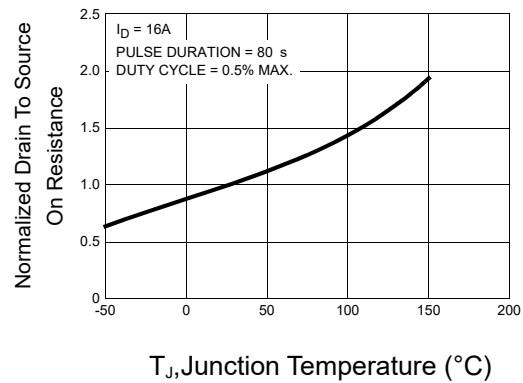


Figure 8: Normalized Drain To Source On Resistance Vs Junction Temperature

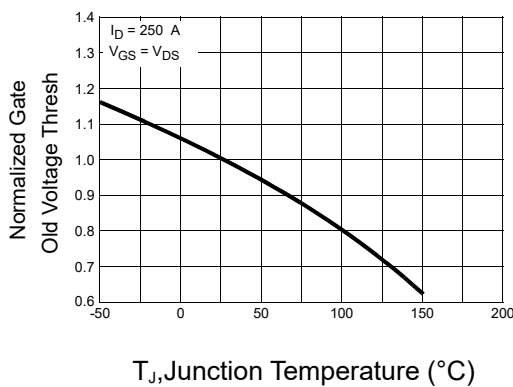


Figure 9: Normalized Gate Threshold Vs Junction Temperature

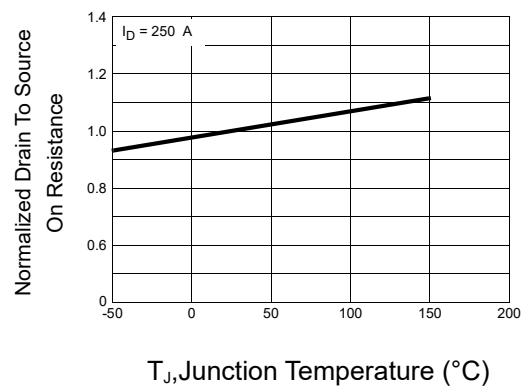


Figure 10: Normalized Drain To Source Breakdown Voltage Vs Junction Temperature

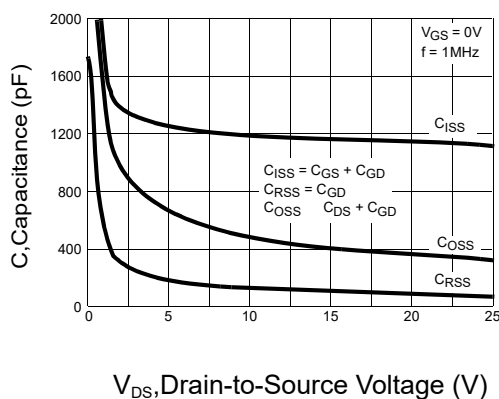


Figure 11: Capacitance Vs Drain To Source Voltage

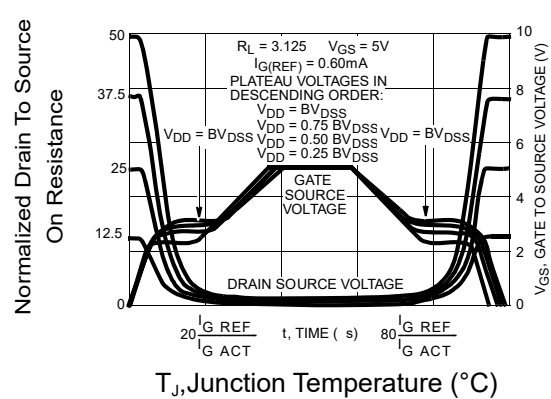


Figure 12: Normalized Switching Waveforms For Constant Gate Current



6. Test Circuits and Waveforms

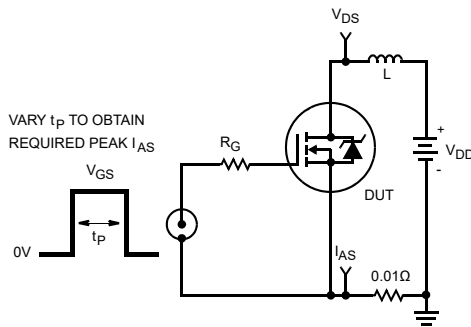


Figure 13: Unclamped Energy Test Circuit

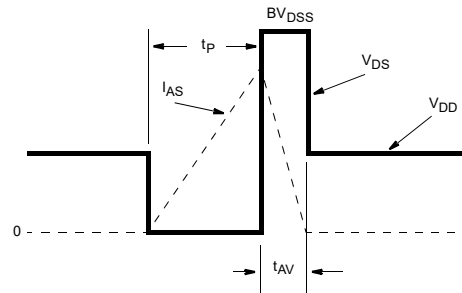


Figure 14: Unclamped Energy Waveforms

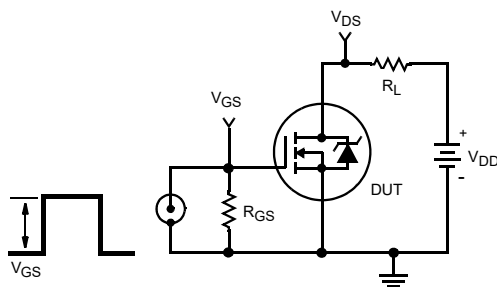


Figure 15: Switching Time Test Circuit

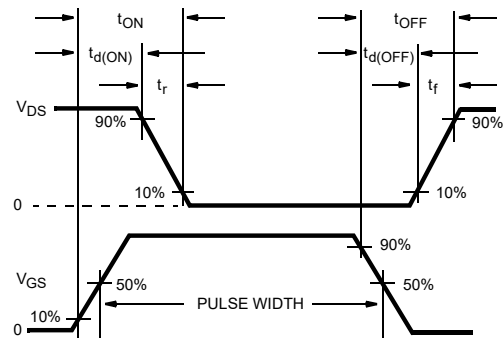


Figure 16: Resistive Switching Waveforms

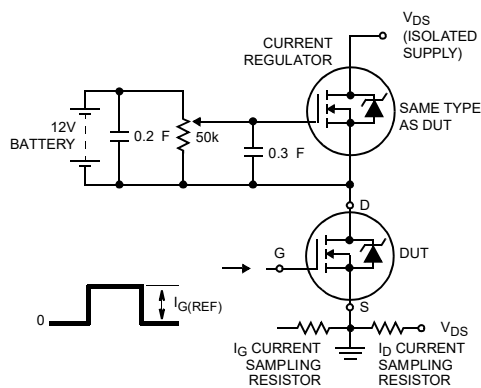


Figure 17: Gate Charge Test Circuit

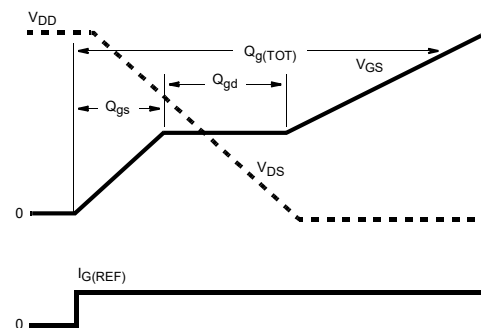
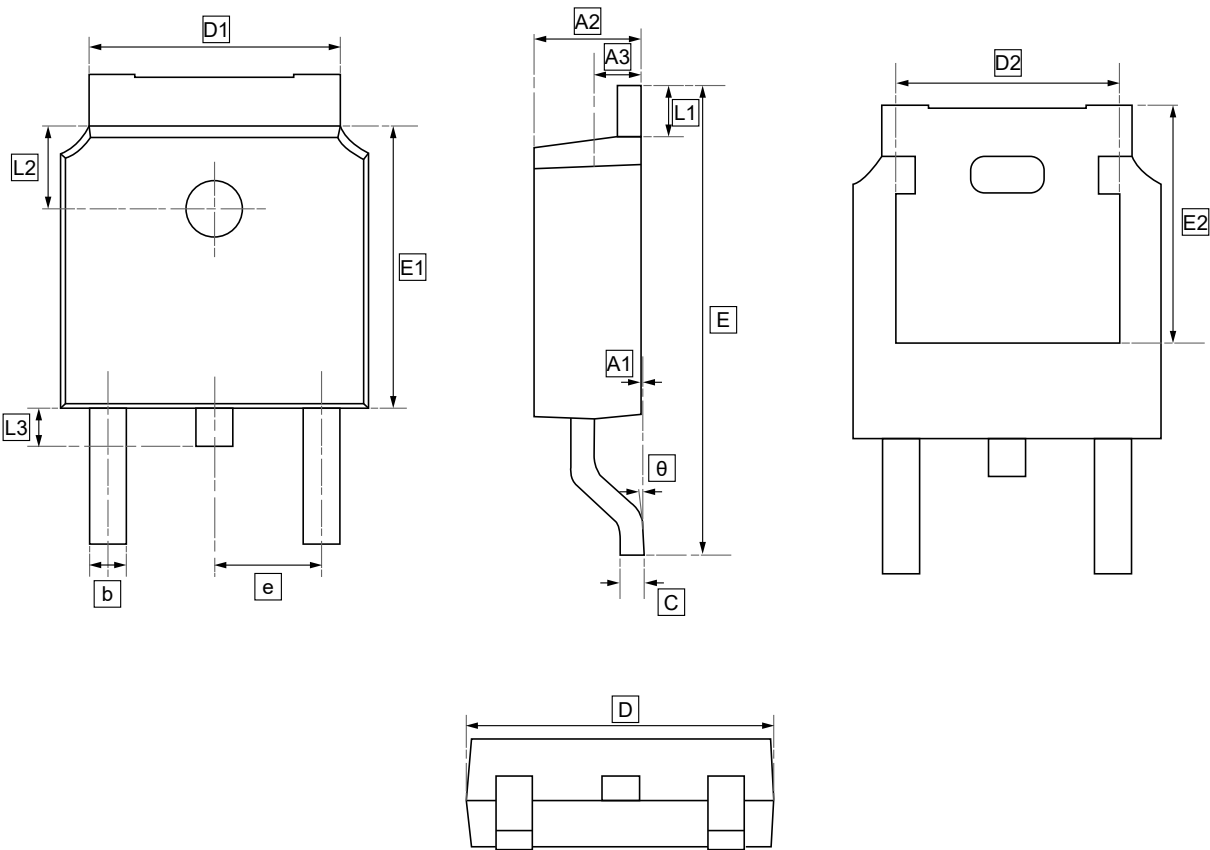


Figure 18: Gate Charge Waveforms



7.TO-252 Package Outline Dimensions

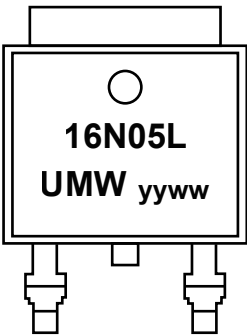


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286 BSC	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW RFD16N05LSM9A	TO-252	2500	Tape and reel



9.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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