

1. Description

This P-channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers, and battery chargers.

2.2 Features

- ESD protection diode (note 3)
- High power and current handling capability

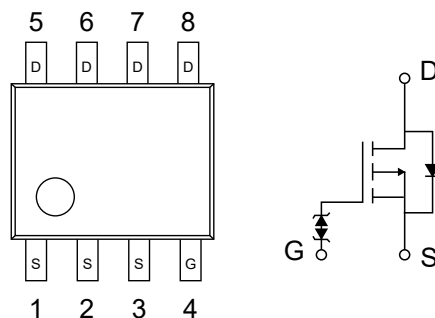
2.1 Features

- $V_{DS(V)} = -30V$
- $I_D = -16A$
- $R_{DS(ON)} < 7.2m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 11.5m\Omega (V_{GS} = -4.5V)$

3. Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4. Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	-30	V
Gate-Source Voltage	V_{GSS}	± 25	V
Drain Current – Continuous	I_D	-16	A
– Pulsed (Note 1a)		-50	
Power Dissipation for Single Operation	P_D	2.5	W
		1.2	
		1	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$



5. Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	25	°C/W



6. Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

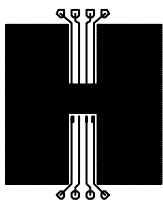
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=-250\mu\text{A}$ Referenced to 25°C		-22		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$			-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$			± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1	-1.5	-3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	$I_D=-250\mu\text{A}$ Referenced to 25°C		5		mV/ $^\circ\text{C}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10\text{V}$, $I_D=-16\text{A}$		6	7.2	m Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-15\text{A}$		9	11.5	m Ω
On-State Drain Current	$I_{D(on)}$	$V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$	-50			A
Forward Transconductance	g_{FS}	$V_{DS}=-5\text{V}$, $I_D=-13\text{A}$		43		S
Input Capacitance	C_{iss}	$V_{DS}=-15\text{V}$		3800		pF
Output Capacitance	C_{oss}	$V_{GS}=0\text{V}$		980		pF
Reverse Transfer Capacitance	C_{rss}	$f=1\text{MHz}$		490		pF
Gate Resistance	R_G	$V_{GS}=15\text{mV}$, $f=1\text{MHz}$		3		Ω
Turn-On DelayTime	$t_{D(on)}$	$V_{DD}=-15\text{V}$, $I_D=-1\text{A}$ $V_{GS}=-10\text{V}$, $R_{GEN}=6\Omega$		20	36	ns
Turn-On Rise Time	t_r			9	18	ns
Turn-Off DelayTime	$t_{D(off)}$			100	160	ns
Turn-Off Fall Time	t_f			55	88	ns
Total Gate Charge	Q_g	$V_{DS}=-15\text{V}$, $I_D=-16\text{A}$ $V_{GS}=-10\text{V}$		70	98	nC
Gate-Source Charge	Q_{gs}			10		nC
Gate-Drain Charge	Q_{gd}			16		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-2.5	A



Drain–Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-2.5A$ (Note 2)		-0.7	-1.2	V
Diode Reverse Recovery Time	T_{rr}	$I_F=-16A, dI_F/dt=100A/\mu s$		39		nS
Diode Reverse Recovery Charge	Q_{rr}	(Note 2)		24		nC

Notes:

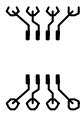
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W (10 sec)
62.5°C/W steady state
when mounted on a
1in² pad of 2 oz copper



b) 105° C/W when
mounted on a 0.4 in²
pad of 2 oz. copper.

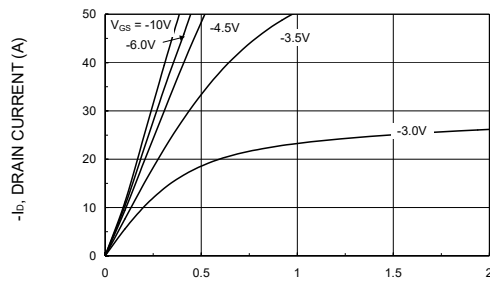


c) 125° C/W when
mounted on a minimum
pad.
Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

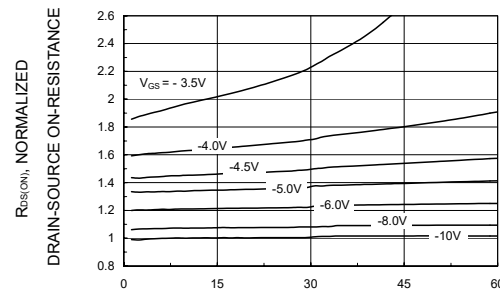


7.1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



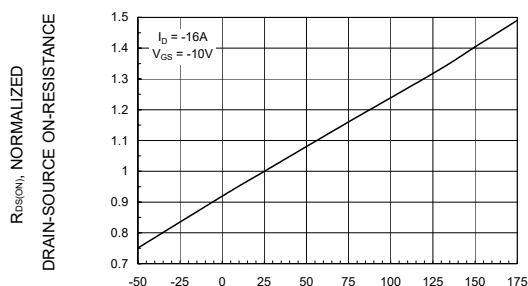
$-V_{DS}$, DRAIN TO SOURCE VOLTAGE (V)

Fig 1: On-Region Characteristics.



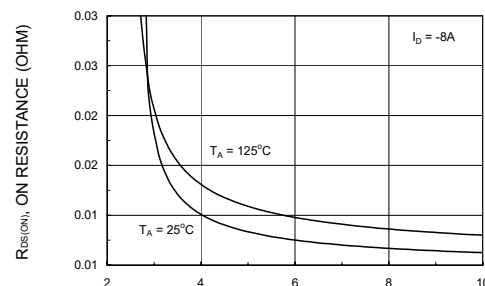
$-I_D$, DRAIN CURRENT (A)

Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.



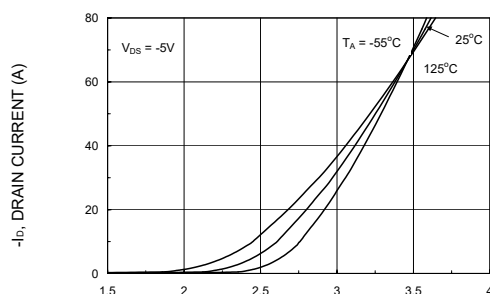
T_J , JUNCTION TEMPERATURE (°C)

Figure 3: On-Resistance Variation with Temperature.



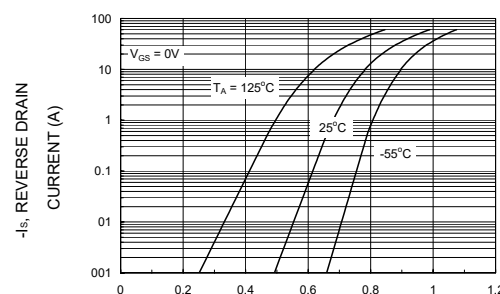
$-V_{GS}$, GATE TO SOURCE VOLTAGE (V)

Figure 4: On-Resistance Variation with Gate-to-Source Voltage.



$-V_{GS}$, GATE TO SOURCE VOLTAGE (V)

Figure 5: Transfer Characteristics.



$-V_{SD}$, BODY DIODE VOLTAGE (V)

Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.



7.2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

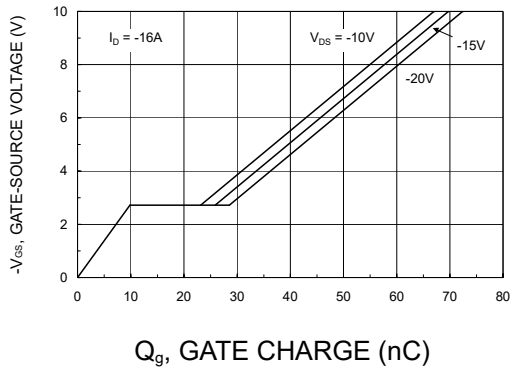


Figure 7: Gate-Charge Characteristics.

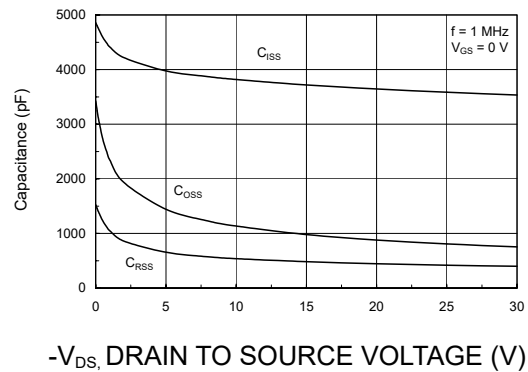


Figure 8: Capacitance Characteristics.

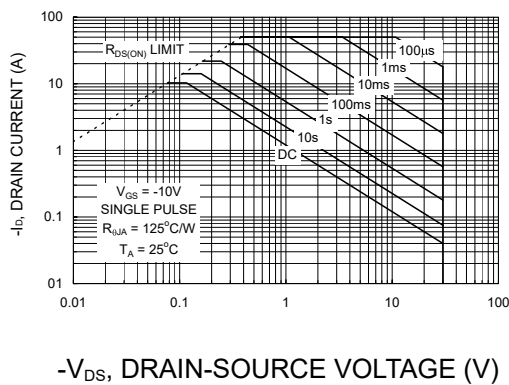


Figure 9: Maximum Safe Operating Area.

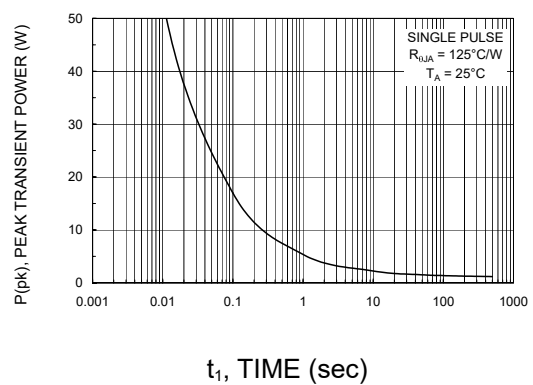


Figure 10: Single Pulse Maximum Power Dissipation.

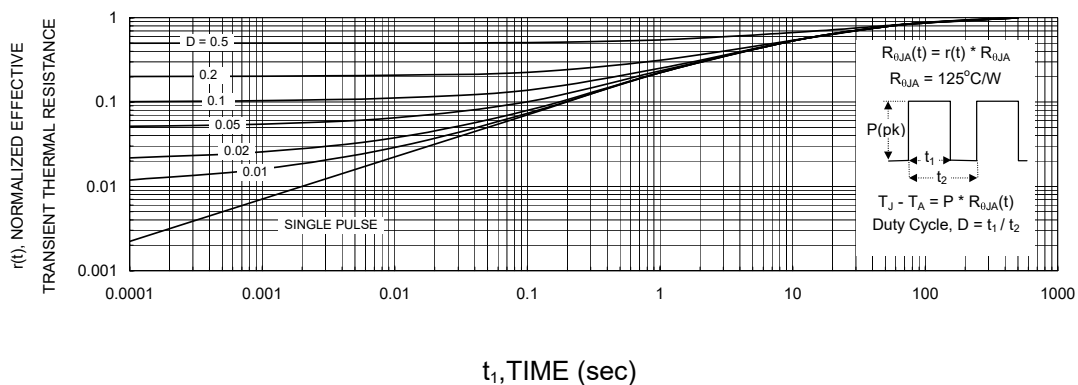
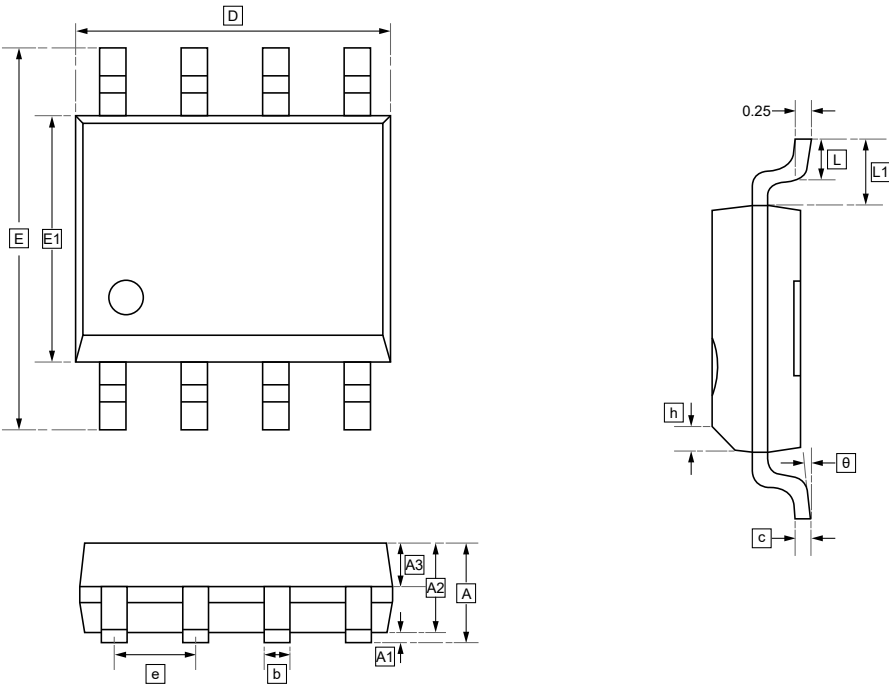


Figure 11: Transient Thermal Response Curve.



8.SOP-8 Package Outline Dimensions



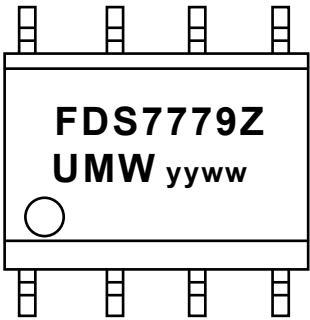
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS7779Z	SOP-8	3000	Tape and reel



10.Disclaimer

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