UMW ISL9N306AD3ST

30V N-Channel MOSFET

1.Description

This device employs a new advanced trench technology and features low gate charge while maintaining low on-resistance. Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

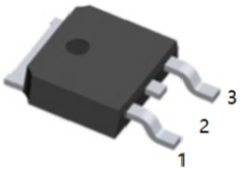
2.Features

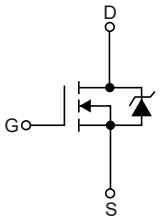
- $V_{DS\ (V)}$=30V
- I_D=50A
- $R_{DS(ON)}$<5.2mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<8.5mΩ(V_{GS}=4.5V)
- Q_g(Typ)=30nC, V_{GS}=5V
- Q_{gd}(Typ)=11nC
- C_{iss}(Typ)=3400pF

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	SOURCE
3	S	DRAIN

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_A= 25°C

Parameter	Symbol	Rating	Units
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (T_C=25°C, V_{GS}=10V)	I_D	50	A
Continuous (T_C=25°C, V_{GS}=4.5V)		50	A
Continuous (T_C=25°C, V_{GS}=V, $R_{\theta JC}$=52°C/W)		16	A
Pulsed		Figure 4	A
Power Dissipation	P_D	125	W
Derate above 25°C		0.83	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Case TO-252	$R_{\theta JC}$	1.2	°C/W
Thermal Resistance, Junction-to-Ambient TO-252	$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction-to-Ambient TO-252,1in^2 copper pad area	$R_{\theta JA}$	52	°C/W

6.Electrical Characteristic (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V		30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=25V				1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V				±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA		1		3	V
Drain to Source On Resistance	$R_{DS(ON)}$	I_D=50A, V_{GS}=10V			5.2	6	mΩ
		I_D=50A, V_{GS}=4.5V			8.5	9.5	mΩ
Input Capacitance	C_{iss}	I_D=15A,V_{GS}=0V, f=1MHz			3400		pF
Output Capacitance	C_{oss}				650		pF
Reverse Transfer Capacitance	C_{rss}				300		pF
Total Gate Charge at 10V	$Q_{g(TOT)}$	V_{GS}=0 to 10V	V_{DD}=15V		60	90	nC
Total Gate Charge at 5V	$Q_{g(5)}$	V_{GS}=0 to 5V	I_D=50A		30	45	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS}=0 to 1V	I_g=1mA		3	4.5	nC
Gate to Source Gate Charge	Q_{gs}				10		nC
Gate to Drain “Miller” Charge	Q_{gd}				11		nC
Turn-On Time	$t_{(on)}$	V_{DD}=15V, I_D=16A V_{GS}=4.5V, R_{GS}=4.3Ω				131	ns
Turn-On Delay Time	$t_{D(on)}$				16		ns
Rise Time	t_r				70		ns
Turn-Off DelayTime	$t_{D(off)}$				34		ns
Fall Time	t_f				30		ns
Turn-Off Time	t_{off}					97	ns
Turn-On Time	$t_{(on)}$	V_{DD}=15V, I_D=16A V_{GS}=10V, R_{GS}=4.3Ω				80	ns
Turn-On Delay Time	$t_{D(on)}$				10		ns
Rise Time	t_r				43		ns
Turn-Off DelayTime	$t_{D(off)}$				62		ns
Fall Time	t_f				29		ns
Turn-Off Time	t_{off}					137	ns

Avalanche Time	t_{av}	I_D=30A, L=200μH	428			μs
Source to Drain Diode Forward Voltage	V_{SD}	I_{SD}=50A			1.25	V
		I_{SD}=25A			1	V
Reverse Recovery Time	t_{rr}	I_{SD}=50A, dI_{SD}/dt=100A/μs			35	ns
Reverse Recovery Charge	Q_{rr}	I_{SD}=50A, dI_{SD}/dt=100A/μs			30	nC

7.1Typical characteristic

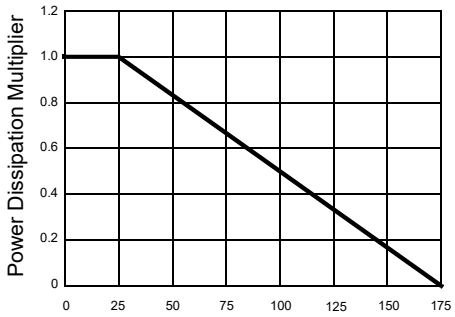


Figure 1: Normalized Power Dissipation vs Case Temperature

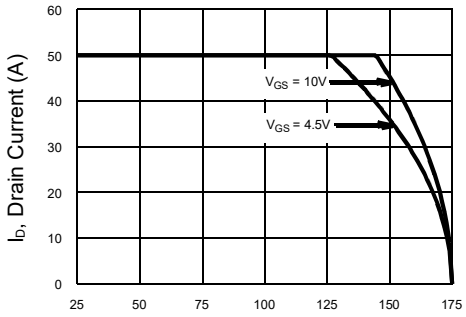


Figure 2: Maximum Continuous Drain Current vs Case Temperature

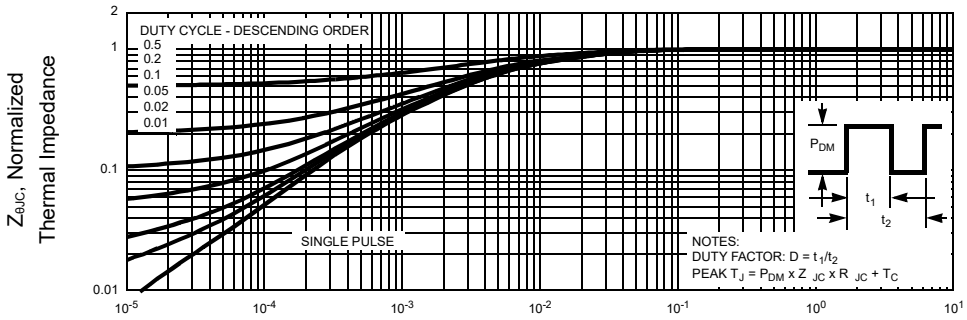


Figure 3: Normalized Maximum Transient Thermal Impedance

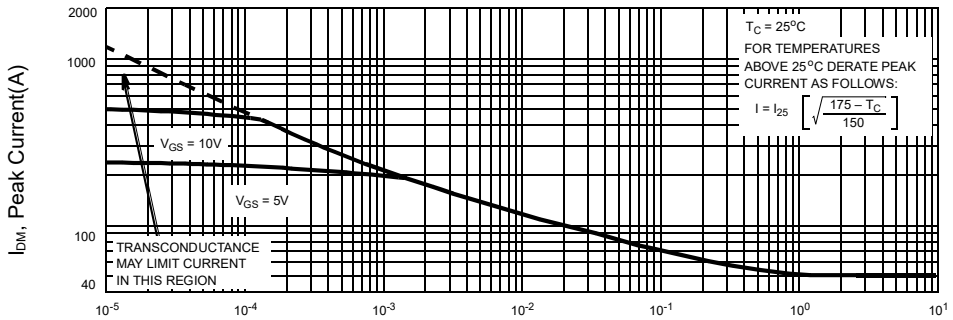


Figure 4: Peak Current Capability

7.2Typical characteristic

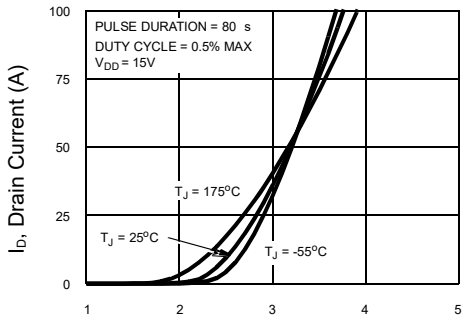


Figure 5: Transfer Characteristics

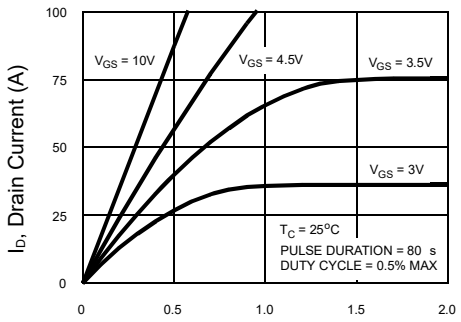


Figure 6: Saturation Characteristics

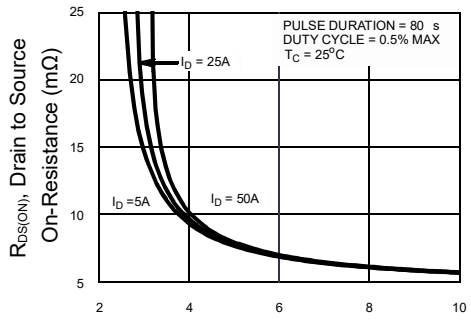


Figure 7: Drain to Source On Resistance vs Gate Voltage and Drain Current

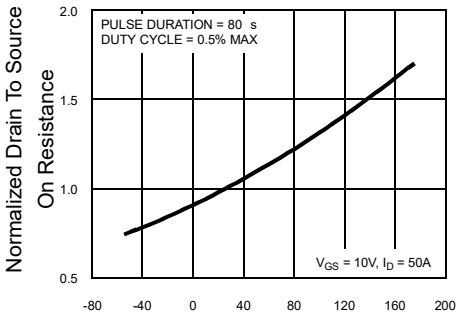


Figure 8: Normalized Drain to Source On Resistance vs Junction Temperature

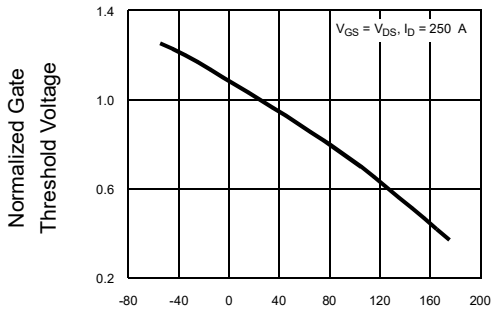


Figure 9: Normalized Gate Threshold Voltage vs Junction Temperature

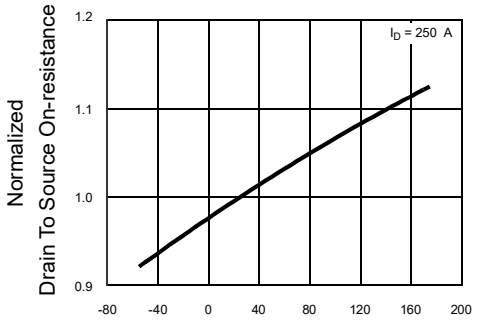


Figure 10: Normalized Drain to Source On Resistance vs Junction Temperature

7.3Typical characteristic

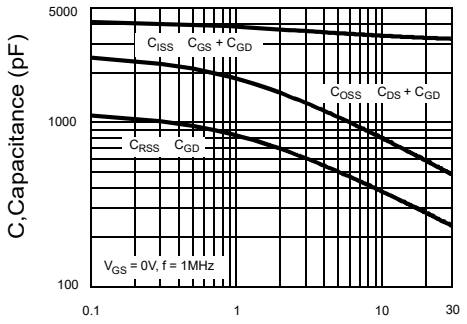


Figure 11: Capacitance vs Drain to Source Voltage

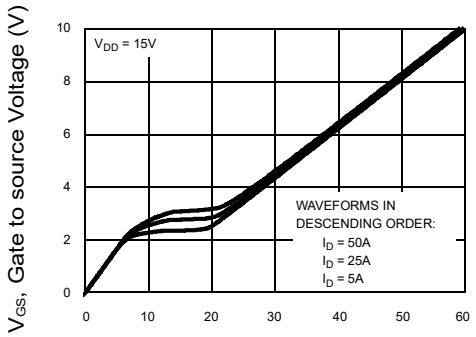


Figure 12: Gate Charge Waveforms for Constant Gate Currents

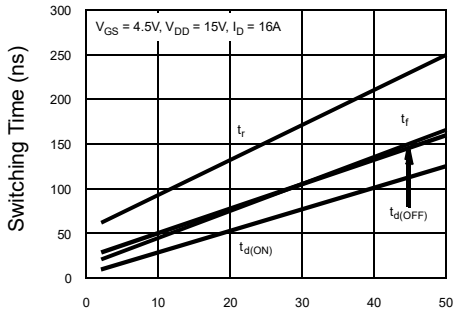


Figure 13: Switching Time vs Gate Resistance

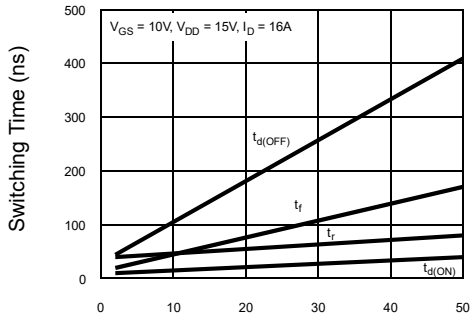
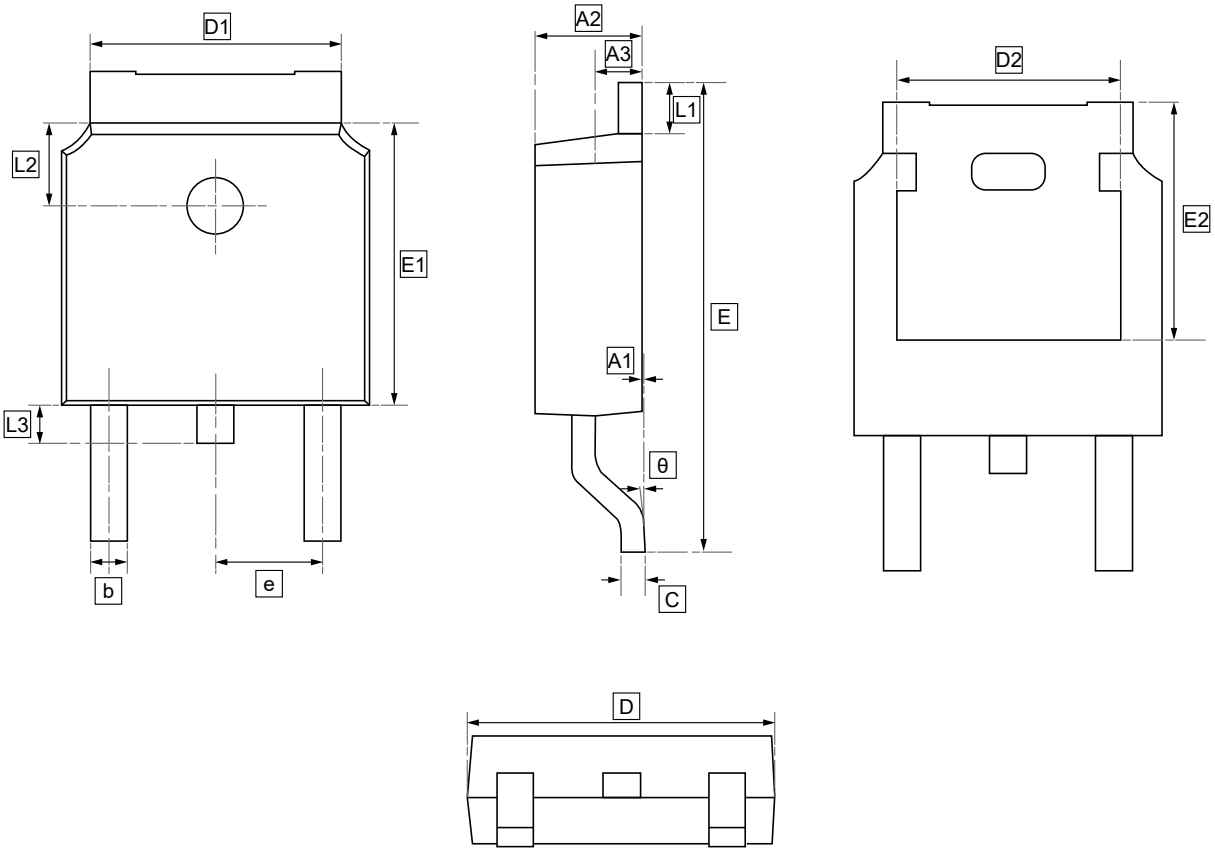


Figure 14: Switching Time vs Gate Resistance

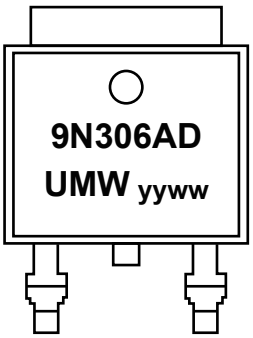
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW ISL9N306AD3ST	TO-252	2500	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.