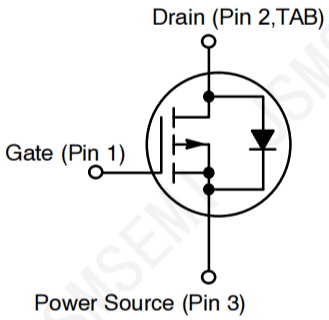
DESCRIPTION

The PMV65XPEAR-JSM is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

ESD Protected : 3KV



FEATURE

- -20V/-4.3A, $R_{DS(ON)}$=34mΩ(typ.)@V_{GS}=-4.5V
- -20V/-3.0A,$R_{DS(ON)}$=44mΩ(typ.)@V_{GS}=-2.5V
- -20V/-2.0A,$R_{DS(ON)}$=56mΩ(typ.)@V_{GS}=-1.8V
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOT23-3Lpackage design

APPLICATIONS

- Power Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

ABSOLUTE MAXIMUM RATINGS (T_A= 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±10	V
I_D	Continuous Drain Current (T_C=25℃)	V_{GS}=-4.5V	-4.3	A
	Continuous Drain Current (T_C=70℃)		-3.0	A
I_{DM}	Pulsed Drain Current		-20	A
P_D	Power Dissipation	T_A=25℃	1.5	W
		T_A=70℃	0.9	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		120	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress rating only and functional device operation is not implied

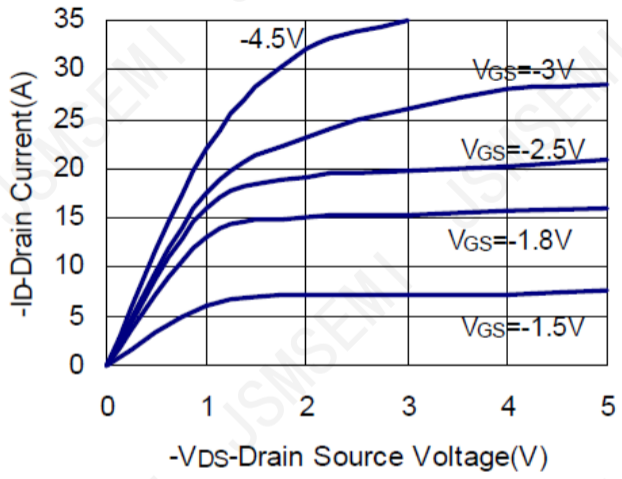
ELECTRICALCHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.6		-1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±10 V			±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0			-1	uA
		V_{DS}=-20V, V_{GS}=0 T_J=55℃			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-4.3A		34	44	mΩ
		V_{GS}=-2.5V, I_D=-3.0A		44	52	
		V_{GS}=-1.8V, I_D=-2.0A		56	75	
		V_{GS}=-1.5V, I_D=-1.0A		85	110	
Gfs	Forward Transconductance	V_{DS}=-5V, I_D=-4.0A		22		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.67	-1.2	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-10V V_{GS}=-4.5V I_D=-4.0A		11.1		nC
Q_{gs}	Gate-Source Charge			3.1		
Q_{gd}	Gate-Drain Charge			2.4		
C_{iss}	Input Capacitance	V_{DS}=-10V V_{GS}=0V f=1MHz		989		pF
C_{oss}	Output Capacitance			167		
C_{rss}	Reverse Transfer Capacitance			75.5		
$T_{d(on)}$	Turn-On Time	V_{DS}=-10V I_D=-3.7A V_{GEN}=-4. 5VR_G=1Ω		712		nS
T_r				1386		
$T_{d(off)}$	Turn-Off Time			9.1		
T_f				4		

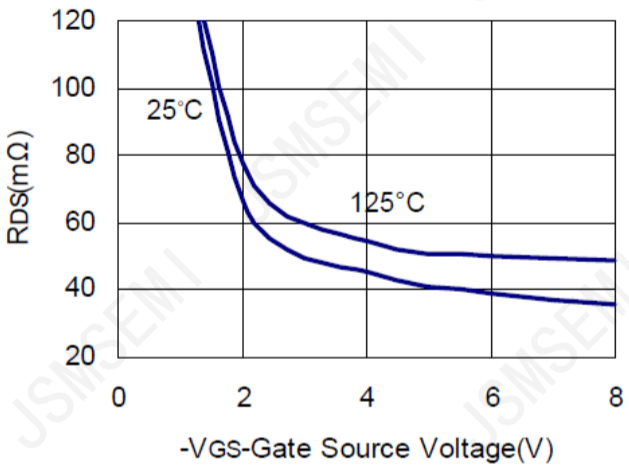
Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%
2.Static parameters are based on package level with recommendedwire bonding

TYPICAL CHARACTERISTICS (25℃ Unless Note)

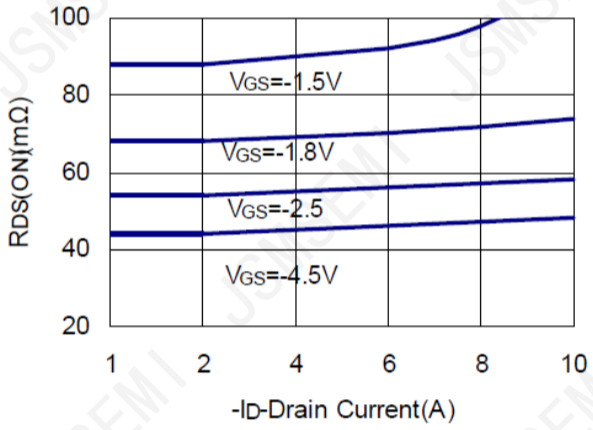
Output Characteristics



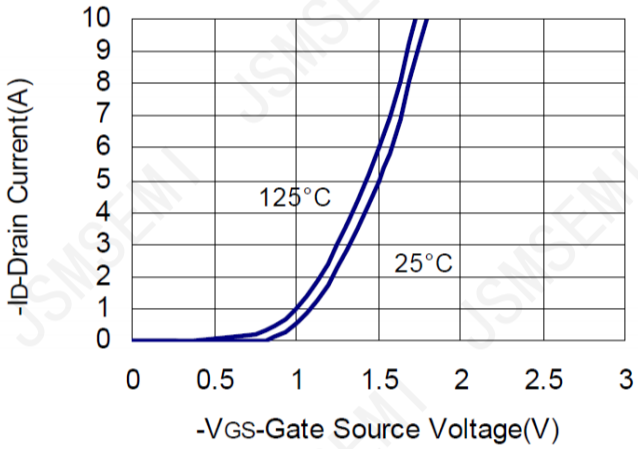
Drain-Source On Resistance



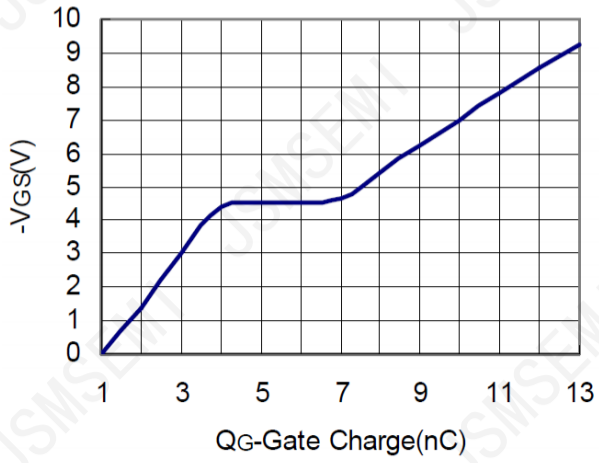
Drain Source On Resistance



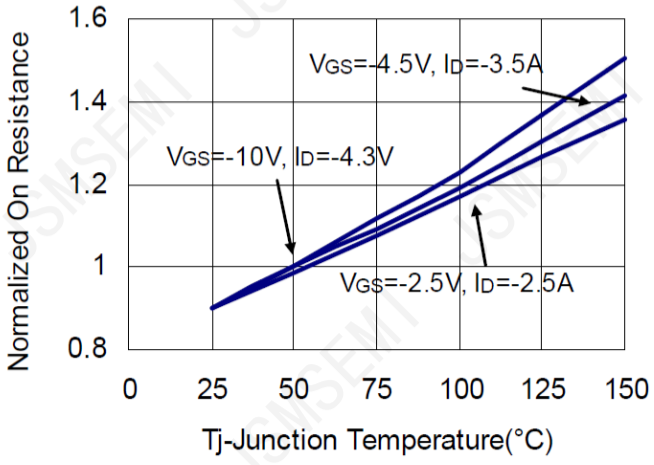
Transfer Characteristics



Gate Charge

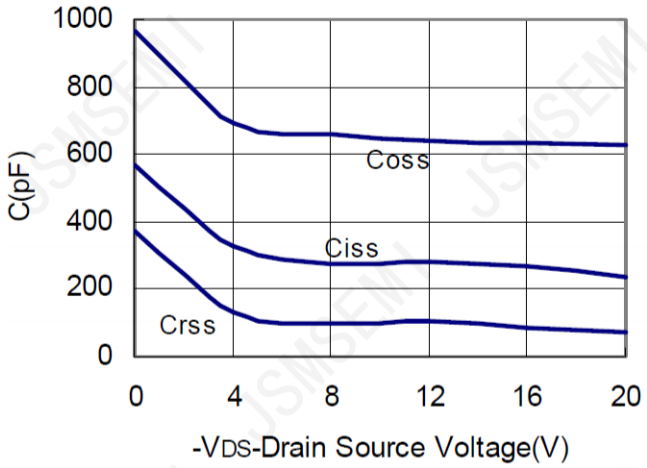


Drain Source Resistance

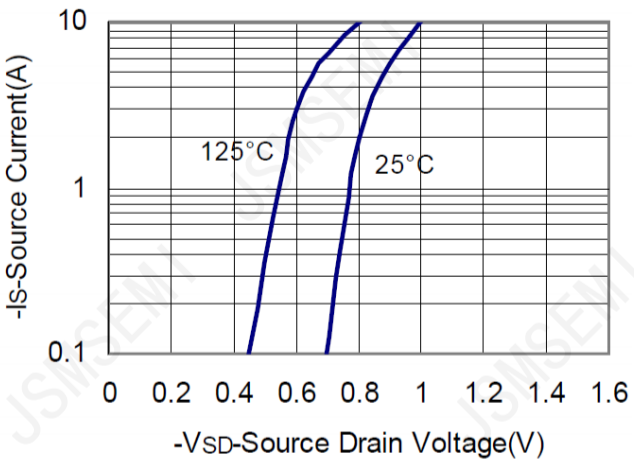


TYPICAL CHARACTERISTICS (continuous)

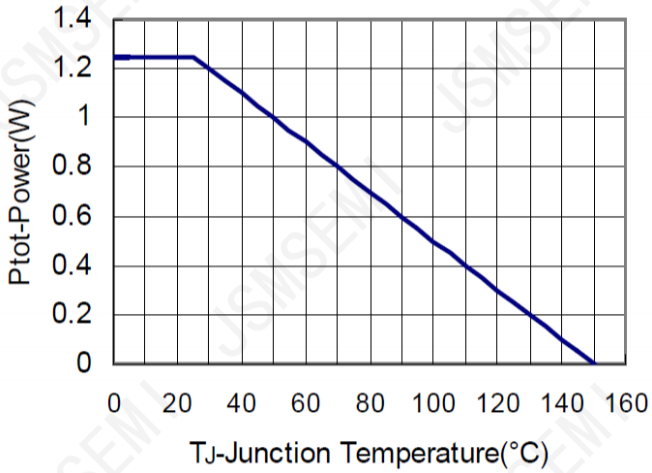
Capacitance



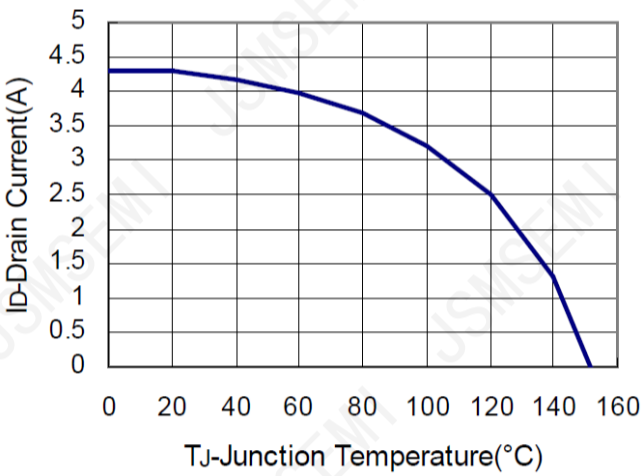
Source Drain Diode Forward



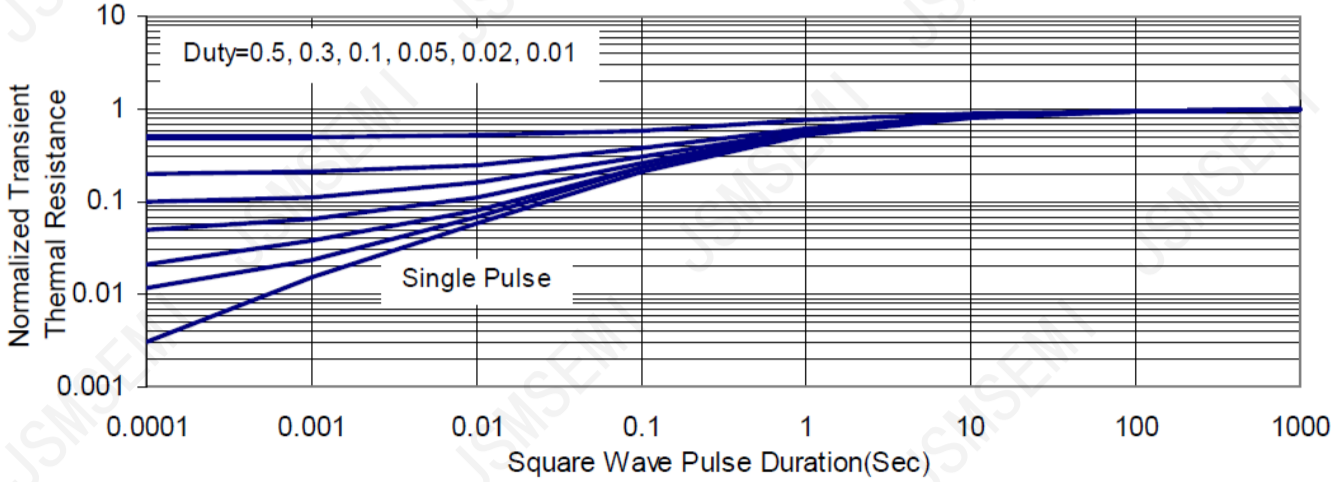
Power Dissipation



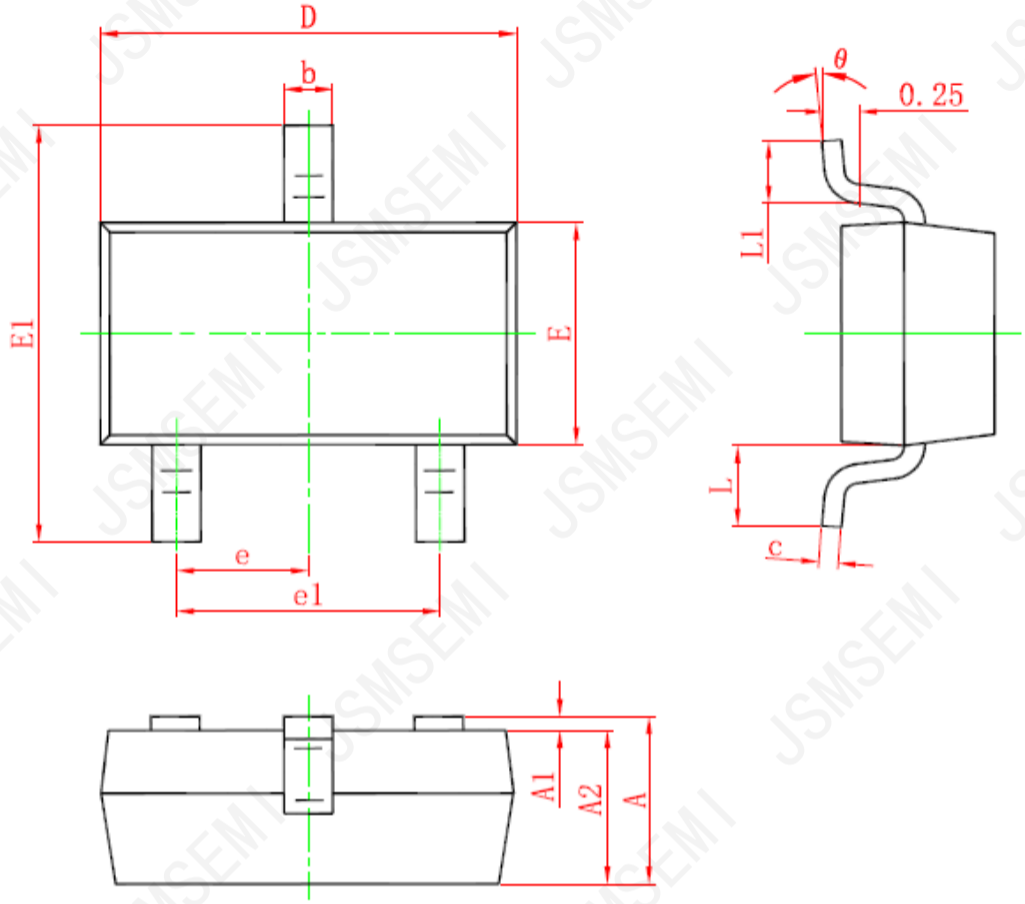
Drain Current



Thermal Transient Impedance



SOT23 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	2/23/2024

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