UMW FDS8878

30V N-Channel MOSFET

1.Features

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

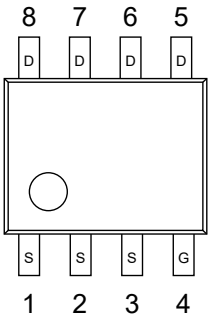
2.Features

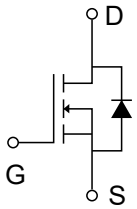
- $V_{DS\ (V)}$=30V
- I_D=10.2A
- $R_{DS(ON)}$<14mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<17 mΩ(V_{GS}=4.5V)

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GS}	±20	
Drain Current Continuous (T_A=25°C, V_{GS}=10V, $R_{\theta JA}$=50°C/W)	I_D	10.2	A
Continuous (T_A=25°C, V_{GS}=4.5V, $R_{\theta JA}$=50°C/W)		9.3	
Pulsed		80	
Single Pulse Avalanche Energy (Note 1)	E_{AS}	57	mJ
Power Dissipation	P_D	2.5	W
Derate above 25°C		20	mW/°C
Operating and Storage Temperature	T_J,T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Case (Note 2)	$R_{\theta JC}$	25	°C/W
Thermal Resistance, Junction to Ambient (Note 2a)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction to Ambient (Note 2b)	$R_{\theta JA}$	125	°C/W

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
		T_J=150°C			250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2		2.5	V
Drain to Source On Resistance	$R_{DS(ON)}$	I_D=10.2A, V_{GS}=10V		11	14	mΩ
		I_D=9.3A, V_{GS}=4.5V		13.8	17	mΩ
		I_D=10.2A, V_{GS}=10V, T_C=150°C		17.5	22.7	mΩ
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		897		pF
Output Capacitance	C_{oss}			190		pF
Reverse Transfer Capacitance	C_{rss}			111		pF
Gate Resistance	R_g	V_{GS}=0.5V, f=1MHz	0.7	2.9	5	Ω
Total Gate Charge at 10V	$Q_{g(TOT)}$	V_{GS}=0V to 10V; V_{DD}=15V		17	26	nC
Total Gate Charge at 5V	$Q_{g(5)}$	V_{GS}=0V to 5V; I_D=10.2A		9	14	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS}=0V to 1V; I_g=1mA		0.9	1.4	nC
Gate to Source Gate Charge	Q_{gs}			2.5		nC
Gate Charge Threshold to Plateau	Q_{gs2}			1.7		nC
Gate to Drain “Miller” Charge	Q_{gd}			3.3		nC
Turn-On Time	t_{on}	V_{DD}=50V, I_D=10.2A, V_{GS}=10V, R_{GS}=16Ω			54	ns
Turn-On Delay Time	$t_{D(on)}$			7		ns
Rise Time	t_r			29		ns
Turn-Off Delay Time	$t_{D(off)}$			45		ns
Fall Time	t_f			18		ns
Turn-Off Time	t_{off}				94	ns

Source to Drain Diode Voltage	V_{SD}	I_{SD}=10.2A			1.25	V
		I_{SD}=2.1A			1	V
Reverse Recovery Time	t_{rr}	I_{SD}=10.2A, dI_{SD}/dt=100A/μs			19	ns
Reverse Recovered Charge	Q_{rr}	I_{SD}=10.2A, dI_{SD}/dt=100A/μs			9.5	nC

Notes:

1: Starting T_J=25°C, L=1mH, I_{AS}=10.7A, V_{DD}=30V, V_{GS}=10V.

2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad.

7.1Typical Characteristics

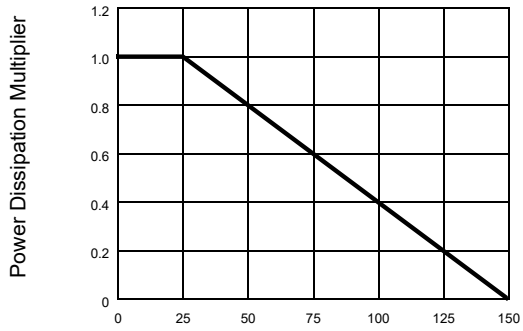


Figure 1: Normalized Power Dissipation vs Ambient Temperature

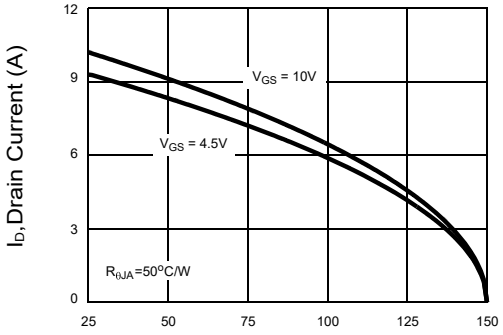


Figure 2: Maximum Continuous Drain Current vs Ambient Temperature

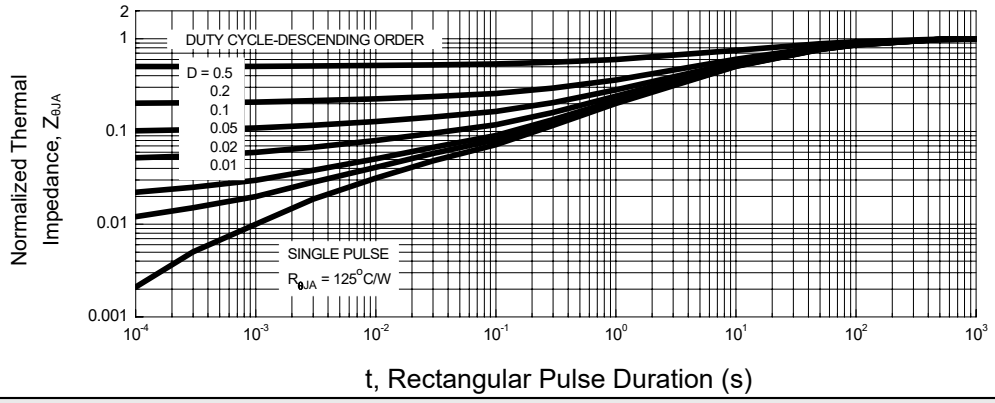


Figure 3: Normalized Maximum Transient Thermal Impedance

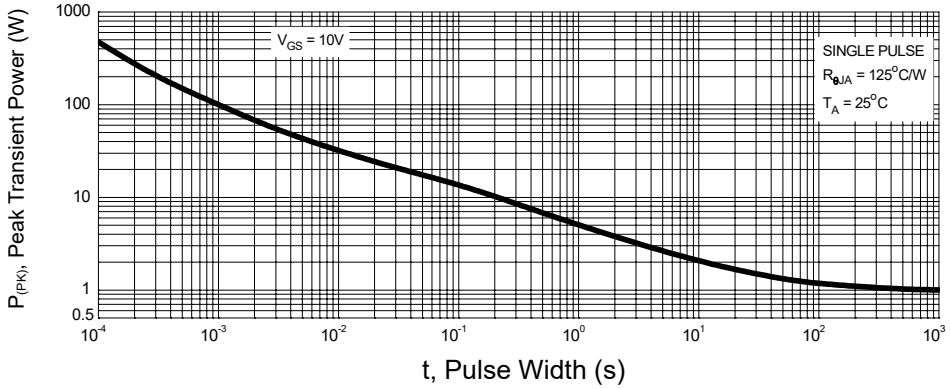
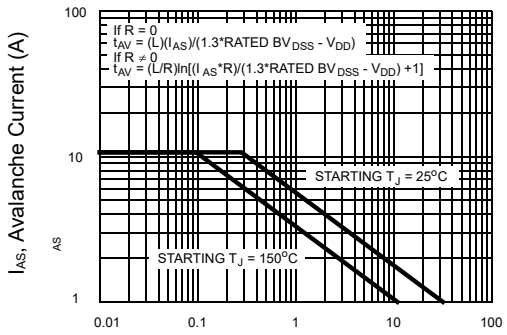


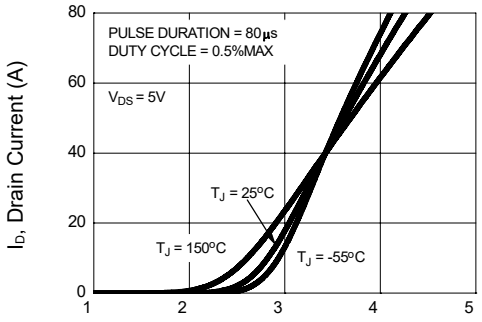
Figure 4: Single Pulse Maximum Power Dissipation

7.2Typical Characteristics



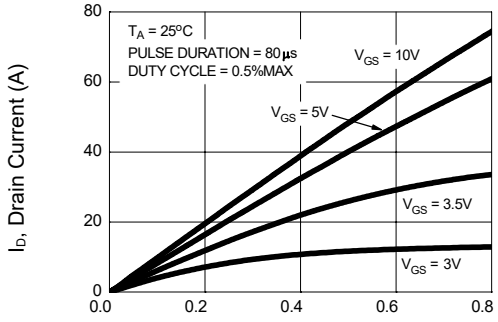
t_{AV}, Time In Avalanche(ms)

Figure 5: Unclamped Inductive Switching Capability



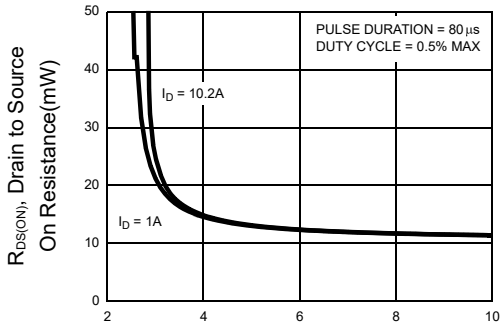
V_{DS},Drain to Source Voltage (V)

Figure 6: Transfer Characteristics



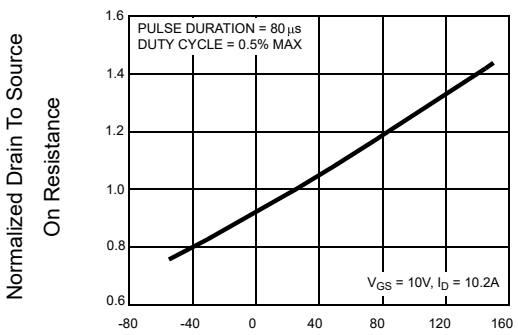
V_{DS},Drain to Source Voltage (V)

Figure 7: Saturation Characteristics



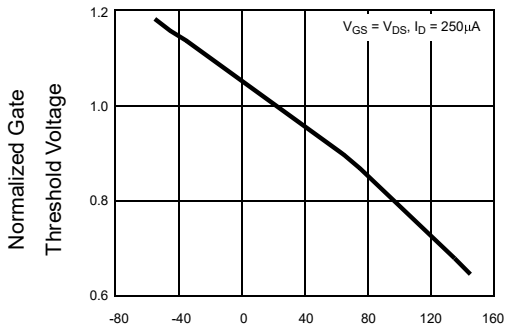
V_{GS},Gate to Source Voltage (V)

Figure 8: Drain to Source On Resistance vs Gate Voltage and Drain Current



T_J,Junction Temperature (°C)

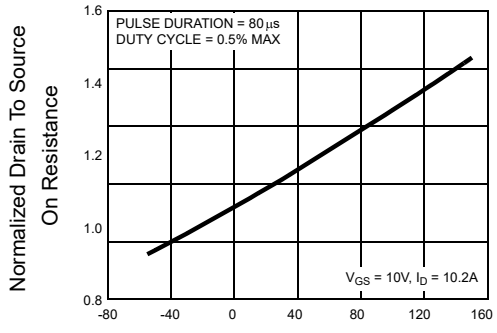
Figure 9: Normalized Drain to Source On Resistance vs Junction Temperature



T_J,Junction Temperature (°C)

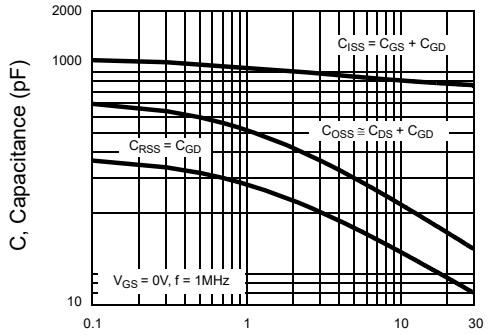
Figure 10: Normalized Gate Threshold Voltage vs Junction Temperature

7.3Typical Characteristics



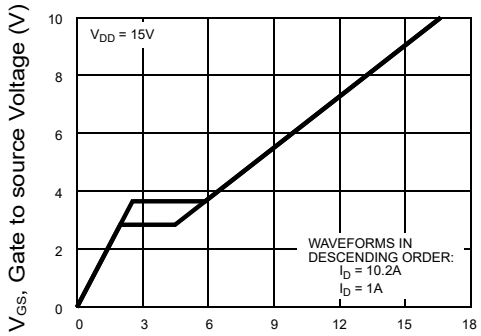
T_J,Junction Temperature (°C)

Figure 11: Normalized Drain to Source Breakdown Voltage vs Junction Temperature



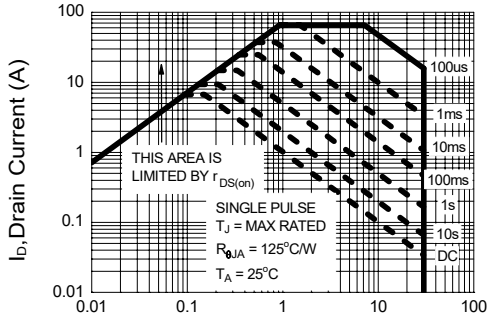
V_{DS},Drain to Source Voltage (V)

Figure 12: Capacitance vs Drain to Source Voltage



Q_G,Gate Charge (nC)

Figure 13: Gate Charge Waveforms for Constant Gate Currents



V_{DS},Drain to Source Voltage (V)

Figure 14: Forward Bias Safe Operating Area

7.4Typical Characteristics

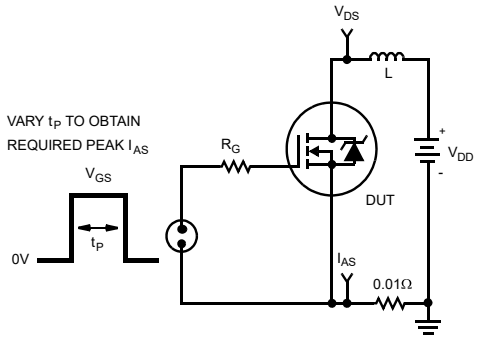


Figure 12: Unclamped Energy Test Circuit

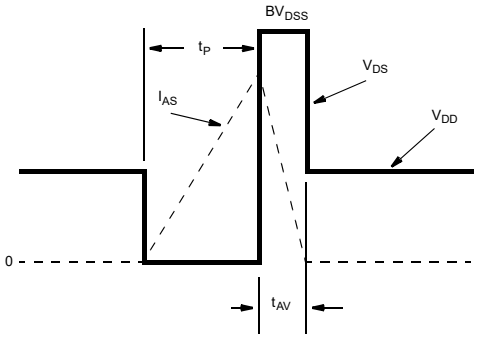


Figure 12: Unclamped Energy Waveforms

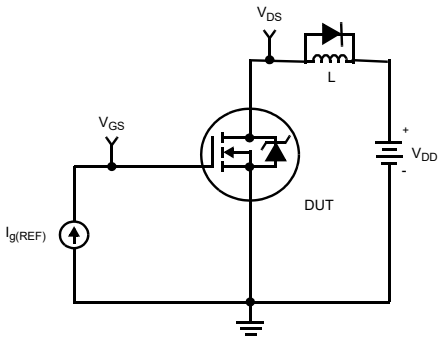


Figure 12: Gate Charge Test Circuit

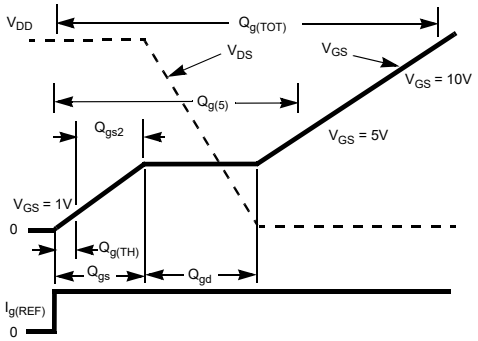


Figure 12: Gate Charge Waveforms

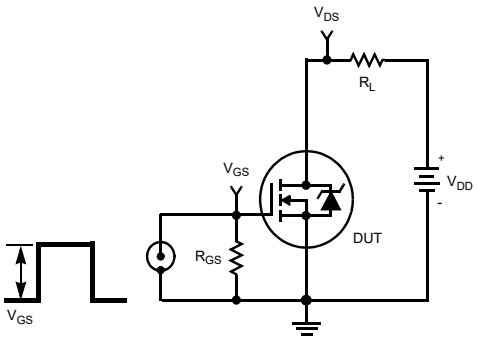


Figure 12: Switching Time Test Circuit

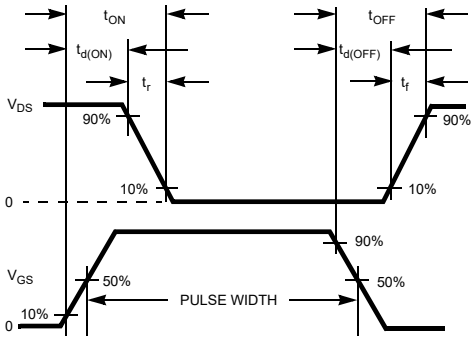
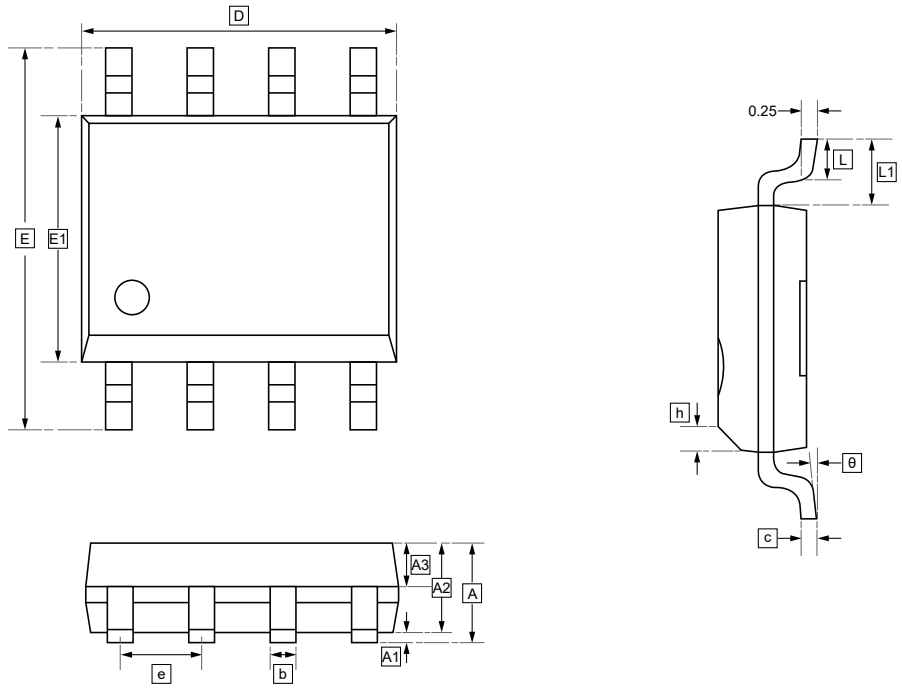


Figure 12: Switching Time Waveforms

8.SOP-8 Package Outline Dimensions

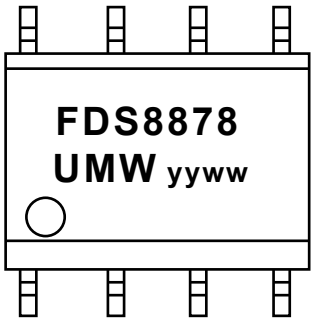


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS8878	SOP-8	3000	Tape and reel

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