

1.Description

The ESD7504 surge protection is designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

3.Features

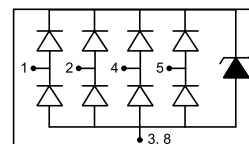
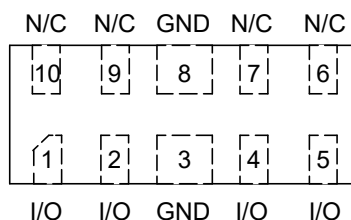
- Low Capacitance (0.55 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
- IEC 61000-4-2 (Level 4)

2.Applications

- USB 3.0
- eSATA 1.0/2.0/3.0
- HDMI 1.3/1.4
- Display Port

- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

4.Pinning information



DFN2510

5.Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Junction Temperature Range	T_J	-55 to 125	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C
Lead Solder Temperature –Maximum (10 Seconds)	T_L	260	°C
IEC 61000-4-2 Contact (ESD)	V_{ESD}	±15	kV
IEC 61000-4-2 Air (ESD)		±15	kV

Notes: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



6. Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Reverse Working Voltage	V _{RWM}	I/O Pin to GND				3.3	V
Breakdown Voltage	V _{BR}	I _T =1mA, I/O Pin to GND		4	5		V
Reverse Leakage Current	I _R	V _{RWM} =3.3V, I/O Pin to GND				1	μA
Clamping Voltage (Note 1)	V _C	IEC61000-4-2, ±8 kV Contact		See Figures 1 and 2			V
Clamping Voltage	V _C	I _{PP} =8A	IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		10.2		V
TLP (Note 2)		I _{PP} =-8A			-4.5		V
See Figures 5 through 6		I _{PP} =16A	IEC 61000-4-2 Level 4 equivalent		13.7		V
		I _{PP} =-16A	(±8 kV Contact, ±15 kV Air)		-8.1		V
Junction Capacitance	C _J	V _R =0 V, f=1MHz between I/O Pins and GND				0.55	pF

Notes:

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted.

Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

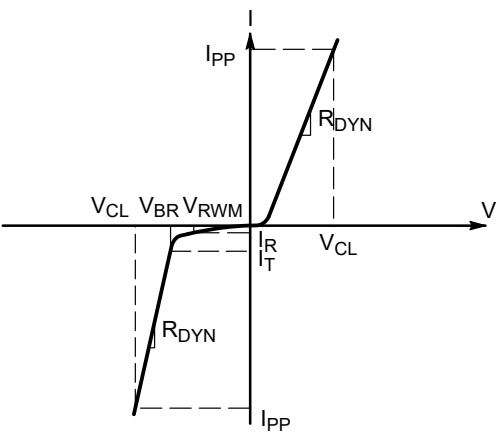
1. For test procedure see Figures 3 and 4

2. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 4\text{ ns}$, averaging window; $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$.



7.Electrical Parameters (T_A=25°C unless otherwise noted)

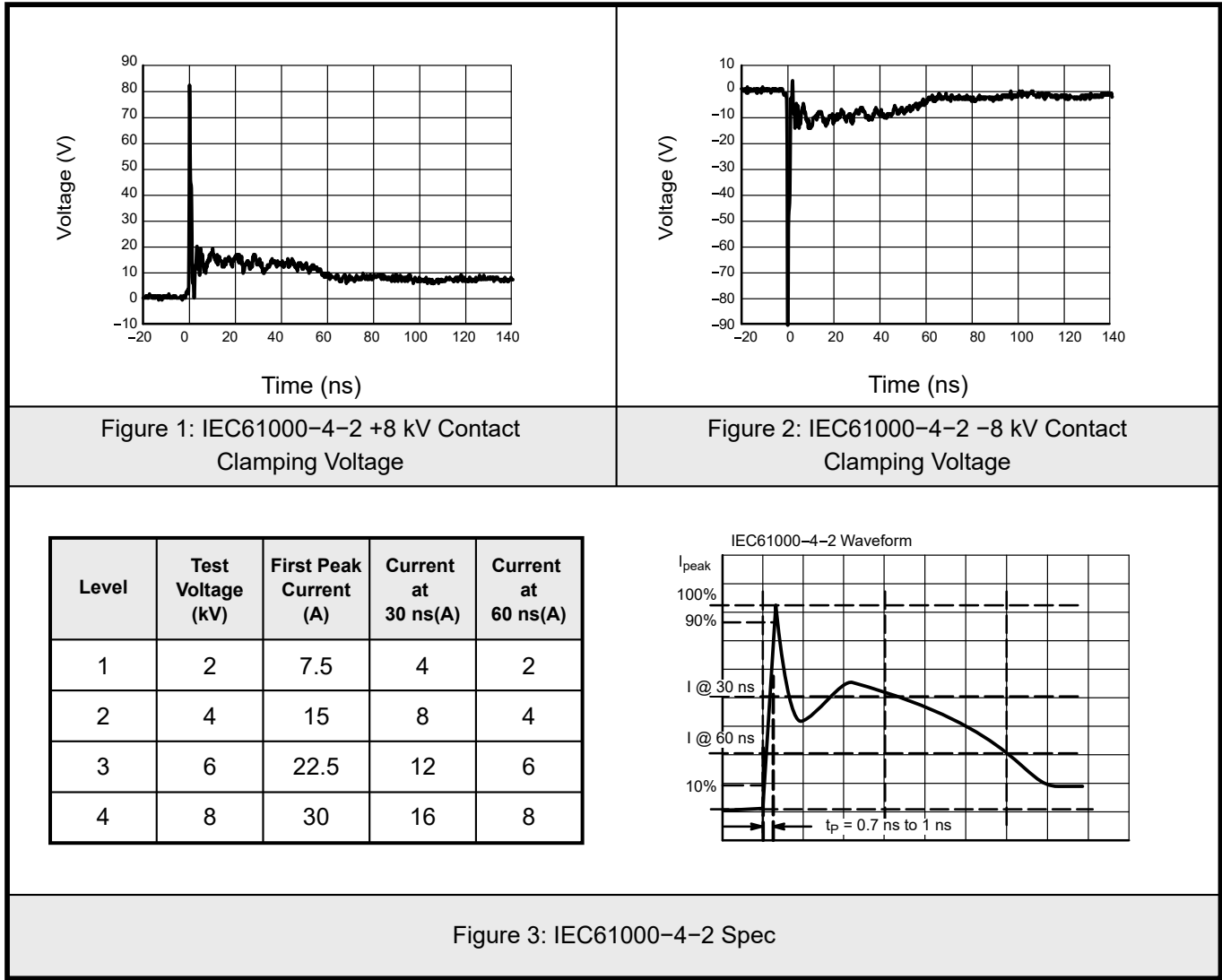


Uni-Directional

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
R_{DYN}	Dynamic Resistance



8.1Typical characteristic





8.2 Typical characteristic

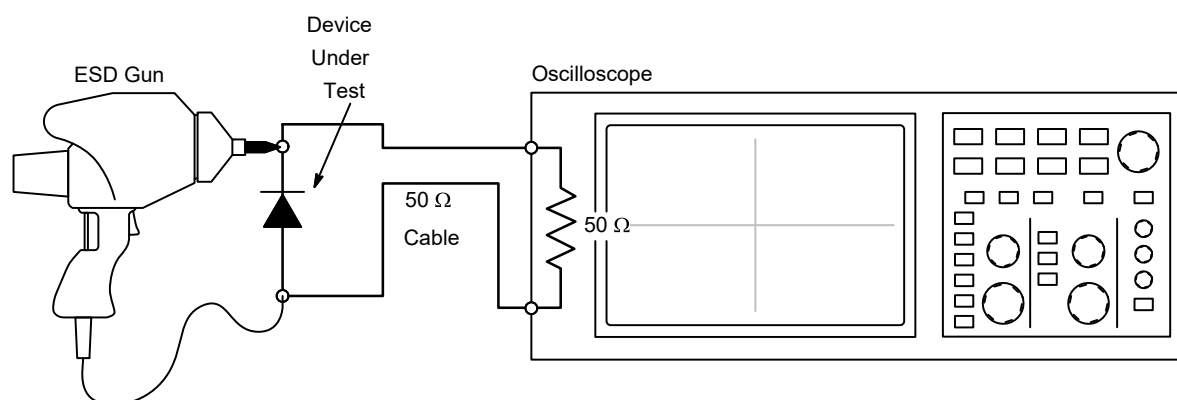


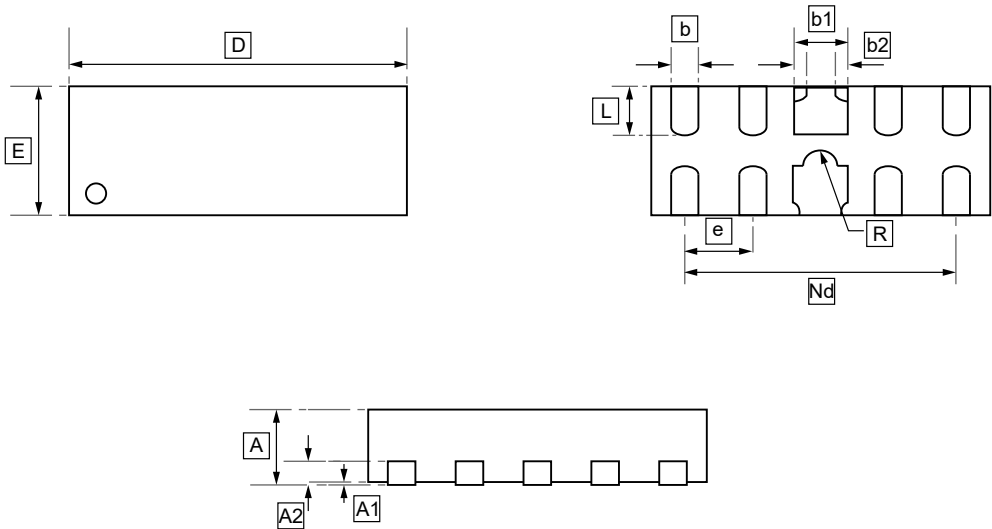
Figure 4. Diagram of ESD Clamping Voltage Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for largesystems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. That has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes.



9.DFN2510 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	D	E	b1	b2	b	L	Nd	e	R	A	A1	A2
Min	2.45	0.95	0.35	0.15	0.10	0.33	2.00	0.50	0.125	0.45	0.152	-
Max	2.55	1.05	0.45	0.25	0.20	0.43	BSC	BSC	BSC	0.55	REF	0.05



10.Ordering information



Order Code	Package	Base QTY	Delivery Mode
UMW ESD7504MUTAG	DFN2510	3000	Tape and reel



11.Disclaimer

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