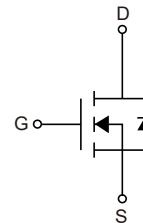
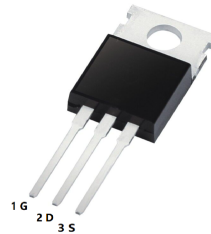


1.Features

- $V_{DS(V)}=40V$
- $I_D=120A$
- $R_{DS(ON)}<1.5m\Omega(V_{GS}=10V)$
- Optimized technology for DC / DC converters
- Fast switching MOSFET for SMPS
- N-channel normal level
- Very low on-resistance $R_{DS(ON)}$
- Excellent gate charge x $R_{DS(ON)}$ product (FOM)

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE



3.Absolute Maximum Ratings $T_C=25^\circ C$

Parameter	Symbol	Conditions	Rating	Units
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^\circ C$	120	A
		$V_{GS}=10V, T_C=100^\circ C$	120	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25^\circ C$	400	
Avalanche current, single pulse ³⁾	I_{AS}	$T_C=25^\circ C$	100	
Avalanche energy, single pulse	E_{AS}	$I_D=100A, R_{GS}=25\Omega$	865	mJ
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25^\circ C$	250	W
storage temperature	T_J, T_{STG}		-55 to 175	$^\circ C$
IEC climatic category; DIN IEC 68-1			55/175/56	

Notes:

- 1) J-STD20 and JESD22.
- 2) See figure 3 for more detailed information.
- 3) See figure 13 for more detailed information.



4. Electrical Characteristic (T_c=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal resistance, junction -case	R _{thJC}				0.6	K/W
SMD version, device on PCB	R _{thJA}	minimal footprint			62	K/W
		6 cm ² cooling area ⁴⁾			40	K/W
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =1mA	40			V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =200μA	2		4	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =40V, V _{GS} =0V, T _J =25°C		0.1	2	μA
		V _{DS} =40V, V _{GS} =0V, T _J =125°C		20	200	μA
Gate-source leakage current	I _{GSS}	V _{GS} =20V, V _{DS} =0V		10	100	nA
Drain-source on-state resistance ⁵⁾	R _{DS(ON)}	V _{GS} =10V, I _D =100A		1.2	1.5	mΩ
Gate resistance	R _G			1.5		Ω
Transconductance	g _{FS}	V _{DS} >2 I _D R _{DS(ON)max} , I _D =100 A	120	230		S
Input capacitance	C _{iss}	V _{GS} =0V, V _{DS} =20V, f=1MHz		15000	20000	pF
Output capacitance	C _{oss}			4000	5300	pF
Reverse transfer capacitance	C _{rss}			160		pF
Turn-on delay time	t _{D(on)}	V _{DD} =20V, V _{GS} =10V I _D =30A, R _G =1.6Ω		40		ns
Rise time	t _r			10		ns
Turn-off delay time	t _{D(off)}			64		ns
Fall time	t _f			13		ns
Gate to source charge	Q _{gs}	V _{DD} =20V, I _D =100A V _{GS} =0 to 10V		76		nC
Gate charge at threshold	Q _{g(th)}			46		nC
Gate to drain charge	Q _{gd}			23		nC
Switching charge	Q _{SW}			75		nC
Gate charge total	Q _g			188	250	nC
Gate plateau voltage	V _{plateau}			5		V



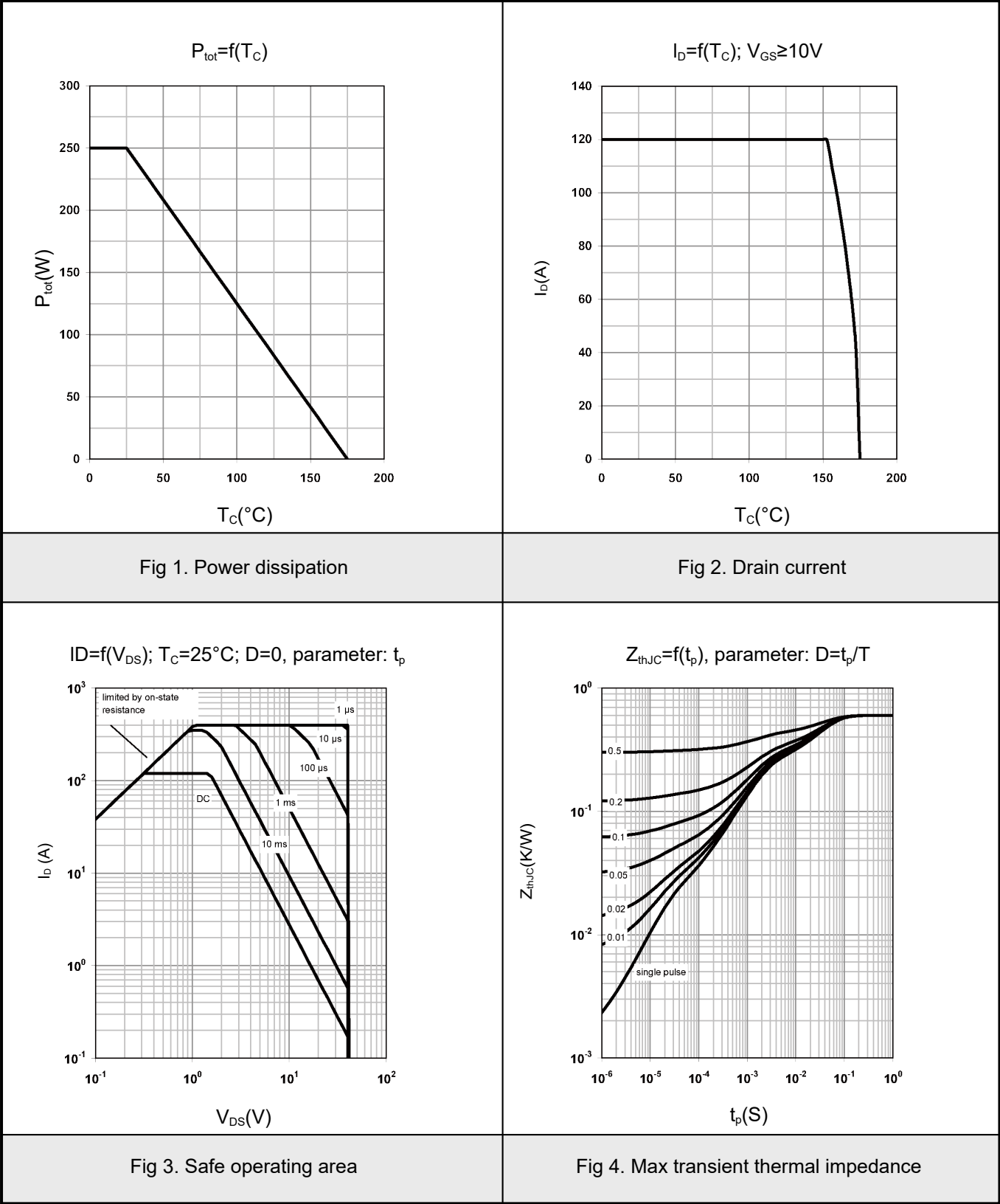
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1V, V_{GS}=0 \text{ to } 10V$		177		nC
Output charge	Q_{oss}	$V_{DD}=20V, V_{GS}=0V$		147		nC
Diode continuous forward current	I_S	$T_C=25^\circ C$			120	A
Diode pulse current	$I_{S,pulse}$				400	A
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=100A, T_J=25^\circ C$		0.88	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15V, I_F=I_S, di_F/dt=400A/\mu s$		141		nC

Notes:

- 4) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 um thick) copper area for drain connection. PCB is vertical in still air.
- 5) Measured from drain tab to source pin.
- 6) See figure 16 for gate charge parameter definition.

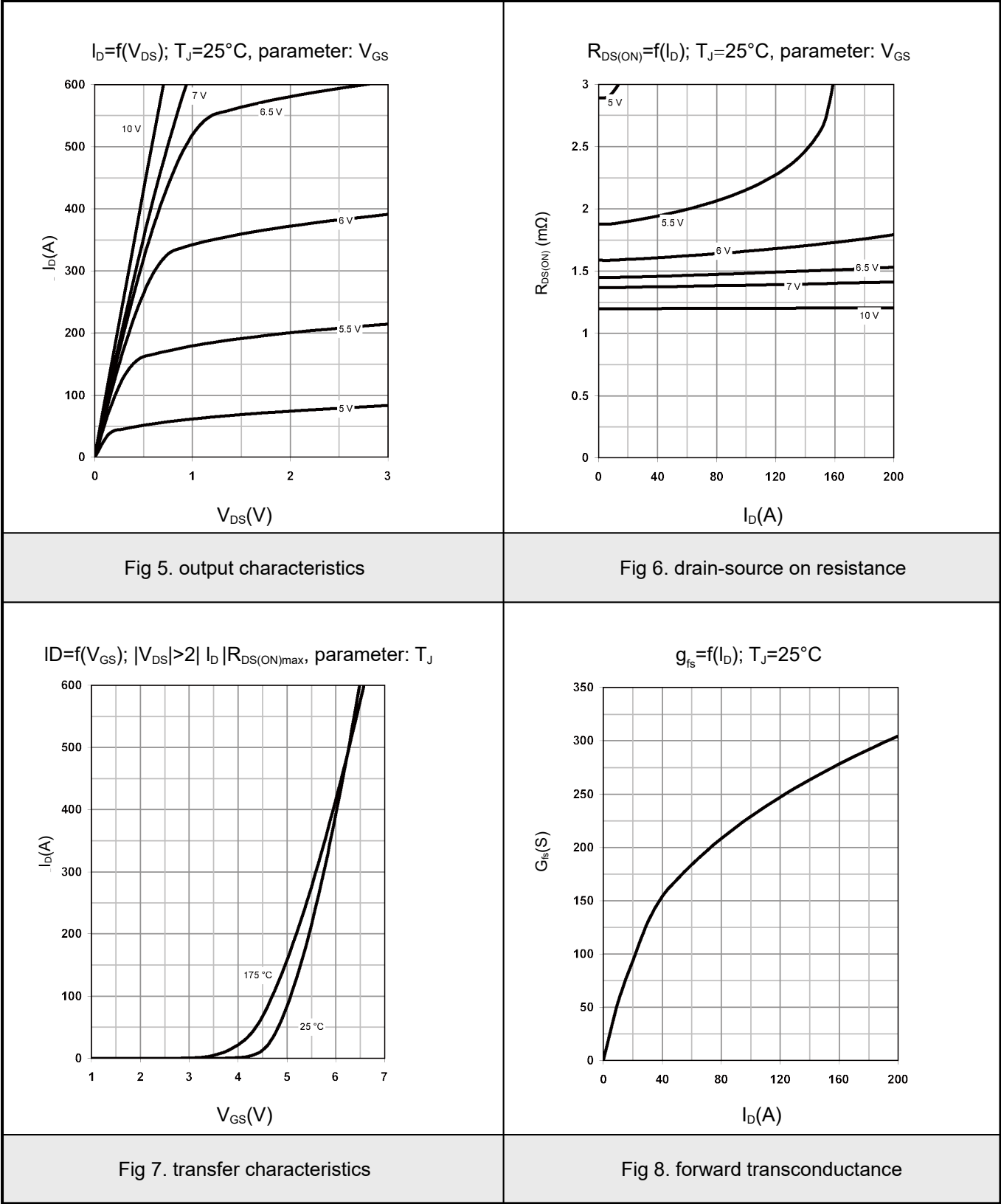


5.1Typical characteristic



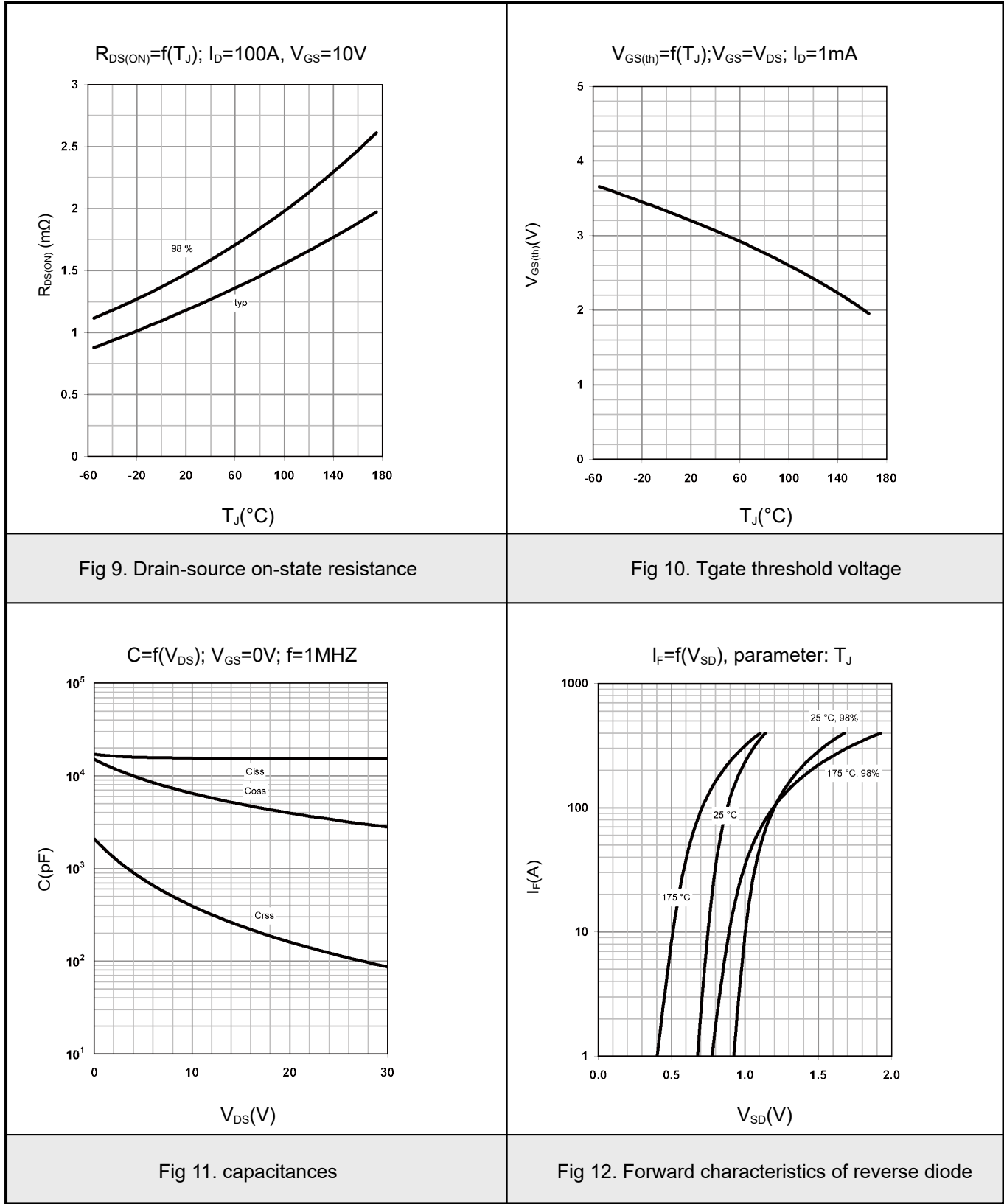


5.2Typical characteristic



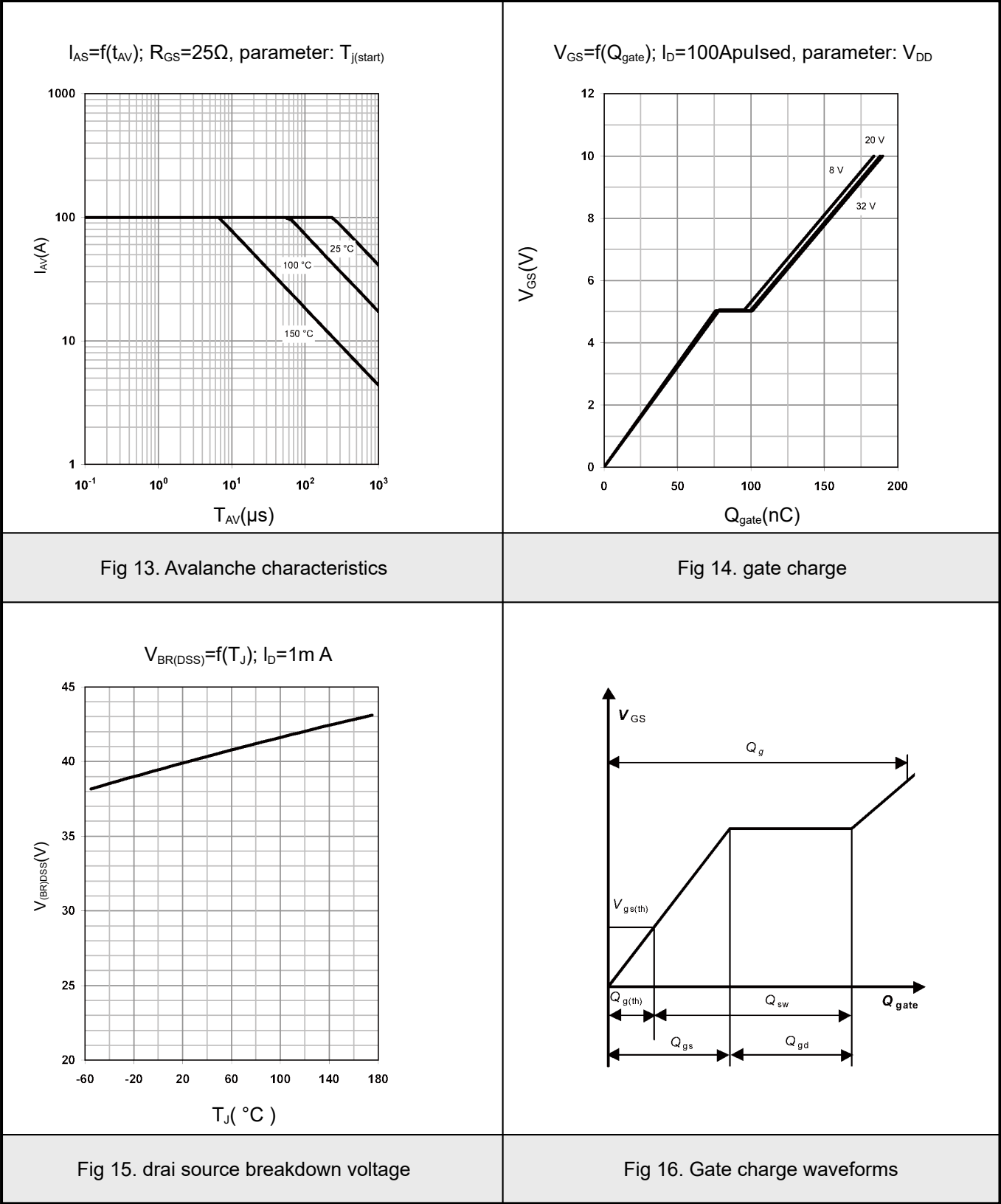


5.3Typical characteristic



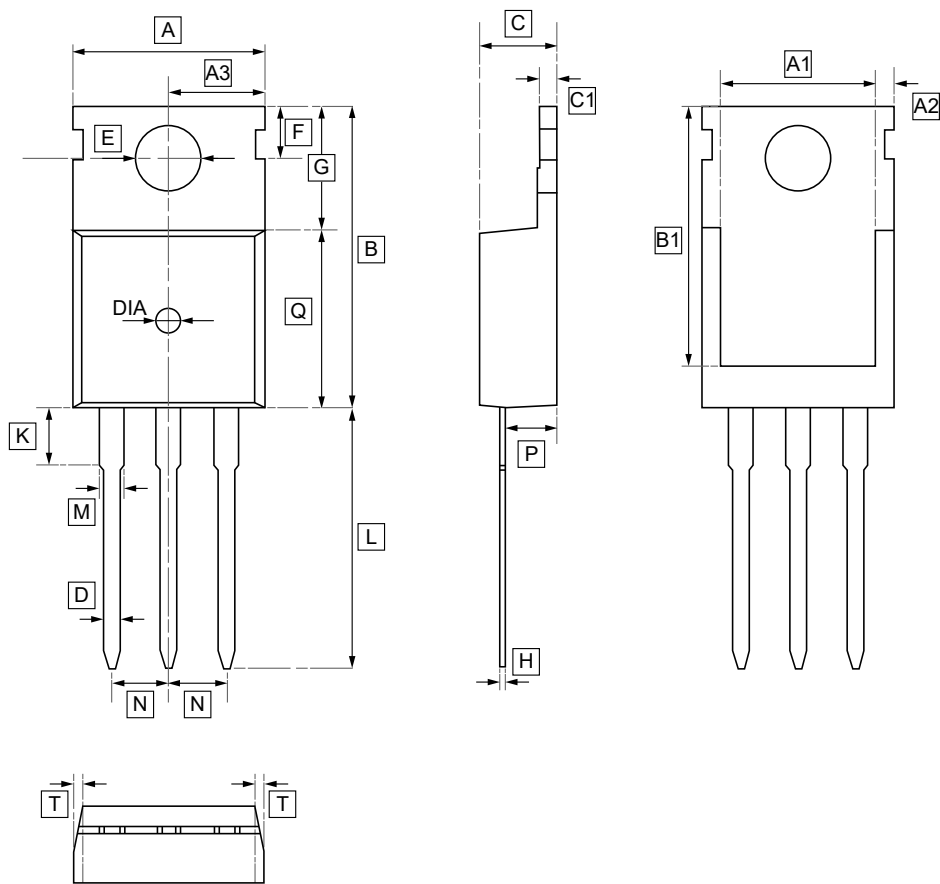


5.4Typical characteristic





6.TO-220 Package Outline Dimensions



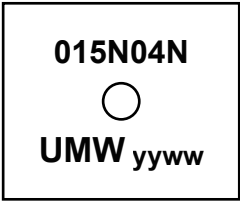
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	D	E	F	G
Min	9.7	8.44	1.05	4.8	15.4	12.9	4.28	1.1	0.6	3.4	2.65	5.2
Max	10.3	8.84	1.25	5.2	16.2	13.5	4.68	1.5	1.0	3.8	3.25	5.8

Symbol	H	K	L	L1	M	N	P	Q	T	DIA
Min	0.4	2.9	12.8	2.7	1.15	2.49	2.1	8.7	W:0.35	⌀1.5
Max	0.6	3.3	13.6	3.3	1.35	2.59	2.7	9.3		(deep 0.2)



7.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IPP015N04N G	TO-220	1000	Tube and box



8.Disclaimer

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