UMW IRS2003STR

250V Half Bridge MOSFET/IGBT Gate Driver

1.Description

The IRS2003S is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 250 V.

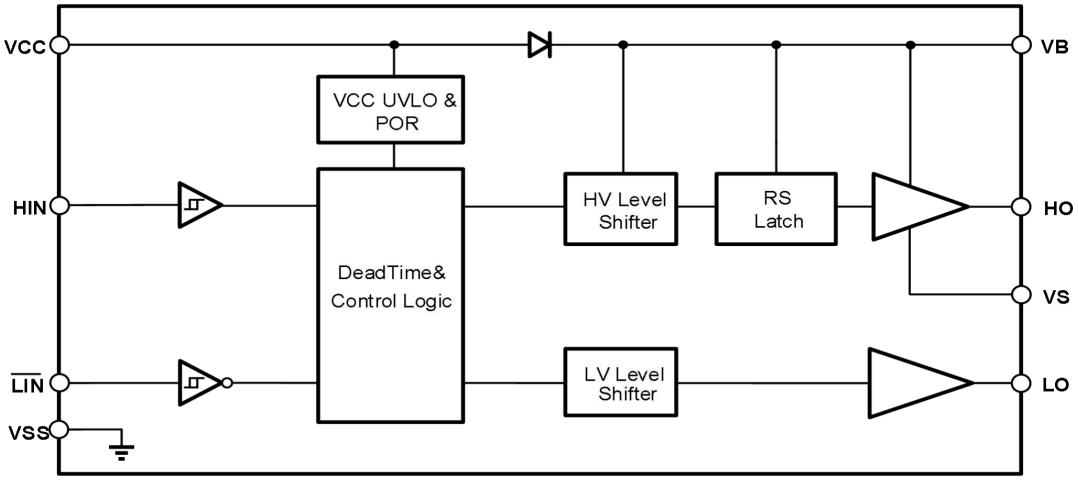
2.Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

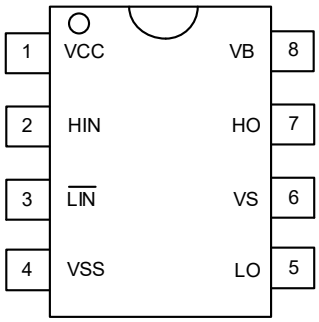
3.Features

- Floating channel designed for bootstrap operation
- Fully operational to +250 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Integrated Bootstrap diode
- Cross-conduction prevention logic
  --Deadtime 520ns
- Propagation delay
  --Ton/Toff =680ns/150ns
- Wide operating temperature range
  -40°C ~125°C
- Typically output Source/Sink current capability: 290mA/600mA

4.Functional Block Diagram



5.Pinning Information



SOP-8

Lead Definitions

Number	Symbol	Description
1	VCC	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase
4	VSS	Low side return
5	LO	Low side gate drive output
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

6.Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to V_{SS} and an ambient temperature of 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	V_B	-0.3	275	V
High side floating supply return	V_S	V_B-25	V_B+0.3	V
High side gate drive output	V_{HO}	V_S-0.3	V_B+0.3	V
Low side and main power supply	V_{CC}	-0.3	25 Note1	V
Low side gate drive output	V_{LO}	-0.3	V_{CC}+0.3	V
Logic input of HIN & $\overline{\text{LIN}}$	V_{IN}	-0.3	V_{CC}+0.3	V
Allowable Offset Supply Voltage Transient	dV_S/dt	-	50	V/ns

7.ESD Rating

Parameter	Symbol	Min	Max	Units
HBM Model	ESD	1500	-	V
Machine Model		500	-	V

8.Rated Power

Parameter	Symbol	Min	Max	Units
Package Power Dissipation @ T_A ≤25°C	PD1	-	625	mW

9.Thermal Information

Parameter	Symbol	Min	Max	Units
Thermal Resistance, Junction to Ambient	Rth_{JA}	-	200	°C/W
Junction Temperature	T_J	-	150	°C
Storage Temperature	T_S	-55	150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	-	300	°C

10.Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	V_B	V_S + 10	V_S + 20	V
High side floating supply return Note2	V_S	-9	250	V
High side gate drive output	V_{HO}	V_S	V_B	V
Low side and main power supply	V_{CC}	10	20	V
Low side gate drive output	V_{LO}	0	V_{CC}	V
Logic input of HIN & $\overline{LIN}$	V_{IN}	0	V_{CC}	V
Ambient temperature	T_A	-40	125	°C

Note1: All power supplies tested at 25V.

Note2: Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design.

11.Dynamical Electrical Characteristics

Valid for temperature range at T_A=25°C, V_{CC}=V_B=15V, C_L=1nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Turn-on propagation delay	t_{ON}	V_S=0V		680	740	ns
Turn-off propagation delay	t_{OFF}	V_S=250V		150	220	ns
Turn-on rise time	t_R	V_S=0V		70	170	ns
Turn-off fall time	t_F	V_S=0V		30	90	ns
Deadtime	DT		400	520	650	ns
Matching delay ON and OFF	MT				30	ns

12.Static Electrical Characteristics

Valid for temperature range at T_A=25°C, V_{CC}=V_B=15V, C_L=1nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{CC} supply UVLO threshold	V_{CCUV+}		8	8.9	9.8	V
	V_{CCUV-}		7.4	8.2	9	V
High-side floating supply leakage current	I_{LK}	V_B=V_S=250V			50	μA
Quiescent V_B supply current	I_{QBS}	V_{IN}=0V or 5V		50	75	μA
Quiescent V_{CC} supply current	I_{QCC}	V_{IN}=0V or 5V		120	250	μA
Logic “1”(HIN&$\overline{\text{LIN}}$) input voltage	V_{IH}	V_{CC}=10V to 20V	2.5			V
Logic “0”(HIN&$\overline{\text{LIN}}$) input voltage	V_{IL}	V_{CC}=10V to 20V			0.8	V
High level output voltage, V_{BIAS} -V_O	V_{OH}	I_O=2mA		0.05	0.2	V
Low level output voltage, V_O	V_{OL}	I_O=2mA		0.02	0.1	V
Logic “1” input bias current	I_{IN+}	HIN=5V, $\overline{\text{LIN}}$=0V		10	20	μA
Logic “0”input bias current	I_{IN-}	HIN=0V, $\overline{\text{LIN}}$=5V			5	μA
Output high short circuit pulsed current	I_{O+}	V_O=0V, PW≤10us	200	290		mA
Output low short circuit pulsed current	I_{O-}	V_O=15V, PW≤10us	420	600		mA
Bootstrap diode conduction resistance	R_{BSD}	I_{BSD}=1mA		200		Ω
Bootstrap diode conduction voltage drop	V_{BSD}	I_{BSD}=1mA		0.6		V

13.Function Description

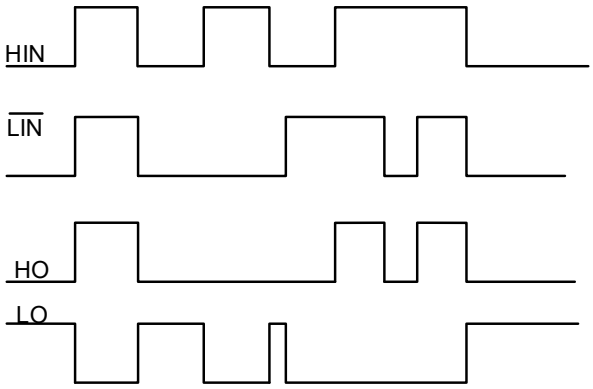


Figure 1. UMW IRS2003STR Input and output timing waveform

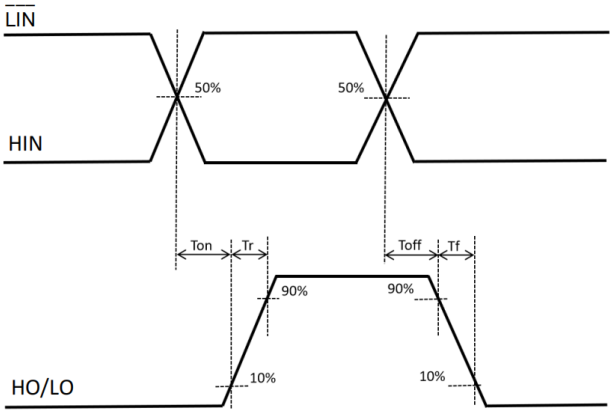


Figure 2. Propagation Time Waveform Definition

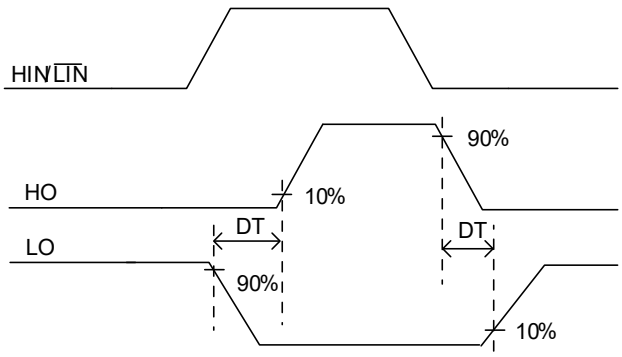


Figure3. Cross Conduction Prevention Delay Time Waveform Definition

14.Function Block Diagram

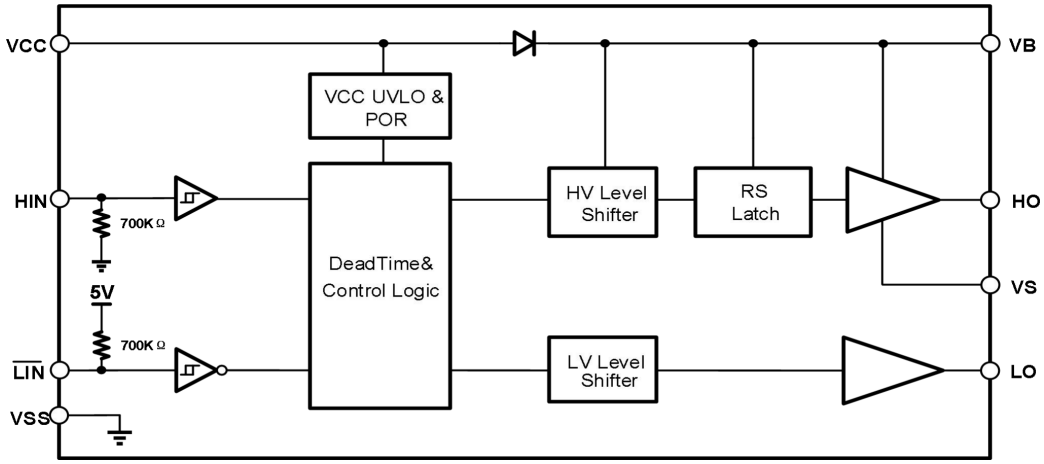


Figure 4. Function Block Diagram of UMW IRS2003STR

15.Application Message

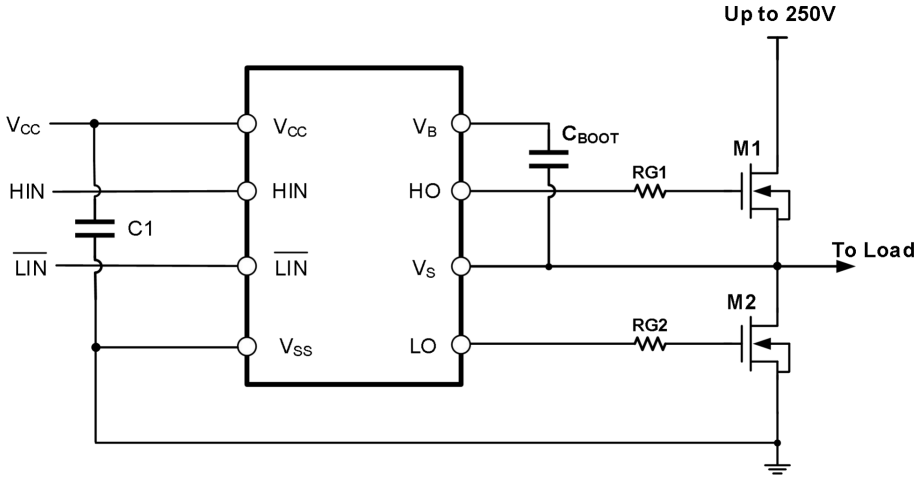
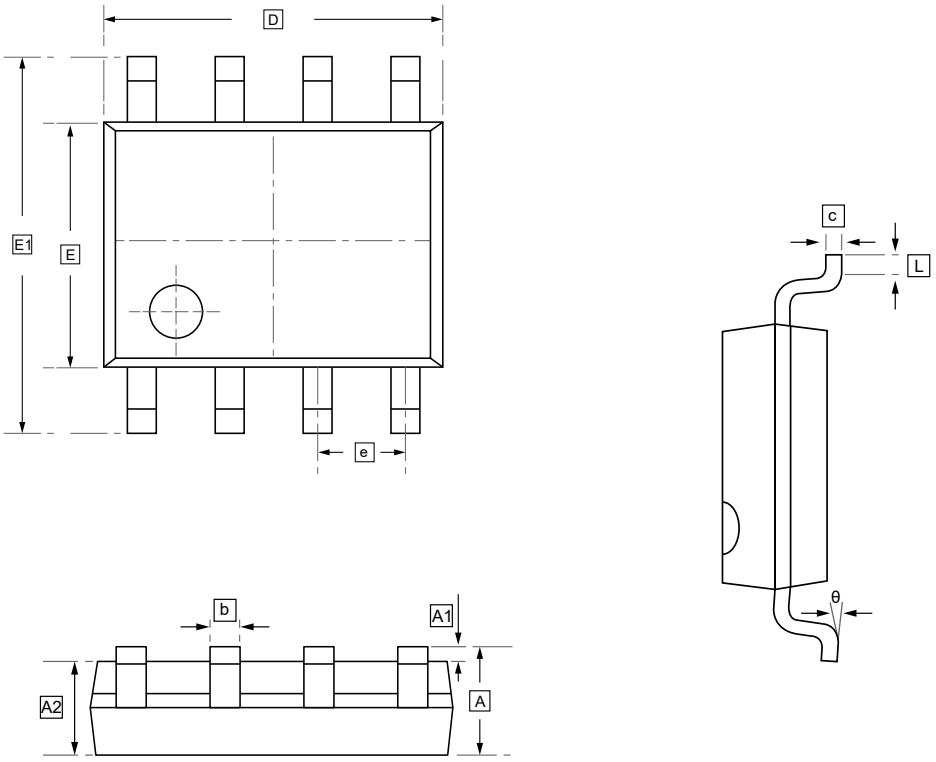


Figure 5. Typical application circuit of UMW IRS2003STR

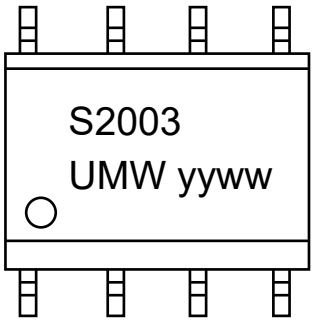
16.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

17.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IR2003STR	SOP-8	2500	Tape and reel

18.Disclaimer

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