UMW FDS6912A

Dual 30V N-Channel MOSFET

1.Description

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

2.1Features

- $V_{DS\ (V)}$=30V
- I_D=6A
- $R_{DS(ON)}$<28mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<35mΩ(V_{GS}=4.5V)

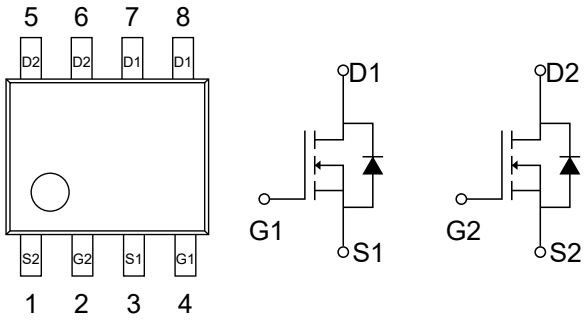
2.2Features

- High power and current handling capability
- High performance trench technology for extremely low $R_{DS(ON)}$
- Fast switching speed
- Low gate charge

3.Pinning information

Pin	Symbol	Description
2,4	G2,G1	GATE
1,3	S2,S1	SOURCE
5,6,7,8	D2,D1	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current – Continuous		I_D	6	A
– Pulsed	(Note 1a)		20	
Power Dissipation for Single Operation	(Note 1a)	P_D	1.6	W
	(Note 1b)		1	
	(Note 1c)		0.9	
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	78	°C/W
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	40	°C/W

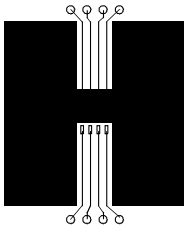
6.Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
		V_{DS}=24V, V_{GS}=0V, T_J=55°C			10	μA
Gate–Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.9	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-4.5		mV/°C
Static Drain–Source On–Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A		19	28	mΩ
		V_{GS}=4.5V, I_D=5A		24	35	mΩ
On–State Drain Current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	20			A
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=6A		25		S
Input Capacitance	C_{iss}	V_{DS}=15V V_{GS}=0V f =1MHz		575		pF
Output Capacitance	C_{oss}			145		pF
Reverse Transfer Capacitance	C_{rss}			65		pF
Gate Resistance	R_G	V_{GS}=15mV, f =1MHz		2.1		Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=15V, I_D=1A V_{GS}=10V, R_{GEN}=6Ω		8	16	ns
Turn-On Rise Time	t_r			5	10	ns
Turn-Off DelayTime	$t_{D(off)}$			23	37	ns
Turn-Off Fall Time	t_f			3	6	ns
Total Gate Charge	Q_g	V_{DS}=15V, I_D=6A V_{GS}=5V		5.8	8.1	nC
Gate–Source Charge	Q_{gs}			1.7		nC
Gate–Drain Charge	Q_{gd}			2.1		nC
Maximum Continuous Drain–Source Diode Forward Current	I_S				1.3	A

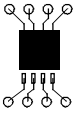
Drain–Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=1.3A (Note 2)		0.75	1.2	V
Diode Reverse Recovery Time	T_{rr}	I_F=6A, d_{IF}/d_t=100A/μs		20		nS
Diode Reverse Recovery Charge	Q_{rr}			10		nC

Notes:

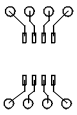
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78° C/W when mounted on a 0.5 in ^{2} pad of 2 oz. copper.



b) 125° C/W when mounted on a 0.02 in ^{2} pad of 2 oz. copper.

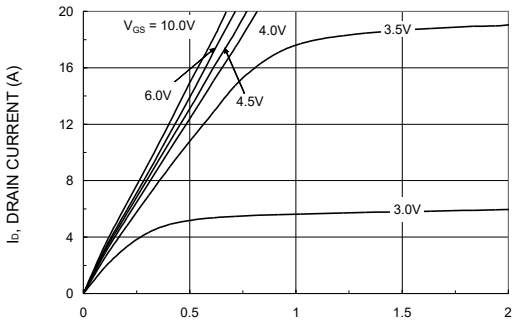


c) 135° C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

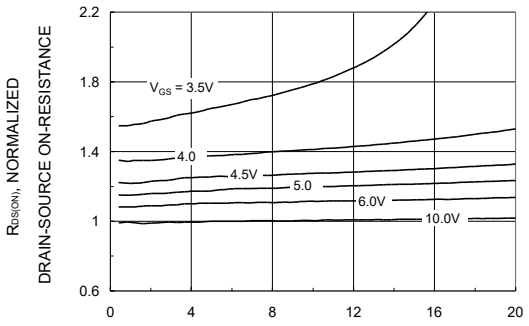
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

7.1 Typical characteristic



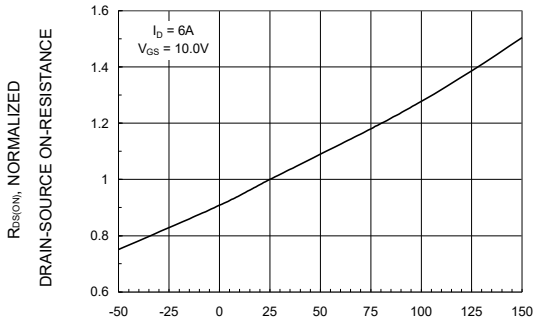
V_{DS}, DRAIN TO SOURCE VOLTAGE (V)

Fig 1: On-Region Characteristics.



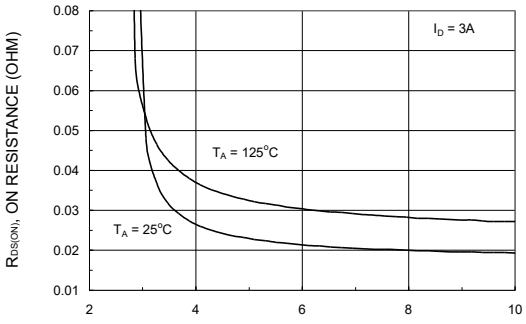
I_D, DRAIN CURRENT (A)

Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.



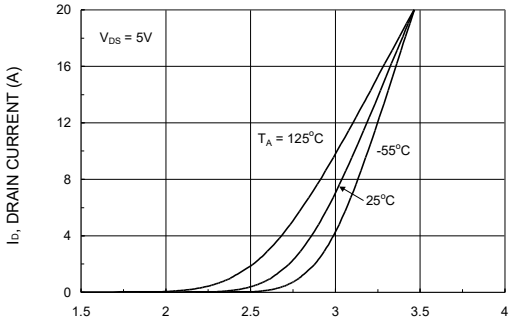
T_J, JUNCTION TEMPERATURE (°C)

Figure 3: On-Resistance Variation with Temperature.



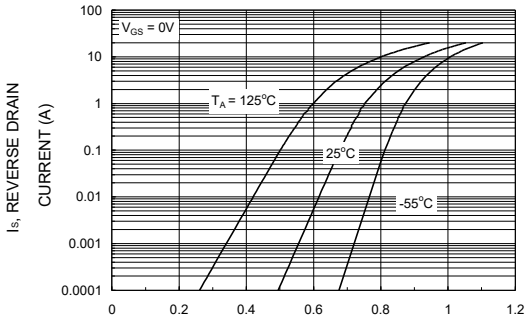
V_{GS}, GATE TO SOURCE VOLTAGE (V)

Figure 4: On-Resistance Variation with Gate-to-Source Voltage.



V_{GS}, GATE TO SOURCE VOLTAGE (V)

Figure 5: Transfer Characteristics.



V_{SD}, BODY DIODE VOLTAGE (V)

Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.

7.2 Typical characteristic

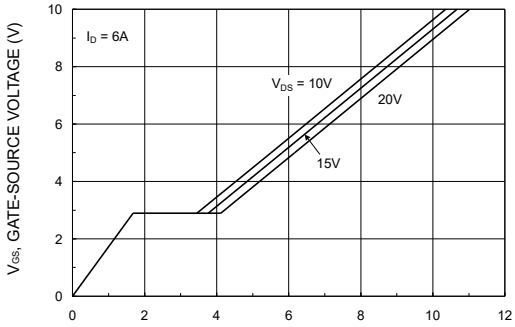


Figure 7: Gate-Charge Characteristics.

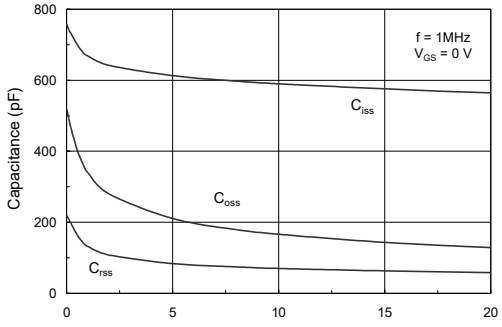


Figure 8: Capacitance Characteristics.

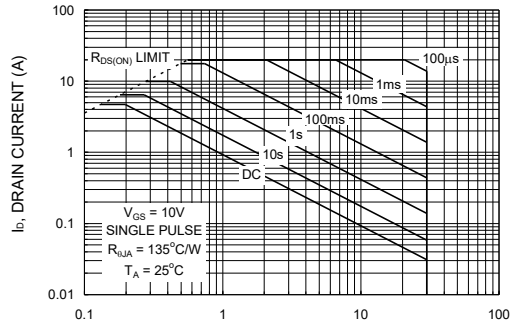


Figure 9: Maximum Safe Operating Area.

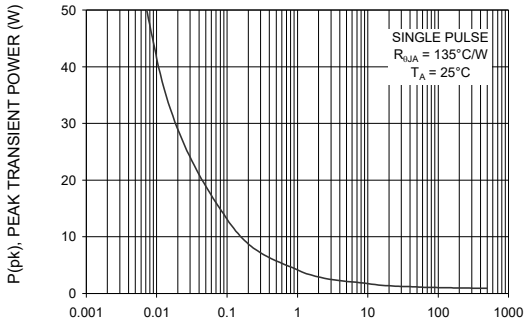


Figure 10: Single Pulse Maximum Power Dissipation.

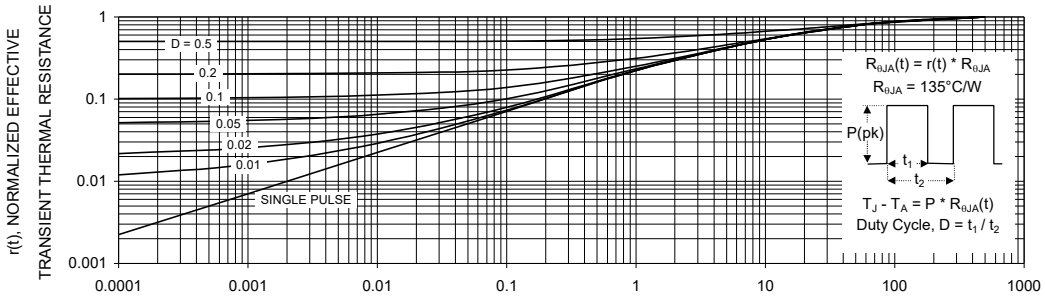
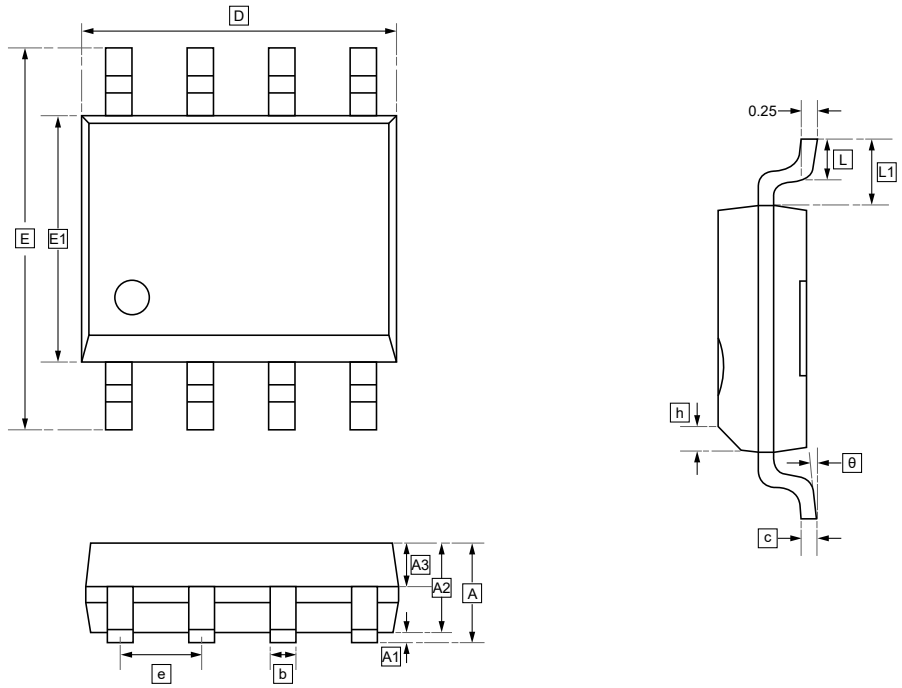


Figure 11: Transient Thermal Response Curve.

8.SOP-8 Package Outline Dimensions

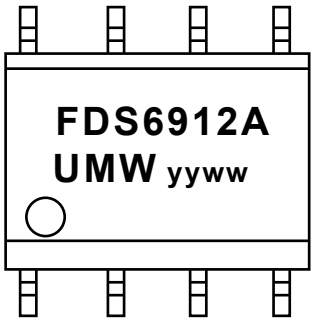


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS6912A	SOP-8	3000	Tape and reel

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