

## 1.Description

The ESD5Zxx Series is designed to protect voltage sensitive components from ESD and transient voltage events. Excellent clamping capability, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium.

## 3.Features

- Low Clamping Voltage
- Small Body Outline Dimensions:  
0.047" x 0.032" (1.20 mm x 0.80 mm)
- Low Body Height: 0.028" (0.7 mm)
- Stand-off Voltage: 2.5 V – 12 V
- Peak Power up to 240 Watts @ 8 x 20  $\mu$ s Pulse
- Low Leakage

## 2.Mechanical Characteristics

CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94V-0

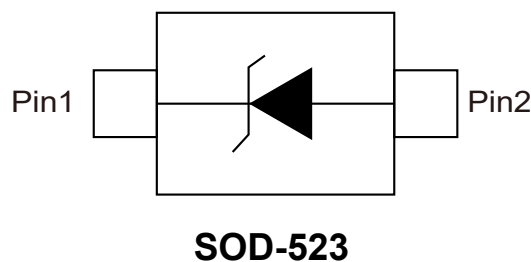
LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE:  
260°C Device Meets MSL 1 Requirements

- Response Time is Typically < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000-4-2 Level 4 ESD Protection
- IEC61000-4-4 Level 4 EFT Protection
- These Devices are Pb-Free and are RoHS Compliant

## 4.Pinning information





## 5. Absolute Ratings

Parameter	Symbol	Value	Units
IEC 61000-4-2 (ESD)	Contact	±30	kV
	Air	±30	kV
IEC 61000-4-4 (EFT)		40	A
ESD Voltage	Per Human Body Model	16	kV
	Per Machine Model	400	V
Total Power Dissipation on FR-4 Board (Note 1)@ T <sub>A</sub> =25°C	P <sub>D</sub>	200	mW
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
Lead Solder Temperature-Maximum (10 Second Duration)	T <sub>L</sub>	260	°C

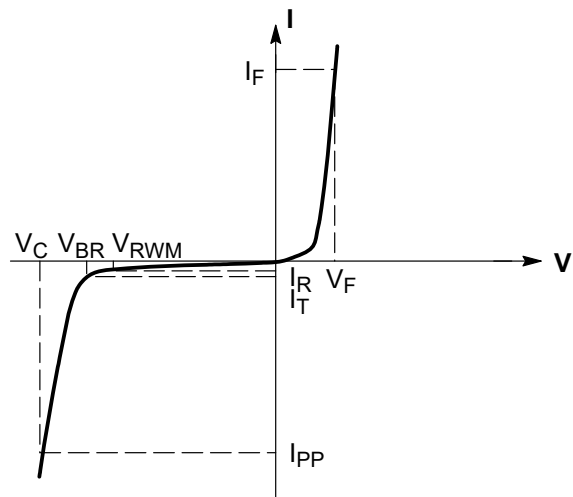
Notes:

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 printed circuit board, single-sided copper, mounting pad 1 cm<sup>2</sup>.



6.Electrical Parameters (T<sub>A</sub>=25°C unless otherwise noted )



Uni-Directional TVS

Symbol	Parameter
I <sub>PP</sub>	Maximum Reverse Peak Pulse Current
V <sub>C</sub>	Clamping Voltage @ I <sub>PP</sub>
V <sub>RWM</sub>	Working Peak Reverse Voltage
I <sub>R</sub>	Maximum Reverse Leakage Current @ V <sub>RWM</sub>
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>
I <sub>T</sub>	Test Current
I <sub>F</sub>	Forward Current
V <sub>F</sub>	Forward Voltage @ I <sub>F</sub>
P <sub>PK</sub>	Peak Power Dissipation
C	Max. Capacitance @V <sub>R</sub> =0 and f =1MHz



## 7. Electrical Characteristic ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Device	Device Marking	$V_{RWM}$ (V)	$I_R$ ( $\mu\text{A}$ ) @ $V_{RWM}$	$V_{BR}$ (V) @ $I_T$ (Note 2)	$I_T$	$V_C$ (V) @ $I_{PP}=5.0\text{A}^\dagger$	$V_C$ (V) @ Max $I_{PP}^\dagger$	$I_{PP}$ (A) <sup>†</sup>	$P_{pk}$ (W) <sup>†</sup>	C (pF)	$V_C$
		Max	Max	Min	mA	Typ	Max	Max	Max	Typ	Per IEC61000-4-2 (Note 3)
ESD5Z2.5T1G	ZD	2.5	6.0	4.0	1.0	6.5	10.9	11.0	120	145	Figures 1 and 2 See Below (Note 4)
ESD5Z3.3T1G	ZE	3.3	0.05	5.0	1.0	8.4	14.1	11.2	158	105	
ESD5Z5.0T1G	ZF	5.0	0.05	6.2	1.0	11.6	18.6	9.4	174	80	
ESD5Z6.0T1G	ZG	6.0	0.01	6.8	1.0	12.4	20.5	8.8	181	70	
ESD5Z7.0T1G	ZH	7.0	0.01	7.5	1.0	13.5	22.7	8.8	200	65	
ESD5Z12T1G	ZM	12	0.01	14.1	1.0	17	25	9.6	240	55	

Notes:

<sup>†</sup> Surge current waveform per Figure 5.

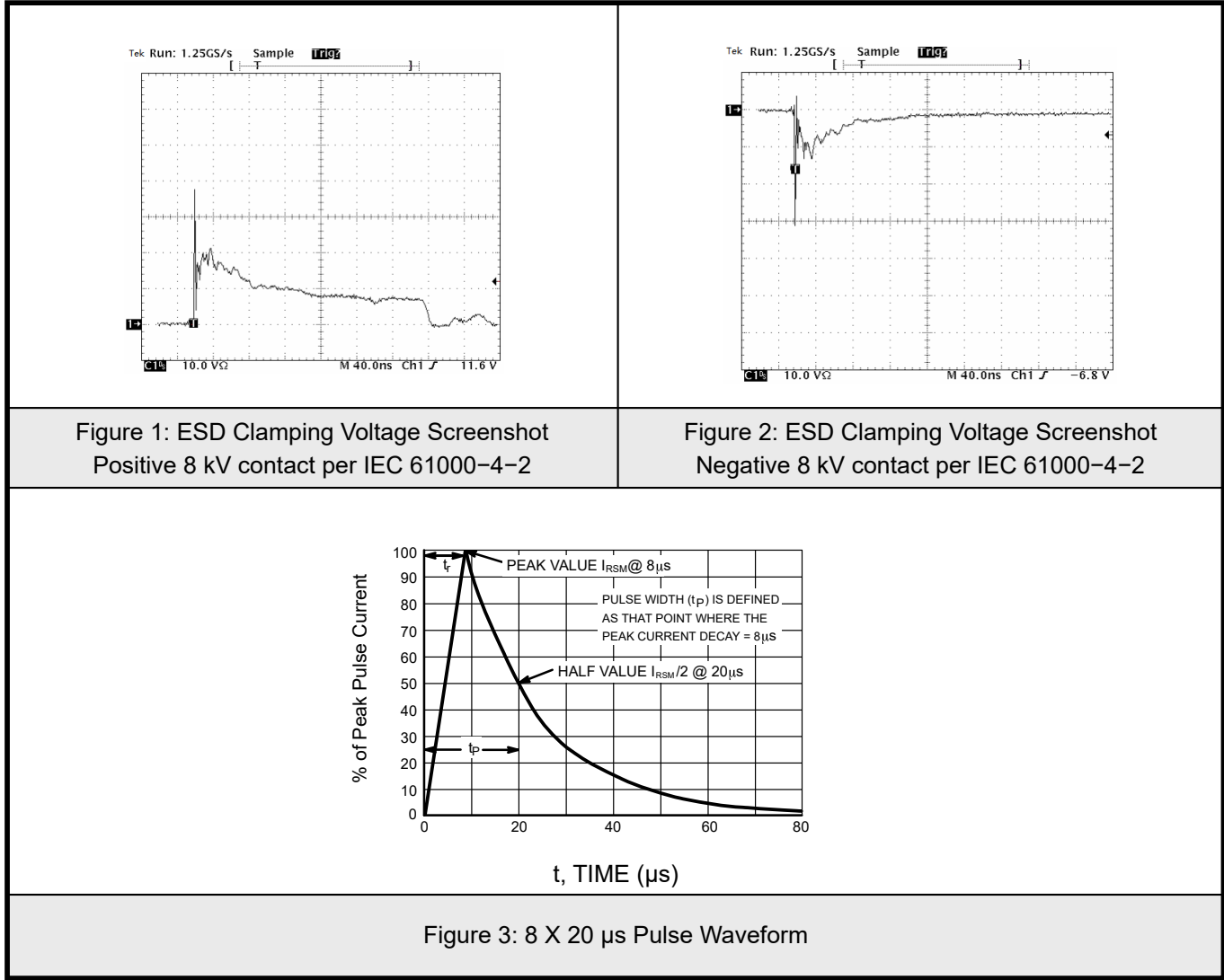
2.  $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .

3. For test procedure see Figures 3 and 4 .

4. ESD5Z5.0T1G shown below.



8.1Typical characteristic





8.2Typical characteristic

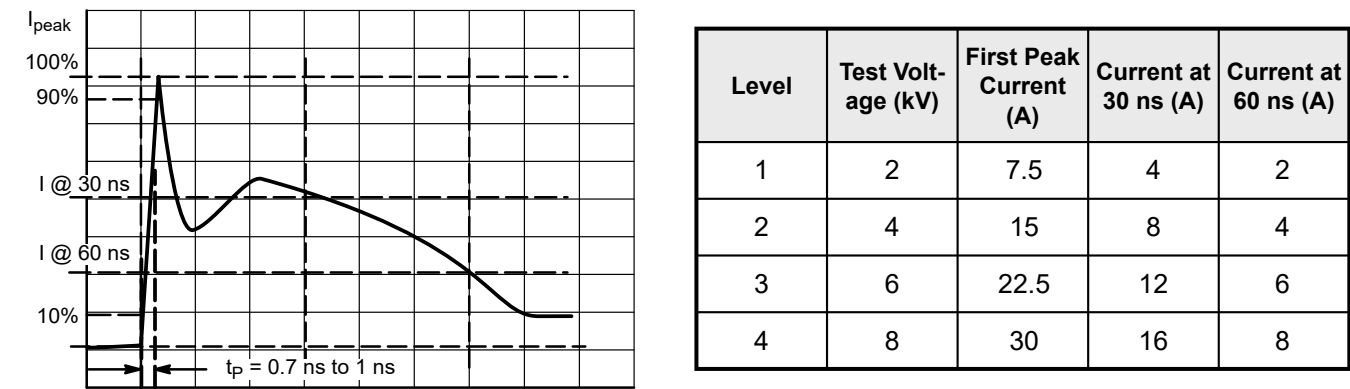


Figure 4: IEC61000-4-2 Spec



### 8.3 Typical characteristic

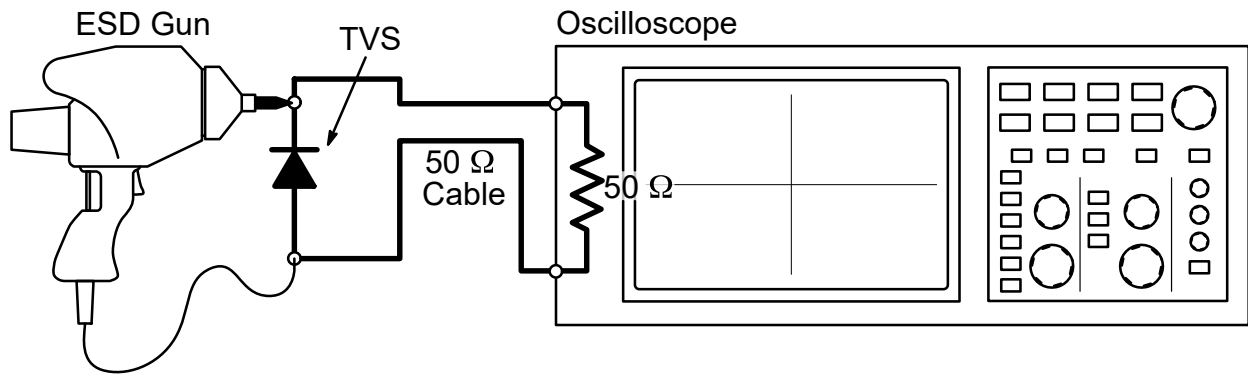


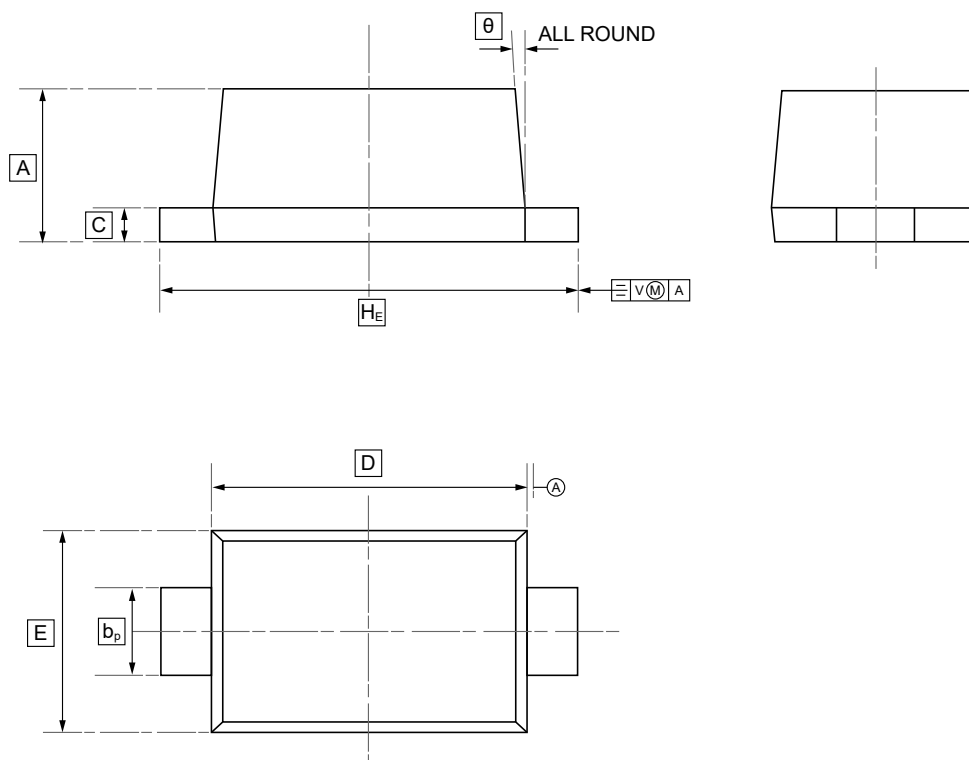
Figure 5: Diagram of ESD Test Setup

#### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. They has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes.



## 9.SOD-523 Package Outline Dimensions



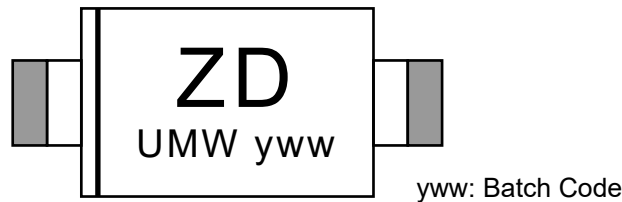
### DIMENSIONS (mm are the original dimensions)

Symbol	A	b <sub>p</sub>	C	D	E	H <sub>E</sub>	θ
Min	0.58	0.3	0.100	1.15	0.75	1.5	5°
Max	0.68	0.4	0.135	1.25	0.85	1.7	





10.Ordering information



Order Code	Package	Base QTY	Delivery Mode
UMW ESD5Z2.5T1G	SOD-523	3000	Tape and reel
UMW ESD5Z3.3T1G	SOD-523	3000	Tape and reel
UMW ESD5Z5.0T1G	SOD-523	3000	Tape and reel
UMW ESD5Z6.0T1G	SOD-523	3000	Tape and reel
UMW ESD5Z7.0T1G	SOD-523	3000	Tape and reel
UMW ESD5Z12T1G	SOD-523	3000	Tape and reel



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