

1. Description

This N-Channel Logic Level MOSFET is produced using advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

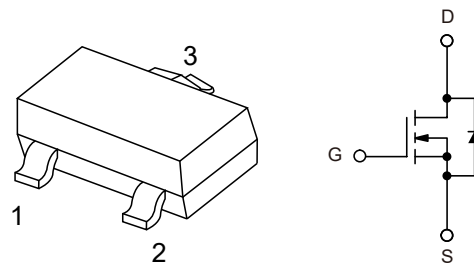
2. Features

- $V_{DS(V)}=30V$
- $I_D=2.7A$
- $R_{DS(ON)}<46m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<60m\Omega(V_{GS}=4.5V)$

3. Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23



4. Maximum ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current – Continuous (Note 1a) – Pulsed	I_D	2.7	A
		15	
Power Dissipation for Single Operation (Note 1a) (Note 1b)	P_D	0.5	W
		0.46	
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$
Thermal Characteristics			
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	250	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	75	$^{\circ}C/W$



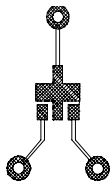
5. $T_A=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Breakdown Voltage Temp. Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA Referenced to 25°C		23		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	μA
		T _J =55°C			10	μA
Gate - Body Leakage, Forward	I _{GSSF}	V _{GS} =20V, V _{DS} =0V			100	nA
Gate - Body Leakage, Reverse	I _{GSSR}	V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.6	3	V
Gate Threshold Voltage Temp. Coefficient	ΔV _{GS(th)} /T _J	I _D =250μA Referenced to 25°C		-4		mV/°C
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =2.7A		37	46	mΩ
		V _{GS} =4.5V, I _D =2.4A		49	60	
On-State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =5V	15			A
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =2.7A		9.5		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =10V, f=1MHz		480		pF
Output Capacitance	C _{oss}			120		pF
Reverse Transfer Capacitance	C _{rss}			45		pF
SWITCHING CHARACTERISTICS (Note 2)						
Turn - On Delay Time	t _{D(on)}	V _{DD} =5V, I _D =1A V _{GS} =4.5V, R _{GEN} =6Ω		6	12	ns
Turn - On Rise Time	t _r			13	24	ns
Turn - Off Delay Time	t _{D(off)}			15	27	ns
Turn - Off Fall Time	t _f			4	10	ns

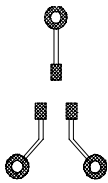


Total Gate Charge	Q _g	V _{DS} =10V, I _D =2.7A V _{GS} =5V		5	7	nC
Gate-Source Charge	Q _{gs}			1.4		nC
Gate-Drain Charge	Q _{gd}			1.6		nC
Drain–Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain–Source Diode Forward Current	I _s				0.42	A
Drain–Source Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _s =0.42A (Note)		0.65	1.2	V

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



6.1 Typical Characteristics

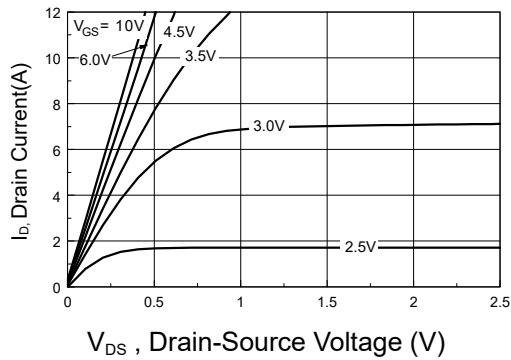


Figure 1: On-Region Characteristics.

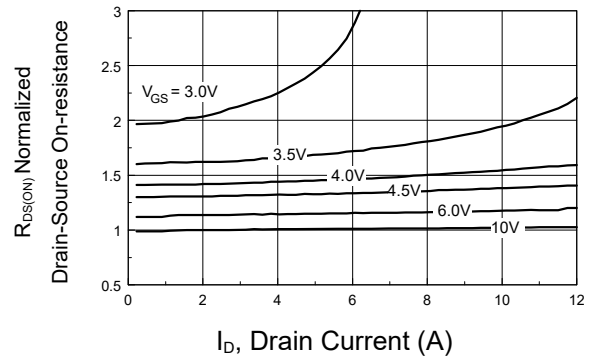


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.

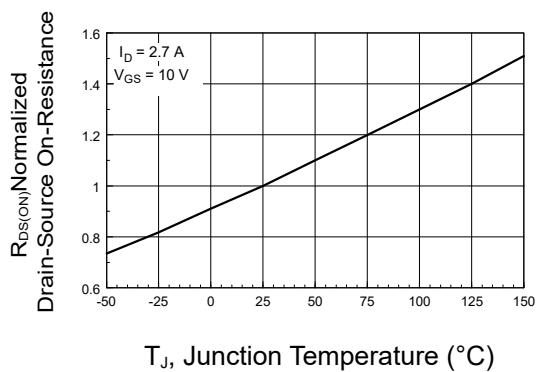


Figure 3: On-Resistance Variation with Temperature.

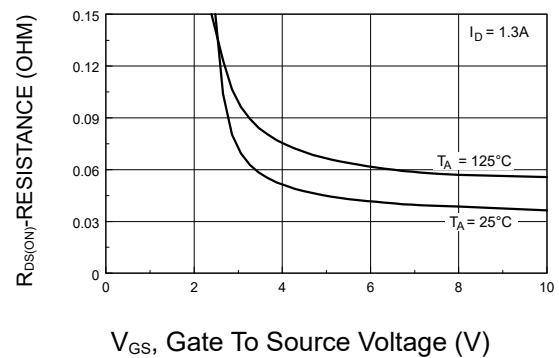


Figure 4: On-Resistance Variation with Gate-to-Source Voltage.

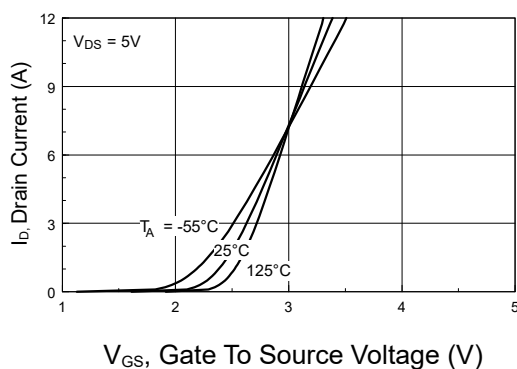


Figure 5: Transfer Characteristics.

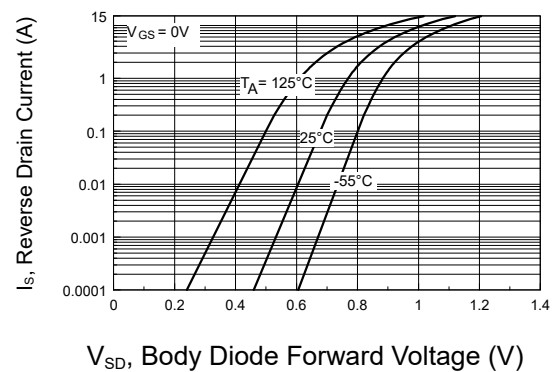


Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.



6.2 Typical Characteristics

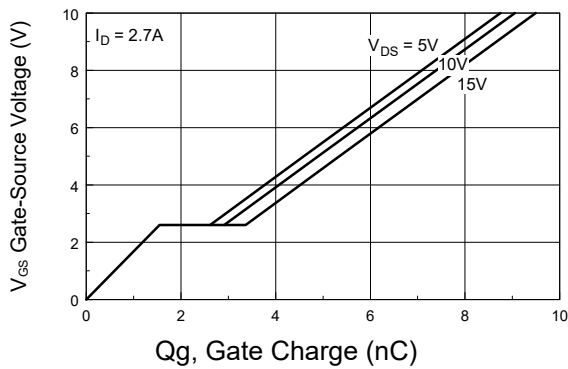


Figure 7: Gate-Charge Characteristics

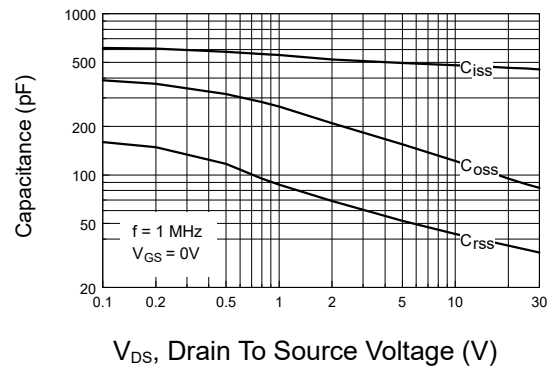


Figure 8: Capacitance Characteristics

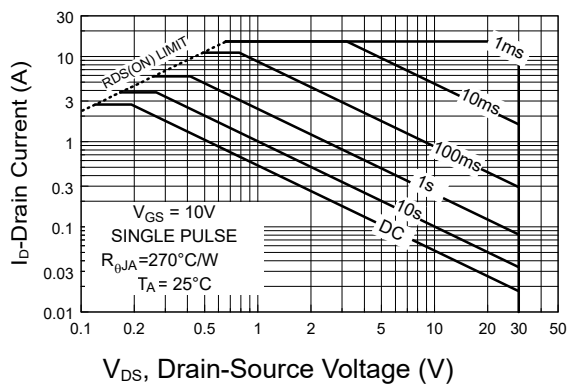


Figure 9: Maximum Safe Operating Area.

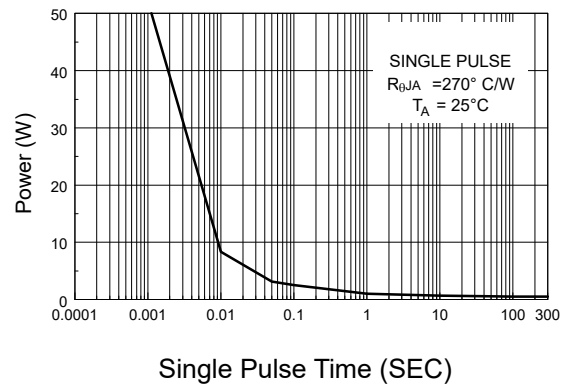


Figure 10: Single Pulse Maximum Power Dissipation.

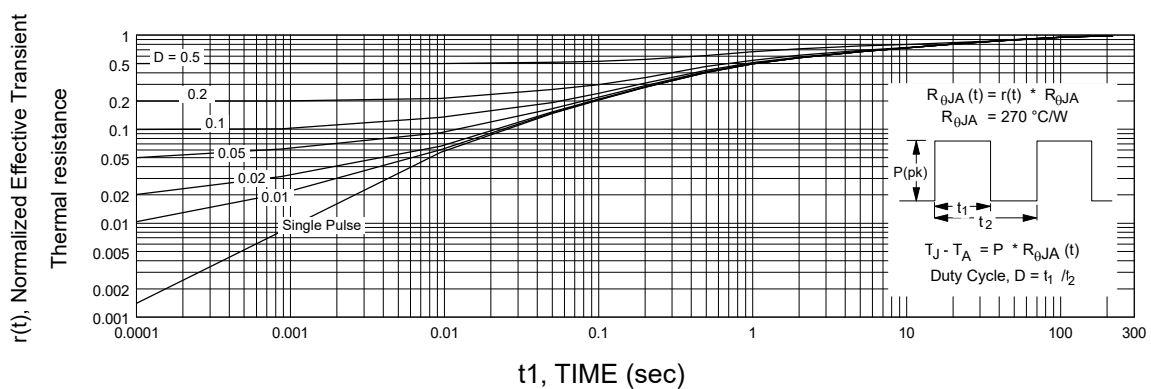
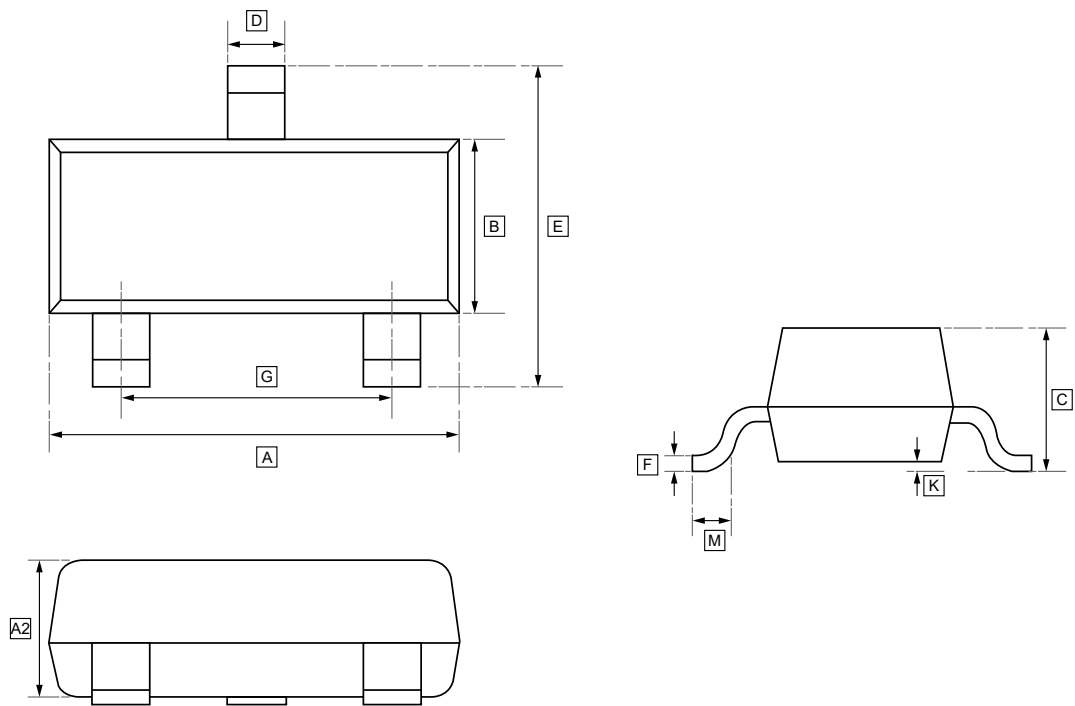


Figure 11: Transient Thermal Response Curve.



7.SOT-23 Package Outline Dimensions

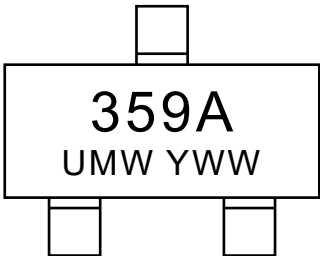


DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	D	E	G	K	M	A2	F
Min	2.85	1.20	0.90	0.40	2.25	1.80	0.00	0.30	0.95	0.095
Max	3.04	1.40	1.10	0.50	2.55	2.00	0.10	-	1.05	0.115



8.Ordering information



YWW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDN359AN	SOT-23	3000	Tape and reel



9.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.