UMW NTD4860NT4G

25V N-Channel MOSFET

1.Description

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses

2.1Features

- $V_{DS\ (V)}$=25V
- I_D=65A(V_{GS}=10V)
- $R_{DS(ON)}$<7.5mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<11.1mΩ(V_{GS}=4.5V)

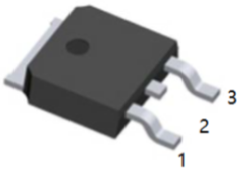
2.2Features

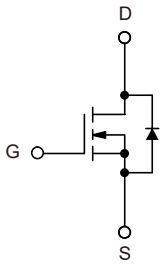
- VCORE Applications
- DC-DC Converters
- High/Low Side Switching

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_J= 25°C

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	Steady State	T_A=25°C	I_D	13	A
		T_A=85°C		10	A
Power Dissipation ($R_{\theta JA}$) (Note 1)		T_A=25°C	P_D	2	W
Continuous Drain Current ($R_{\theta JA}$) (Note 2)		T_A=25°C	I_D	10.4	A
		T_A=85°C		8	A
Power Dissipation ($R_{\theta JA}$) (Note 2)		T_A=25°C	P_D	1.28	W

Continuous Drain Current ($R_{\theta JC}$) (Note 1)	Steady State	T_C=25°C	I_D	65	A
		T_C=85°C		50	A
Power Dissipation ($R_{\theta JC}$) (Note 1)		T_C=25°C	P_D	50	W
Pulsed Drain Current	t_p=10μs	T_C=25°C	I_{DM}	130	A
Curent Limited by Package		T_A=25°C	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature		T_A=25°C	T_J,T_{STG}	-55 to+175	°C
Source Current (Body Diode)			I_S	42	A
Drain to Source dv/dt			dv/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (T_J=25°C ,V_{DD}=50V, V_{GS}=10V, I_L=13A_{pk}, L=1mH, R_G=25 Ω)			E_{AS}	84.5	mJ
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

5.Thermal resistance rating

Parameter	Symbol	Value	Units
Junction-to-Case (Drain)	$R_{\theta JC}$	3	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	°C/W
Junction-to-Ambient-Steady State (Note 1)	$R_{\theta JA}$	75	°C/W
Junction-to-Ambient-Steady State (Note 2)	$R_{\theta JA}$	117	°C/W

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

6.Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=0V	T_J=25°C			1	μA
		V_{DS}=20V	T_J=125°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V				±100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA		1.45		2.5	V
Negative Temperature Coefficient	$V_{GS(th)}/T_J$				5.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V	I_D=30A		6.1	7.5	mΩ
		V_{GS}=4.5V	I_D=30A		8.9	11.1	mΩ
Forward Transconductance	g_{FS}	V_{DS}=1.5V, I_D=15A			48		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=12V, f=1MHz			1308		pF
Output Capacitance	C_{oss}				342		pF
Reverse Transfer Capacitance	C_{rss}				169		pF
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}=4.5V, V_{DS}=15V, I_D=30A			11	16.5	nC
Threshold Gate Charge	$Q_{G(TH)}$				1.2		nC
Gate-to-Source Charge	Q_{GS}				3.9		nC
Gate-to-Drain Charge	Q_{GD}				4.7		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}=10V, V_{DS}=15V, I_D=30A			21.8		nC

SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(on)}$	V_{GS}=4.5V, V_{DS}=15V I_D=15A, R_G=3Ω		12.2		ns
Rise Time	t_r			20.1		ns
Turn-Off Delay Time	$t_{D(off)}$			15.2		ns
Fall Time	t_f			4.3		ns
Turn-On Delay Time	$t_{D(on)}$	V_{GS}=11.5V, V_{DS}=15V I_D=15A, R_G=3Ω		7.1		ns
Rise Time	t_r			17		ns
Turn-Off Delay Time	$t_{D(off)}$			22		ns
Fall Time	t_f			2.3		ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS}=0V I_D=30A	T_J=25°C	0.9	1.2	V
			T_J=125°C	0.76		V
Reverse Recovery Time	t_{rr}	V_{GS}=0V, dIs/dt=100A/μs I_S=30A		12.7		ns
Charge Time	t_a			7		ns
Discharge Time	t_b			5.7		ns
Reverse Recovery Time	Q_{rr}			3.5		nC
PACKAGE PARASITIC VALUES						
Source Inductance	L_S	T_A=25°C		2.49		nH
Drain inductance, DPAK	L_D			0.0164		nH
Drain Inductance, IPAK	L_D			1.88		nH
Gate Inductance	L_G			3.46		nH
Gate Resistance	R_G			0.75		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

7.1Typical Characterisitics

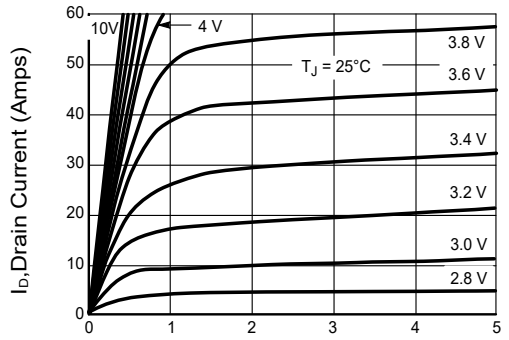


Figure 1: On−Region Characteristics

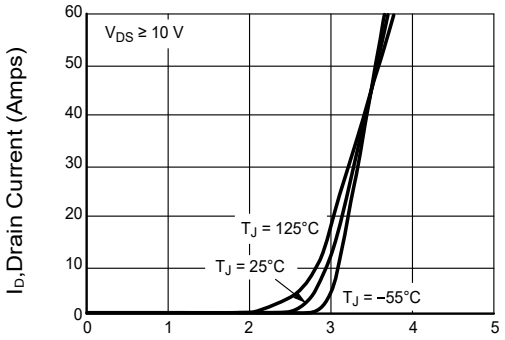


Figure 2: Transfer Characteristics

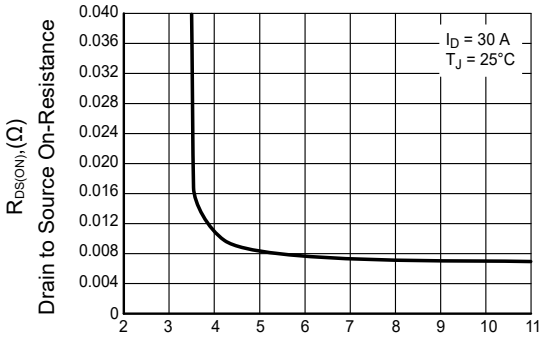


Figure 3: On−Resistance vs. Gate−to−Source Voltage

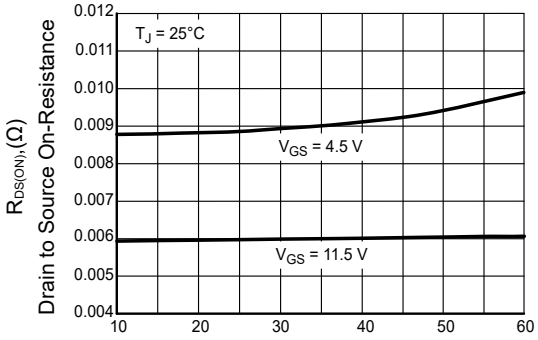


Figure 4: On−Resistance versus Drain Current and Gate Voltage

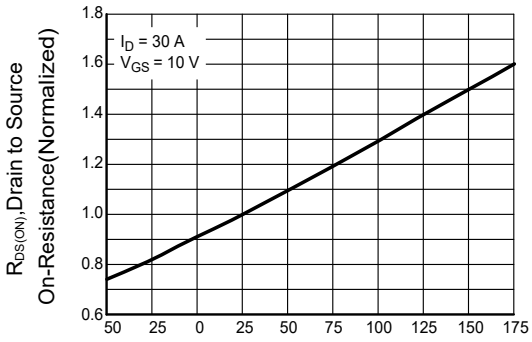


Figure 5: On−Resistance Variation with Temperature

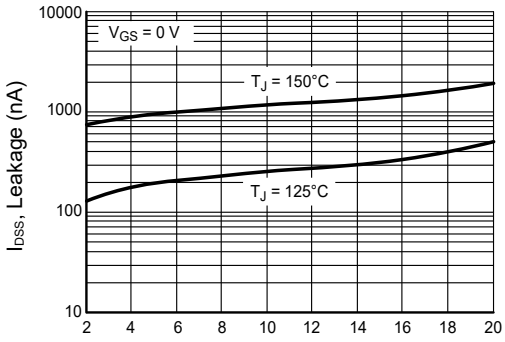


Figure 6: Drain−To−Source Leakage Current versus Voltage

7.2Typical Characterisitics

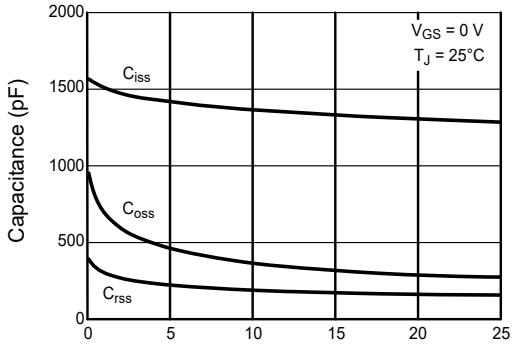


Figure 7: Capacitance Variation

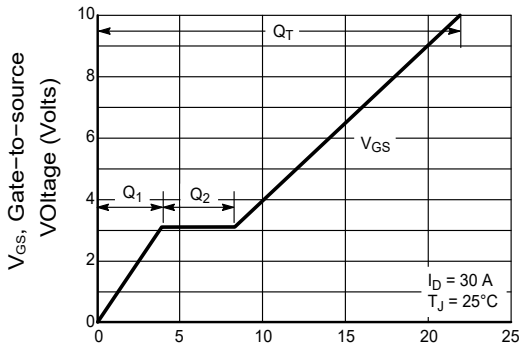


Figure 8: Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

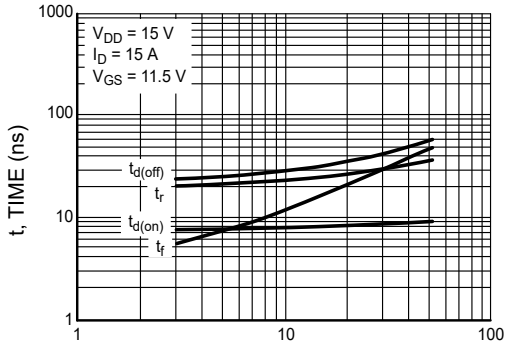


Figure 9: Resistive Switching Time Variation vs. Gate Resistance

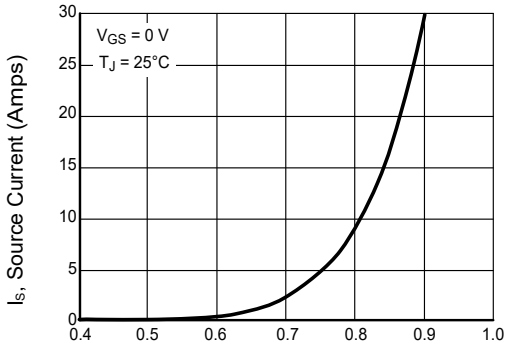


Figure 10: On−Resistance versus Drain Current and Gate Voltage

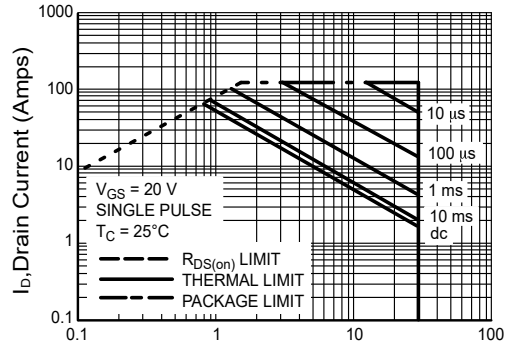


Figure 11: Maximum Rated Forward Biased Safe Operating Area

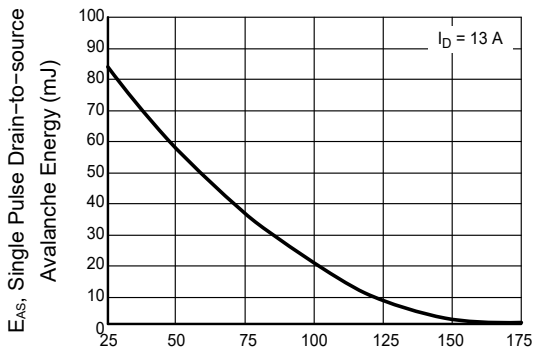


Figure 12: Maximum Avalanche Energy vs. Starting Junction Temperature

7.3Typical Characterisitics

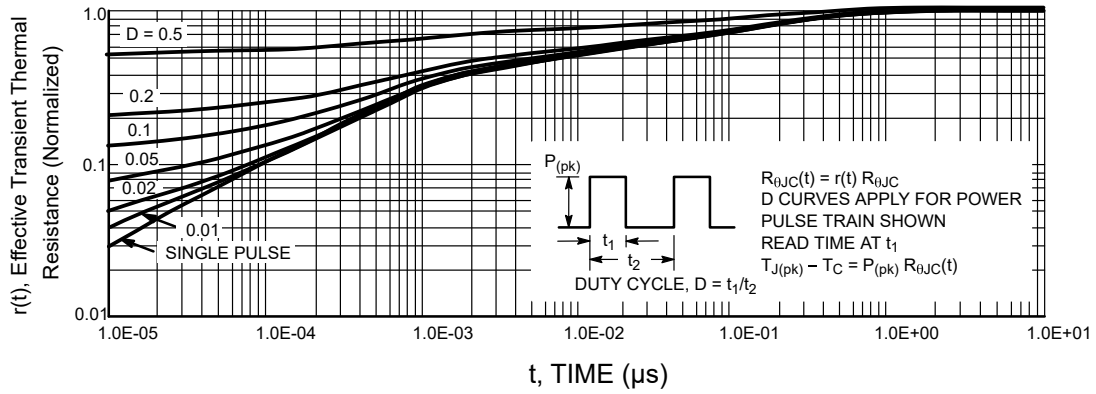
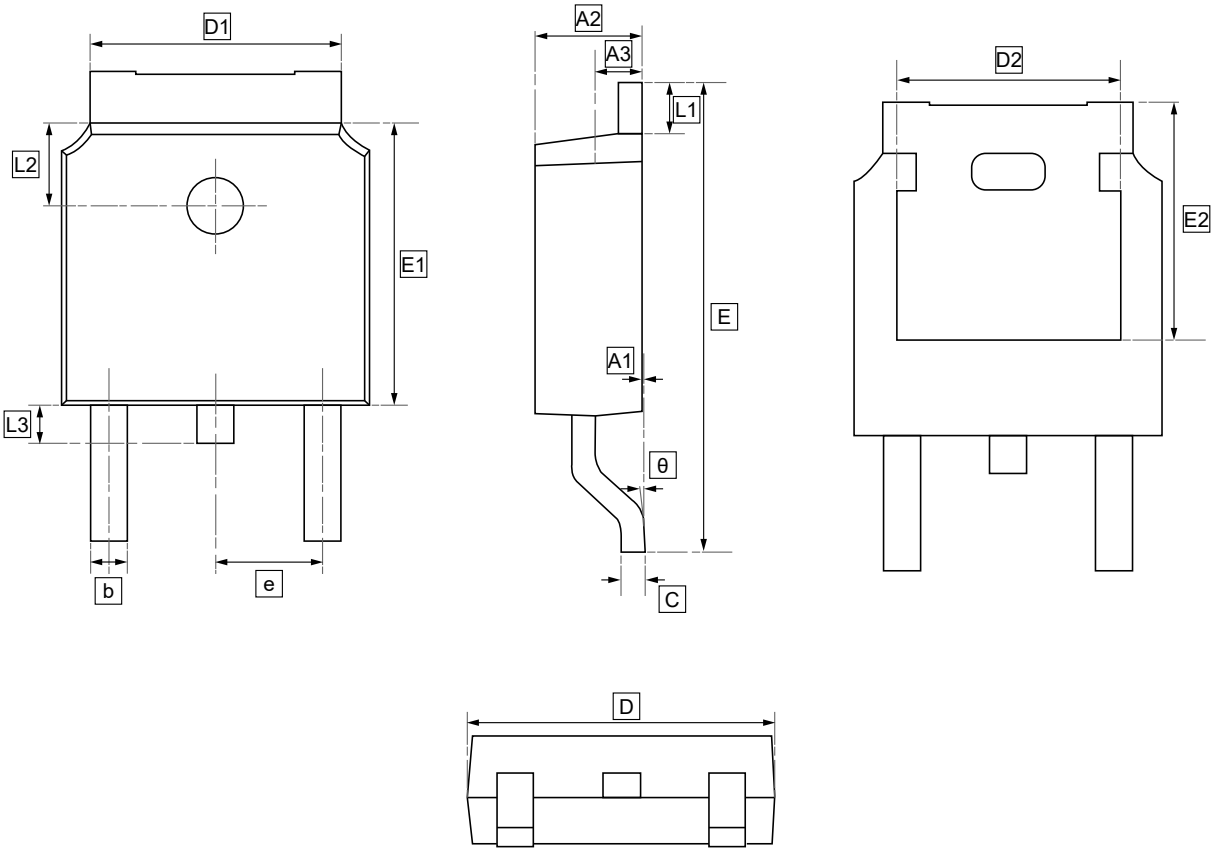


Figure 13: Thermal Response

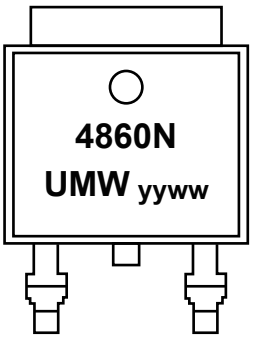
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NTD4860NT4G	TO-252	2500	Tape and reel

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