

1.Description

The TMP103 series temperature sensors are all in 4-Ball wafer-level packages, of which the TMP103A has a resolution of 1°C and the TMP103B has a resolution of 0.125°C.

The two-wire interface of the TMP103 series is compatible with SMBus and IC2 communication modes, and supports multi-chip access (MDA) commands, which can realize the communication between the host and multiple chips on the bus at the same time, without sending separate read and write commands to each TMP103 series chip. TMP103A supports up to 8 different address chips to be mounted on a main line, and TMP103B supports 16 different address chips to be mounted.

The TMP103 series is suitable for the system with limited temperature measurement area, temperature sensitivity, and multi-temperature area measurement and monitoring. The rated operating temperature range of the TMP103 series is -40°C ~ +125°C.

3.Applications

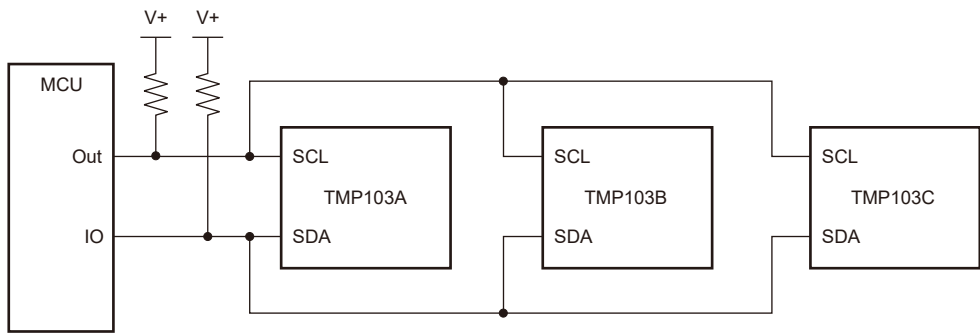
- Phone
- Laptop
- Solid State Drive (SSDs)
- Server

2.Features

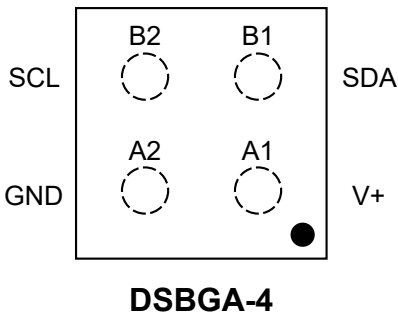
- Multiple Device Access (MDA)
 - Global read and write operations
- Temperature range: -40°C to +125°C
- Temperature measurement accuracy:
 - ±1°C (-40°C ~ +125°C)
- Package: 4-Ball WCSP (DSBGA)
- Supply voltage
 - TMP103A: 1.4V ~ 2.8V
 - TMP103B: 1.4V ~ 3.6V
- Low static current
 - Normal operation: ≤3μA (0.25Hz)
 - Off mode: ≤1μA
- Resolution
 - TMP103A: 8Bits
 - TMP103B: 11Bits
- Digital output: compatible with SMBus™ and IC² interfaces



4.TMP103 Application Diagram



5.Pinning Information



Pin Functions

Pin		Description
NO.	Name	
A1	V+	Supply voltage
A2	GND	Ground
B1	SDA	Serial data input. Open-drain output, requires a pull-up resistor
B2	SCL	Serial clock. Open-drain output, requires a pull-up resistor



6. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage, V+		4	V
Voltage at SCL, SDA	0.3	((V +) + 0.3) and ≤4	V
Operating Temperature	-55	150	°C
Junction Temperature		150	°C
Storage Temperature	-60	150	°C

In the course of using the TMP103 series, Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

7. ESD Ratings

Parameter		Value	Unit
Electrostatic discharge, V _{ESD}	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±5000	V
	Machine Mode (MM), per JEDEC-STD Classification	300	V

8. Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
Power supply voltage V+	TMP103A	1.4		2.8	V
	TMP103B	1.4		3.6	V
Operating temperature range T		-40		125	°C



9. Electrical Characteristics

Unless otherwise specified, the following data are the characteristics of the TMP103 series chip at the temperature of +25°C and the supply voltage in the range of 1.4V ~ 2.8V (TMP103A) / 1.4V ~ 3.6V (TMP103B).

Parameter	Conditions	Min	Typ	Max	Units
Operating Temperature Range		-40		125	°C
Accuracy (Temperature Error)	-10°C to 100°C, V+=1.8V	-2	0	2	°C
	-40°C to 125°C, V+=1.8V	-3	Plus or	3	°C
	vs Supply	0.5	+/-0.2	0.5	°C/V
Resolution	TMP103A		1		°C
			8		Bits
	TMP103B		0.125		°C
			11		Bits
Conversion Time			26	35	ms
Conversion Modes	CR1=0, CR0=0		0.25		Conv/s
	CR1=0, CR0=1		1		Conv/s
	CR1=1, CR0=0		4		Conv/s
	CR1=1, CR0=1		8		Conv/s
Timeout Time			30	40	ms
Communication Frequency		0.001		2.75	MHz
Power supply operating voltage	TMP103A	1.4		2.8	V
	TMP103B	1.4		3.6	V
Average Quiescent Current, I _Q	Bus not activated, CR1=0,CR0=0(default)		1.5	3	μA
	Bus activated, SCL frequency=400kHz		15		μA
	Bus activated, SCL frequency=3.4MHz		85		μA
Shutdown Current, I _{SD}	Bus is not activated, V+=1.8V		0.5		μA
	Bus activated, SCL frequency=400kHz		10		μA
	Bus activated, SCL frequency=3.4MHz		80		μA



10. Detailed Description

10.1 Device Functional Modules

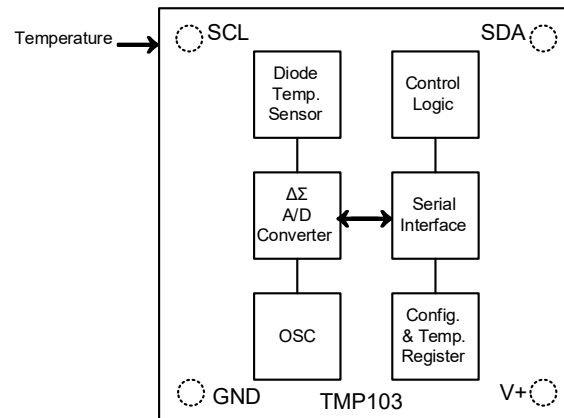


Figure 1: Block diagram of TMP103 series internal modules

10.2 Chip function mode

10.2.1 Continuous Conversion Mode

Write the M1 bit in the TMP103 series configuration register to 1, and the chip will be in continuous conversion mode. By changing the CR1 and CR0 bits in the configuration register, the temperature measurement rate of the TMP103 series in this mode can be configured to 0.25Hz, 1Hz, 4Hz, or 8Hz. After each conversion, the TMP103 series will power down and wait for a fixed delay set by CR1 and CR0 bits before the next conversion, as shown in Figure 2. Table 1 shows the configuration of the CR1 and CR0 bits.

Table 1. Conversion Rate Settings

CR1	CR0	Conversion Rate
0	0	0.25Hz (default)
0	1	1Hz
1	0	4Hz
1	1	8Hz

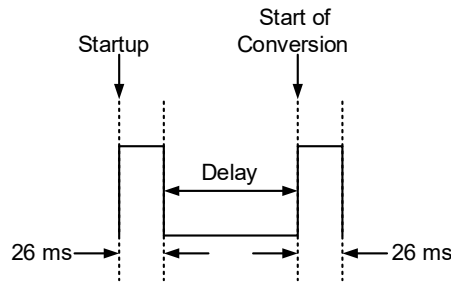


Figure 2: Schematic diagram of continuous conversion

10.2.2 Shutdown Mode

Write the M1 and M0 bits in the TMP103 series configuration register to 00, and the chip will enter shutdown mode after completing the conversion. In this mode, all circuits except the serial interface stop working, thus reducing the current of the TMP103 series to below 0.5 μ A (typical value).

10.2.3 Single Shot Mode (One-Shot Mode)

When the TMP103 series is in off mode, write the M1 and M0 bits of the configuration register to 01 to enable single shot conversion. During the conversion, the M1 and M0 bits are read as 01. After the single conversion is complete, the chip will return to the critical off state, with the M1 and M0 bits reading 00. When continuous temperature measurement is not required, this function can greatly reduce the chip power consumption.

Since the TMP103 series only takes 26ms (typical value) for a single temperature measurement, a higher temperature measurement rate can be achieved through this mode. By continuously configuring the TMP103 series in One-Shot mode, 30 or more temperature measurements per second can be achieved.

10.2.4 Temperature Monitoring Function

TMP103 series has temperature monitoring function. When the LC bit in the configuration register is written to 0, the chip goes into comparison mode. At this time, if the temperature measurement result is greater than or equal to the temperature threshold in the T_{HIGH} register, the high temperature marker bit FH in the configuration register will be set to 1, otherwise the bit will be set to 0; If it is less than or equal to the threshold value in the T_{LOW} register, the low temperature marker FL will be set to 1, otherwise the bit will be set to 0.



When the LC bit in the configuration register is written to 1, the chip enters interrupt mode. At this time, the FH and FL bits are set to 1 under the same conditions as in comparison mode. But after being set to 1, the FH and FL bits will remain in this state until the host sends a read command to the configuration register, and the FH and FL bits will be reset to 0.

The above process is shown in Figure 3. The default values for the above bits at power-on reset are FH=0, FL=0, LC=0.

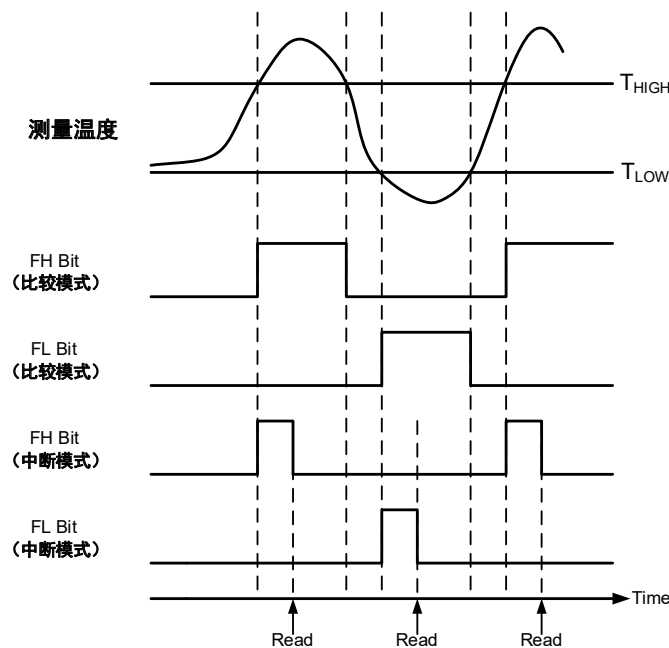


Figure 3: Schematic diagram of temperature monitoring function

10.3 Serial Interface

10.3.1 Bus Overview

The TMP103 series is compatible with SMBus and IC² interfaces. In the SMBus protocol, the device that initiates the transmission is called the host, and the device controlled by the host is called the slave. The bus must be controlled by the host, which produces the Serial clock Line (SCL), controls the bus access and produces the START and STOP signals. To address a specific slave, the master pulls the data line (SDA) from the high to the low level when the SCL is high to produce the START signal. All slaves on the bus receive 8bits of the slave address on the rising edge of the clock, where the last bit indicates whether to perform a read or write operation. In the ninth clock, the slave being addressed responds to the host by generating the Acknowledge bit and pulling the SDA



down. Thereafter the data transmission begins and sends an Ack bit after every eight clocks. The SDA must remain stable during the data transfer period when the SCL is at high power level. Because the SCL is on high power, any change in the SDA will be treated as a START or STOP signal.

After the data transfer is complete, the master generates a STOP signal to end the communication by pulling the SDA from low to high level during high SCL.

10.3.2 Serial Bus Address

In order to communicate with the TMP103 series, the host must first address the specified slave through the slave address byte. The slave address byte consists of seven address bits and a flag bit that indicates the execution of a read or write operation. TMP103 can provide 8 different address versions, TMP103S can provide 16 different address versions, respectively, as shown in Table 2 and Table 3. These addresses can be used as indicators of measuring positions or temperature zones.

Table 2. Mapping between TMP103 slave address and chip number

Product Number	Two-wire Address	Temperature Area
TMP103A	1110000	Zone1
TMP103B	1110001	Zone2
TMP103C	1110010	Zone3
TMP103D	1110011	Zone4
TMP103E	1110100	Zone5
TMP103F	1110101	Zone6
TMP103G	1110110	Zone7
TMP103H	1110111	Zone8



Table 3. Mapping between TMP103S slave address and chip number

Product Number	Two-wire Address	Temperature Area
TMP103SA	1110000	Zone1
TMP103SB	1110001	Zone2
TMP103SC	1110010	Zone3
TMP103SD	1110011	Zone4
TMP103SE	1110100	Zone5
TMP103SF	1110101	Zone6
TMP103SG	1110110	Zone7
TMP103SH	1110111	Zone8
TMP103SI	1111000	Zone9
TMP103SJ	1111001	Zone10
TMP103SK	1111010	Zone11
TMP103SL	1111011	Zone12
TMP103SM	1111100	Zone13
TMP103SN	1111101	Zone14
TMP103SO	1111110	Zone15
TMP103SP	1111111	Zone16



10.3.3 Read and Write Operations

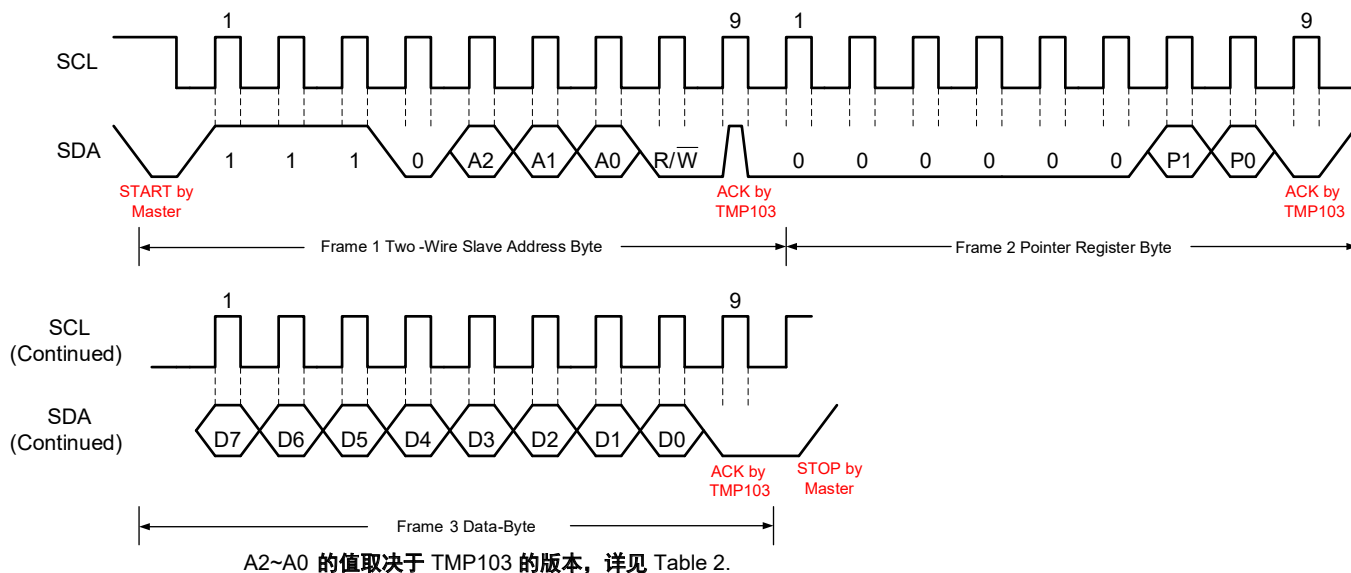


Figure 4: Two-wire write command timing diagram

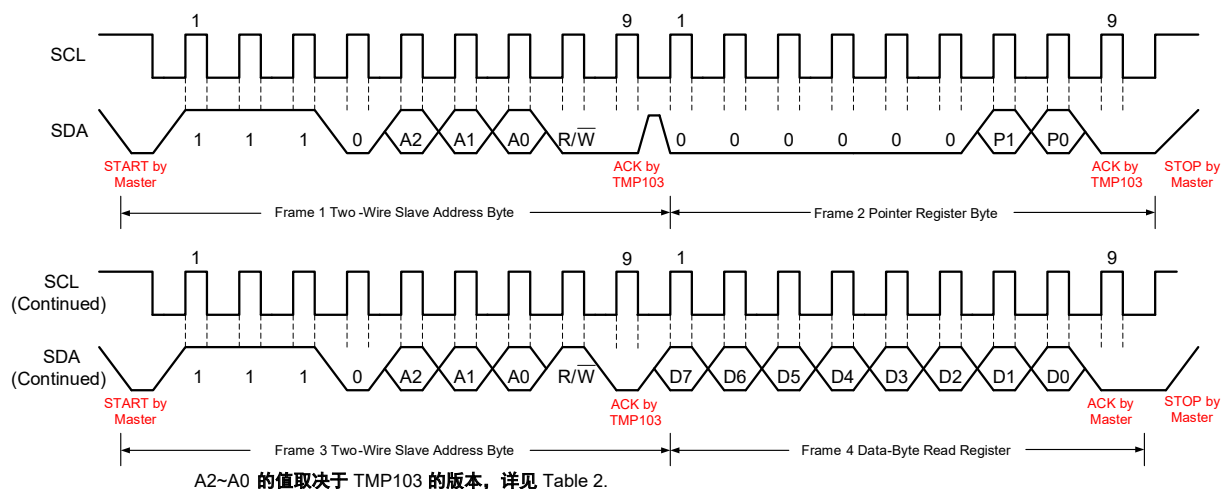


Figure 5: Two-wire reading command timing diagram

When writing data to the TMP103 series, after sending the slave address byte, the corresponding pointer register byte needs to be sent to access the specific register in the TMP103 series. Each write to the series requires the pointer register byte to be sent.

When reading data from the TMP103 series, after sending the slave address byte, you also need to send the corresponding pointer register byte. Unlike the write operation, if the data needs to be read from the same register repeatedly, the pointer register byte does not need to be sent each time, the chip will automatically read the data



from the previous pointer register; If the data needs to be read from a new register, it needs to rewrite and send a low slave address byte, then send a new pointer register byte, and then the host generates a START signal and sends a high slave address byte to start the read command. R/\bar{W} R/\bar{W}

It should be noted that the register byte should be sent first to MSB, then to LSB. Figure 4 and Figure 5 give a schematic of the above read and write operations, both using TMP103 as an example.

10.3.4 Multiple Device Access

TMP103 series supports multi-chip access (MDA), allowing the host to communicate with multiple TMP103 Series chips at different addresses on the same bus at the same time. The MDA command consists of an MDA read address (01h) and an MDA write address (00h), by which the chip acknowledges the MDA address and responds to the command. In order for the MDA command to execute properly, different numbered products from the single series of TMP103 must be used in the system, as shown in Table 2 and Table 3. It must be noted that when MDA functions are used, they cannot be used across series, such as TMP103A, TMP103B, and TMP103SC cannot be mounted on the same bus at the same time.

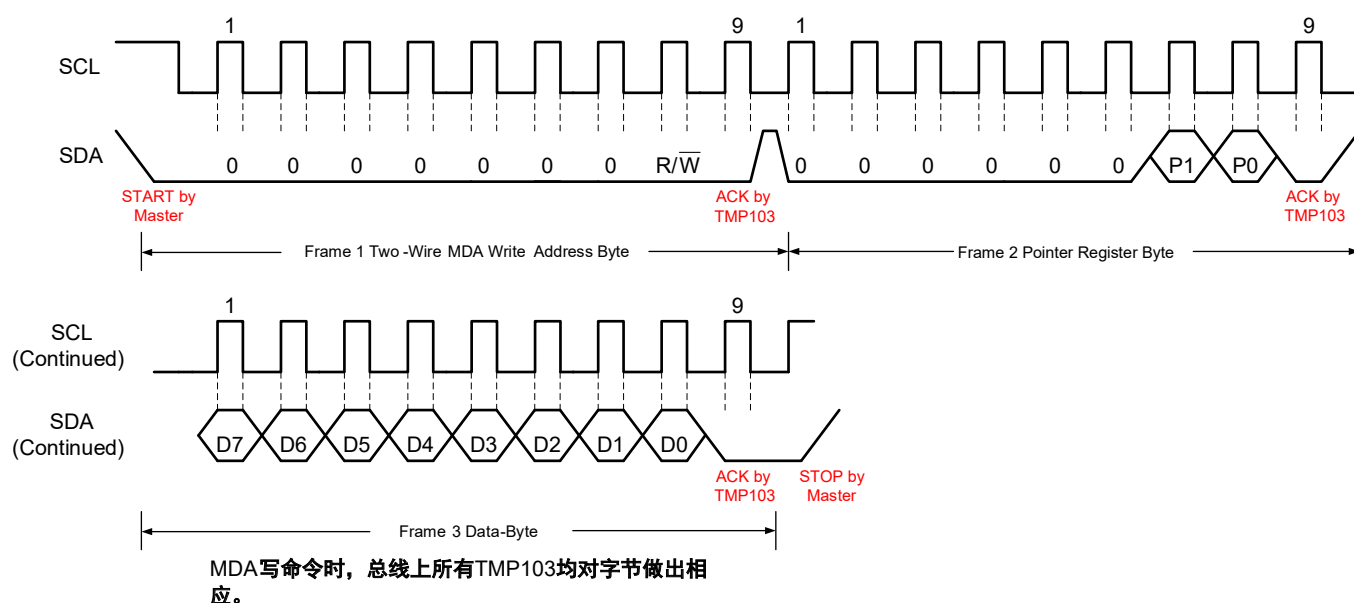


Figure 6: Timing diagram of two-wire MDA writing commands

When using the MDA write command, the host should send the MDA write address first, and then send the pointer address of the register that needs to be accessed. After sending the pointer address, all TMP103 series



chips on the bus will answer to this. The host will continue to send the byte that needs to be written to the appropriate register, and the multiple TMP103 series chips on the bus will store and answer the byte. The above process is shown in Figure 6.

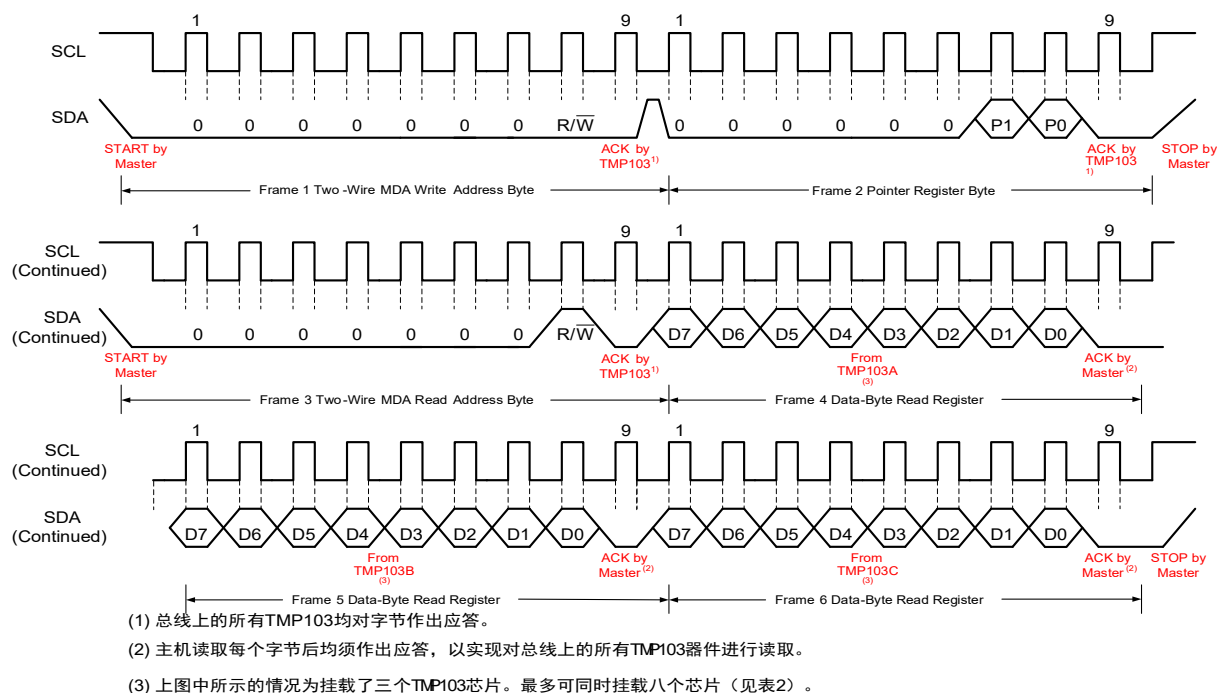


Figure 7: Timing diagram of two-wire MDA command reading

When the MDA read command is used, the host must first send the MDA write address and the pointer address of the register to be accessed. After that, the host continues to send the MDA read address. The TMP103 series chip on the bus returns the bytes to be read in turn. The host must send an ACK signal for each byte read. If the host does not respond to one of the returned bytes, all subsequent slaves will stop returning data. The above process is shown in Figure 7, with TMP103A, TMP103B, and TMP103C mounted on the bus at the same time.

For TMP103S, when the MDA command is used to read its temperature register, each chip of different models needs two bytes to return the data, and the host needs to respond to both high and low bytes.

If the bus contains an incomplete TMP103-series address sequence, the host must send all the required bytes for the free chip address to ensure normal MDA read operations. For example, if TMP103A, TMP103B, and TMP103D are mounted on the bus, the host must first send the MDA read address, which must be followed by four read register data bytes, each of which must be answered by the host to complete the MDA read operation. In the third byte where TMP103C is originally to be read, SDA should remain 1 in that data byte since TMP103C is not



mounted on the main line. If models A, B, and D of TMP103S are mounted, when the MDA command is used to read the temperature register, the host first sends the MDA read address, which must be followed by eight read register data bytes, and the host needs to respond to each data byte. In the fifth and sixth bytes of the TMP103SC that need to be read, SDA should remain 1 in both bytes since TMP103SC is not mounted on the main line.

10.3.5 Global Call Reset (General Call Reset)

The TMP103 series responds to the two-wire global response reset command 00h and executes the command in the second byte after it. If the second byte is 06h, the internal registers of the TMP103 series will all be reset to their power-on initial values. If the second byte is any other value, the TMP103 series will not respond to it.

10.3.6 High Speed Mode

The TMP103 series supports bus operation at frequencies higher than 400kHz. The host issues a high speed mode command (00001xxb) after the START signal to switch the bus to high speed mode. The TMP103 series does not answer the byte, but switches the input filter on its internal SDA and SCL pins and the output filter on the SDA pins to work in high speed mode, enabling the bus to transmit at a maximum frequency of 2.75MHz. When the high speed mode command is issued, the host will continue to send the slave address to initiate data transmission. The bus will continue to operate in high speed mode until a STOP signal appears on the bus. After receiving the STOP signal, the TMP103 series will switch to fast mode.

When using the high-speed mode for communication, it is necessary to pay attention to the size of the pull-up resistance on the SDA, SCL pins. If you need to communicate at a higher frequency, the size of the mounted pull-up resistance should be reduced accordingly. For a 5kΩ pull-up resistor, the upper limit of the communication frequency is 1.2MHz (typical value); To achieve a communication frequency of 2.75MHz, the pull-up resistor should have a resistance of less than 1.5kΩ (typical value).

10.3.7 Timeout Mode

If the SCL remains low at 30ms (typical value) between the START and STOP signals, the TMP103 series will reset its serial interface. That is, if the SCL is pulled down more than 30ms, the TMP103 series releases the SDA and waits for the START signal. To avoid activating the timeout function, the SCL should operate at a frequency greater than 1kHz.



10.4 Register Description

10.4.1 Pointer Register

Figure 8 shows the internal register structure of the TMP103 series. One of the 8-bit pointer registers is used to address specific data registers. The pointer register uses two LSBs to identify which data register should respond to read or write commands. Table 4 shows the configuration of each bit of the pointer register byte. During command writing, P2 through P7 must always be 0. Table 5 gives the pointer addresses of the available registers in the TMP103 series. The P1/P0 power-on reset value is 00. The TMP103 series is powered on by default to read the temperature register.

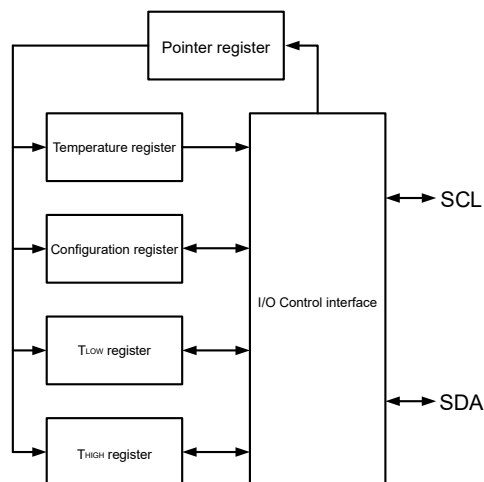


Figure 8: Internal register structure

Table 4. Each bit of pointer register byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	



Table 5. points to addresses

P1	P0	Register
0	0	Temperature register (R)
0	1	Configure Register (R/W)
1	0	T _{LOW} register (R/W)
1	1	T _{HIGH} register (R/W)

10.4.2 Temperature Register

The temperature registers of the TMP103 series are read-only registers, which are used to store the latest temperature measurement results, where the negative temperature is expressed in the form of binary complement. After power-on or reset, the temperature register reads 0 ° C by default.

The temperature register of the TMP103 is an 8-bit read only register, 1LSB=1 ° C. The temperature register of the TMP103S is a 16-bit read-only register, where byte 1 is a high byte, byte 2 is a low byte, and the high 11 bits are used to indicate the temperature (1LSB=0.125 ° C). The specific configuration and temperature data format are shown in Tables 6 to 8.

Table 6. TMP103 temperature register

D7	D6	D5	D4	D3	D2	D1	D0
T7	T6	T5	T4	T3	T2	T1	T0

Table 7. TMP103S temperature register

Byte	D7	D6	D5	D4	D3	D2	D1	D0
Byte1	T10	T9	T8	T7	T6	T5	T4	T3
Byte2	T2	T1	T0	0	0	0	0	0



Temperature (°C)	TMP103		TMP103S	
	Digital Output	Hexadecimal	Digital Output	Hexadecimal
128	0111 1111	7F	011 1111 1111	3FF
127.875	/	/	011 1111 1111	3FF
127	0111 1111	7F	011 1111 1000	3F8
100	0110 0100	64	011 0010 0000	320
80	0101 0000	50	010 1000 0000	280
75	0100 1011	4B	010 0101 1000	258
50	0011 0010	32	001 1001 0000	190
25	0001 1001	19	000 1100 1000	0C8
0.25	/	/	000 0000 0010	002
0	0000 0000	00	000 0000 0000	000
0.25	/	/	111 1111 1110	7FE
-1	1111 1111	FF	111 1111 1000	7F8
25-	1110 0111	E7	111 0011 1000	738
55-	1100 1001	C9	110 0100 1000	648



Table 12. Configuration Register High Byte

Bit	Field	Default	Description
7	ID (R)	0	BLANK
6	CR1 (R/W)	0	Continuous conversion rate selection bit Default: 00=0.25Hz, see Table 1
5	CR0 (R/W)	0	
4	FH (R)	0	High temperature marker bit 1= Temperature measured above T 0= Temperature measured below T
3	FL (R)	0	Low temperature marker bit 1= The temperature is measured below T 0= Temperature measured above T
2	LC (R/W)	0	Temperature monitoring mode selection bit 1= Interrupt mode 0= Compare mode
1	M1 (R/W)	1	Chip function mode select bit 00= Off mode 01= Single Switch mode 10, 11= Continuous conversion mode
0	M0 (R/W)	0	

10.4.4 Temperature Limit Register

The T_{HIGH} and T_{LOW} registers are used to store the temperature limit threshold of the TMP103 series temperature monitoring function. At the end of each temperature measurement, the TMP103 series compares the temperature measurement results to the temperature limit threshold. The temperature limit registers in the TMP103 series are all 8-bit read/write registers, where 1LSB=1 ° C, as shown in Table 10 and Table 11. It is worth noting that when the TMP103S performs temperature comparison, the result of the high 8 bits (byte 1) of its temperature register is compared with the value in the T_{HIGH} and T_{LOW} registers. The power- T_{LOW} on reset values of T_{HIGH} and T are: $T_{HIGH} = 60\text{ ° C}$; $T_{LOW} = -10\text{ ° C}$.

Table 10. T_{HIGH} registers in the TMP103 series

D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0

Table 11. T_{LOW} registers in the TMP103 series

D7	D6	D5	D4	D3	D2	D1	D0
L7	L6	L5	L4	L3	L2	L1	L0

11. Specific Applications

As a low power chip, the TMP103 series can further reduce the impact of external noise by adding an RC filter to its V+ pin, as shown in Figure 9, where R must be less than 5kΩ and C must be greater than 10nF.

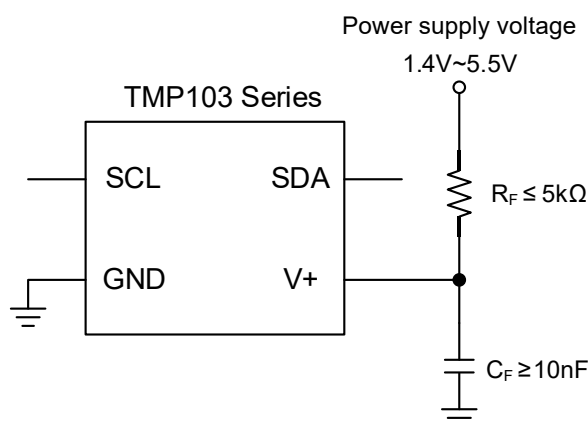
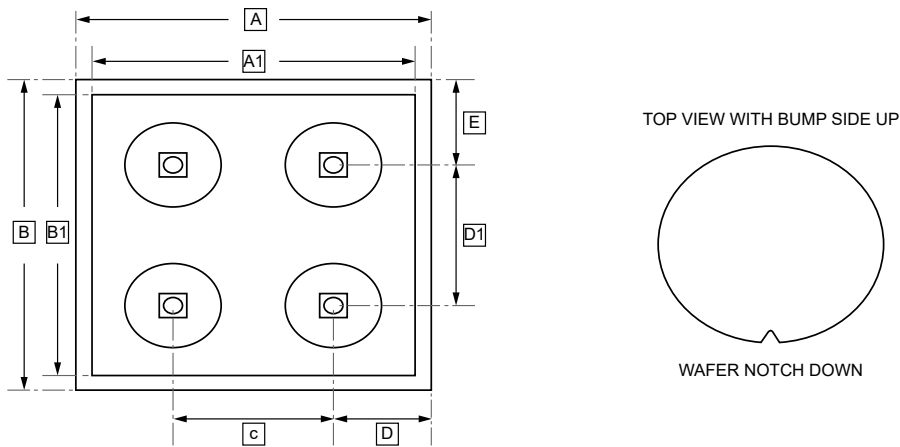


Figure 9: Noise cancellation technique

Place the device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.



12.DSBGA-4 Package Outline Dimensions

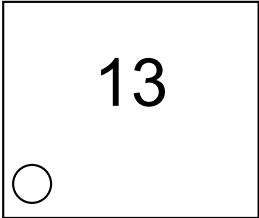


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	B	B1	c	D	D1	E
Nom	0.88	0.80	0.88	0.80	0.40	0.24	0.40	0.24



13.Ordering Information



Order Code	Marking	Package	Base QTY	Delivery Mode
UMW TMP103AYFFR	13	DSBGA-4	3000	Tape and reel
UMW TMP103BYFFT	TB	DSBGA-4	3000	Tape and reel



14.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.