

1.Features

- $V_{DS(V)}=60V$
- $R_{DS(ON)}<15.8m\Omega(V_{GS}=10V)$

3.Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply

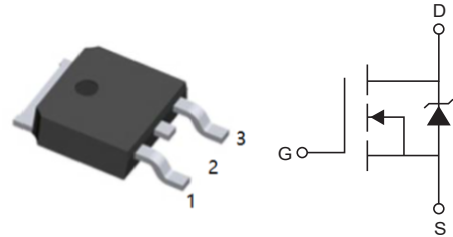
2.Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

4.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view



5.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, $V_{GS}=10V$	$T_C=25^{\circ}C$	I_D	43	A
Continuous Drain Current, $V_{GS}=10V$	$T_C=100^{\circ}C$		31	A
Pulsed Drain Current ①		I_{DM}	170	A
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	71	W
Linear Derating Factor			0.47	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Peak Diode Recovery ③		dv/dt	24	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)			300	°C



6.Avalanche Characteristics

Parameter	Symbol	Typ	Max	Units
Single Pulse Avalanche Energy ②	$E_{AS(Thermally\ limited)}$		73	mJ
Avalanche Current ①	I_{AR}		25	A
Repetitive Avalanche Energy ④	E_{AR}		7.1	mJ

7.Thermal Resistance

Parameter	Symbol	Typ	Max	Units
Junction-to-Case ⑧	$R_{\theta JC}$		2.12	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	0.5		°C/W
Junction-to-Ambient ⑦⑧	$R_{\theta JA}$		62	°C/W



8. Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	I _D =250μA, V _{GS} =0V	60			V
Breakdown Voltage Temp. Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D =5mA①,Reference to 25°C		0.075		V/°C
Static Drain-to-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =25A ④		12.6	15.8	mΩ
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =50μA	1		2.2	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			20	μA
		V _{DS} =48V, V _{GS} =0V, T _J =125°C			250	μA
Gate-to-Source Forward Leakage	I _{GSS}	V _{GS} =20V			100	nA
Gate-to-Source Reverse Leakage		V _{GS} =-20V			-100	nA
Dynamic @ T _J =25°C (unless otherwise specified)						
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =25A	41			S
Total Gate Charge	Q _g	I _D =25A, V _{DS} =30V, V _{GS} =10V④		22	30	nC
Gate-to-Source Charge	Q _{gs}			5		nC
Gate-to-Drain ("Miller") Charge	Q _{gd}			6.3		nC
Total Gate Charge Sync.(Q-Qdd	Q _{sync}	I _D =25A, V _{DS} =0V, V _{GS} =10V		28.3		nC
Internal Gate Resistance	R _{G(int)}			0.79		Ω
Turn-On Delay Time	t _{D(on)}	V _{DD} =39V, I _D =25A R _G =20Ω, V _{GS} =10V ④		6.3		ns
Rise Time	t _r			40		ns
Turn-Off Delay Time	t _{D(off)}			49		ns
Fall Time	t _f			47		ns
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =50V, f=1MHz		1150		pF
Output Capacitance	C _{oss}			130		pF
Reverse Transfer Capacitance	C _{rss}			67		pF
Effective Output Capacitance (Energy Related) ⑥	C _{oss} eff.(ER)	V _{GS} =0V, V _{DS} =0V to 60V ⑥		190		pF
Effective Output Capacitance (Time Related)⑤	C _{oss} eff.(TR)	V _{GS} =0V, V _{DS} =0V to 60V ⑤		230		pF



Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			43	A
Pulsed Source Current (Body Diode) ①	I_{SM}				170	A
Diode Forward Voltage	V_{SD}	$T_J=25^{\circ}\text{C}, I_S=25\text{A}, V_{GS}=0\text{V}$ ④			1.3	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, V_R=51\text{V}$		22	33	ns
		$T_J=125^{\circ}\text{C}, I_F=25\text{A}$		26	39	ns
Reverse Recovery Charge	Q_{rr}	$T_J=25^{\circ}\text{C}, di/dt=100\text{A}/\mu\text{s}$ ④		17	26	nC
		$T_J=125^{\circ}\text{C}$		24	36	nC
Reverse Recovery Current	I_{RRM}	$T_J=25^{\circ}\text{C}$		1.4		A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax} , starting $T_J=25^{\circ}\text{C}$, $L=0.23\text{mH}$, $R_G=25\Omega$, $I_{AS}=25\text{A}$, $V_{GS}=10\text{V}$.

Part not recommended for use above this value.

③ $I_{SD} \leq 25\text{A}$, $di/dt \leq 1580\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^{\circ}\text{C}$.

④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑧ R_{θ} is measured at T_J approximately 90°C .



9.1 Typical Characteristics

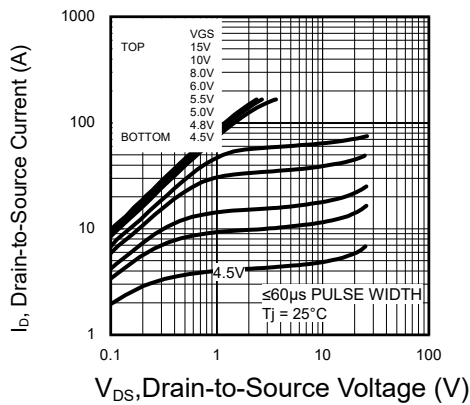


Figure 1: On-Region Characteristics

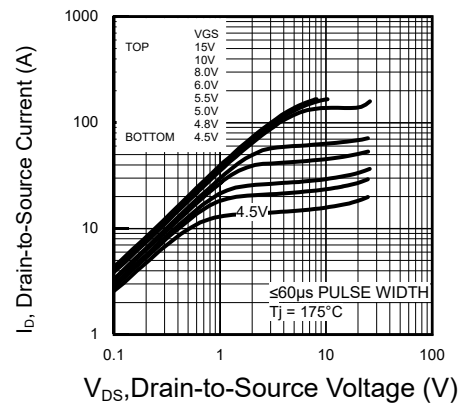


Figure 2: Typical Output Characteristics

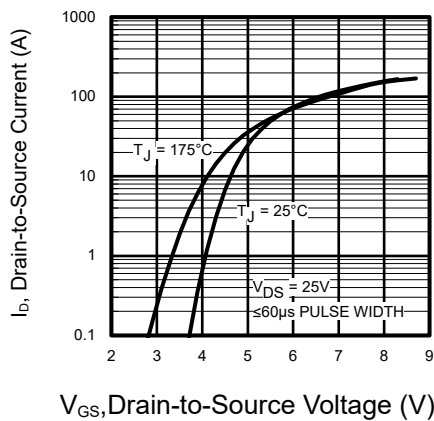


Figure 3: Typical Transfer Characteristics

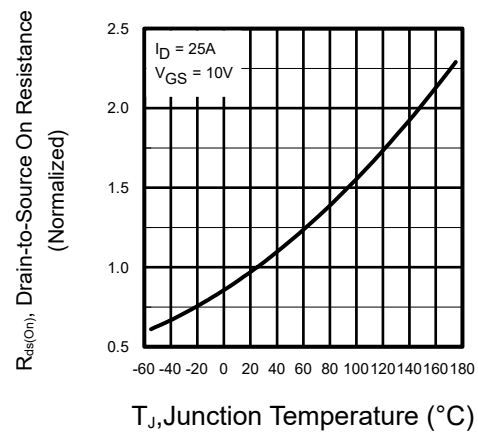


Figure 4: Normalized On-Resistance vs. Temperature

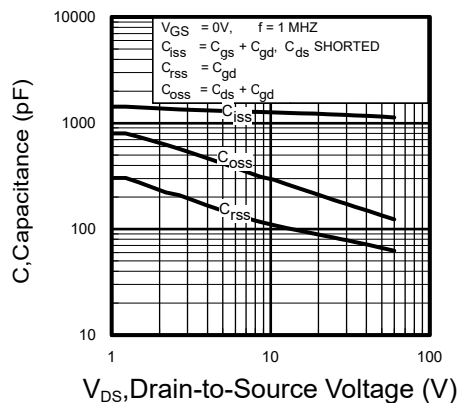


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

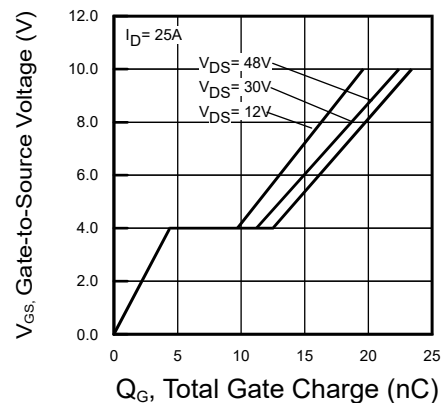


Figure 6: Typical Gate Charge vs. Gate-to-Source Voltage



9.2 Typical Characteristics

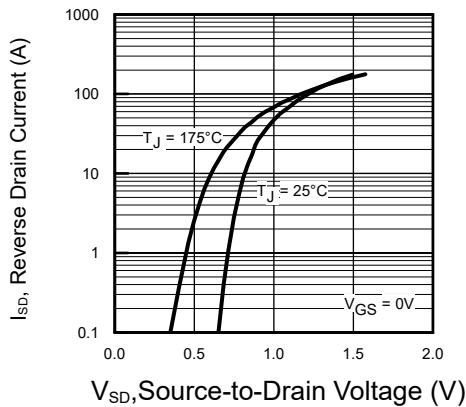


Figure 7: Typical Source-Drain Diode Forward Voltage

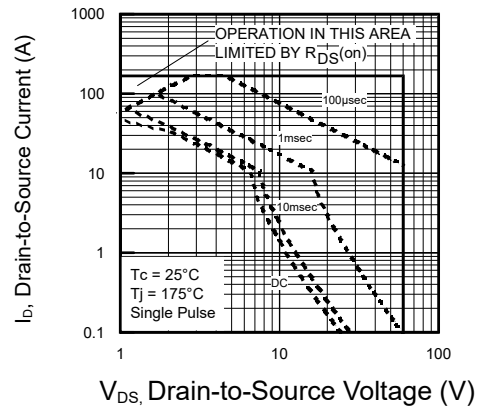


Figure 8: Maximum Safe Operating Area

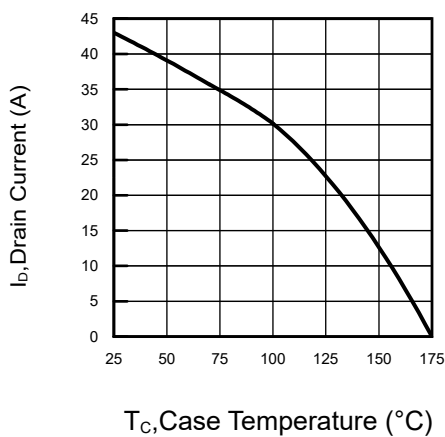


Figure 9: Maximum Drain Current vs. Case Temperature

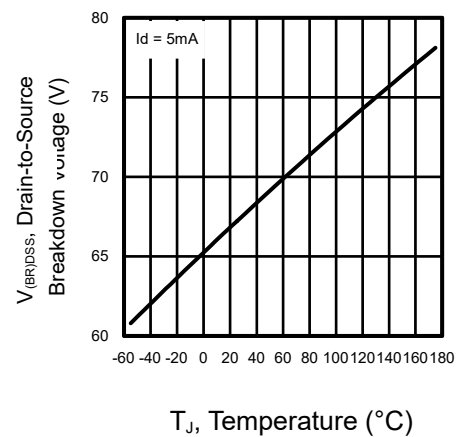


Figure 10: Drain-to-Source Breakdown Voltage

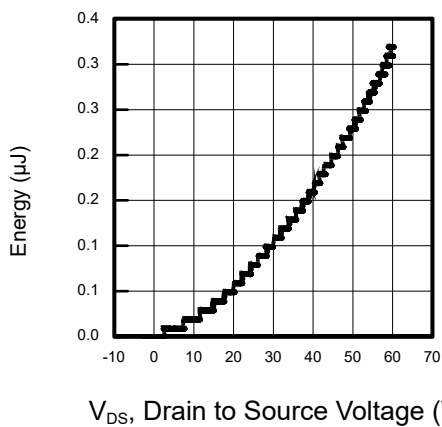
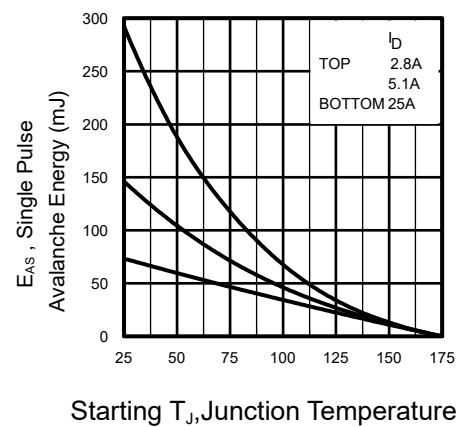
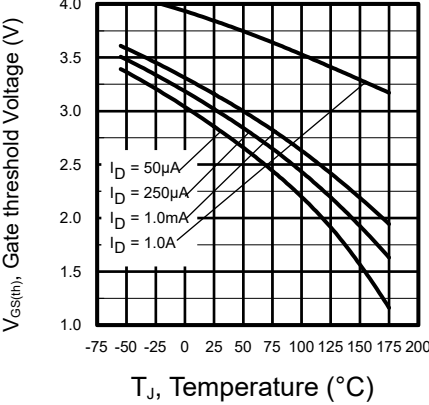
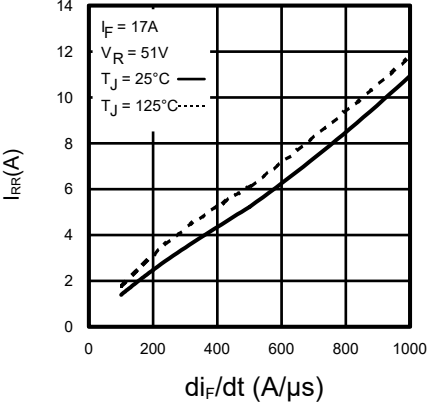
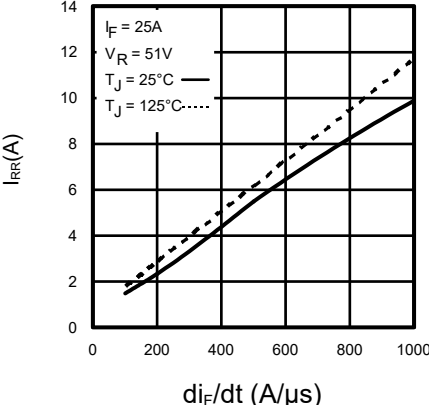
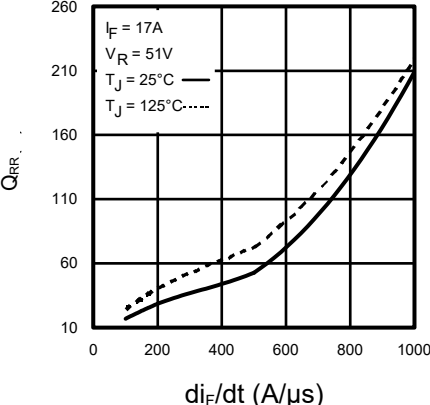
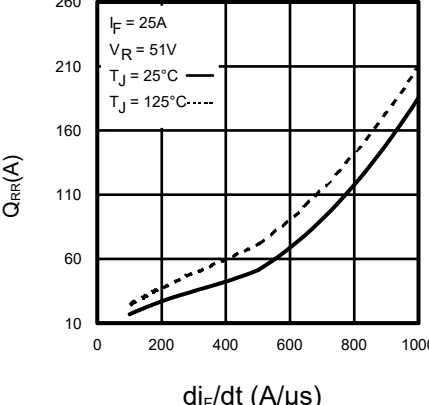
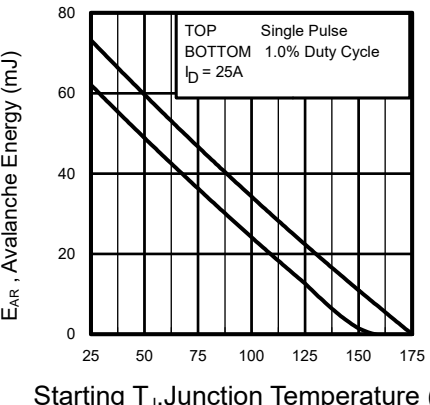
Figure 11: Typical C_{OSS} Stored Energy

Figure 12: Maximum Avalanche Energy vs. DrainCurrent

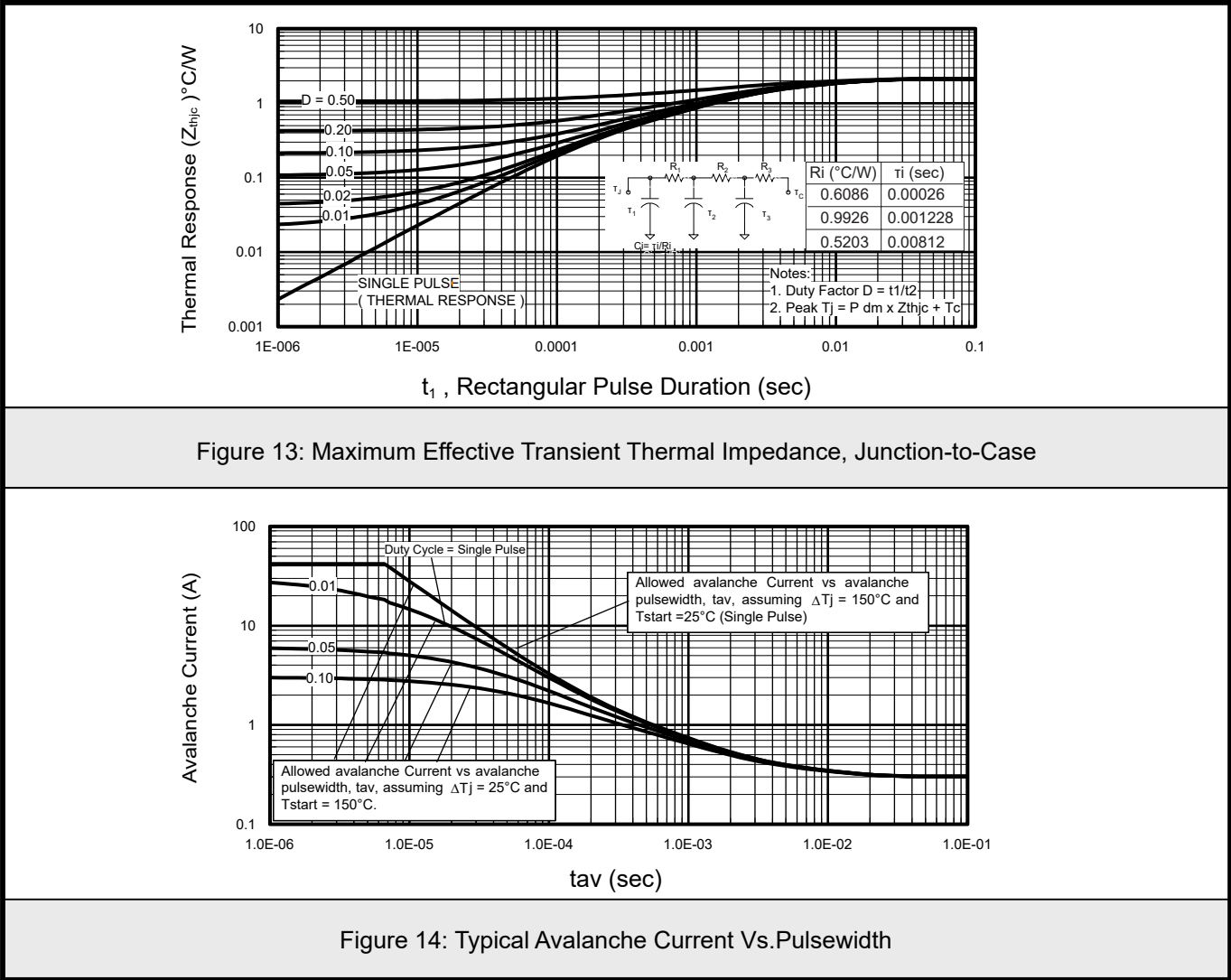


9.3Typical Characterisitics

	
Figure 13: Threshold Voltage vs. Temperature	Figure 14: Typical Recovery Current Vs. di_F/dt
	
Figure 15: Typical Recovery Current vs. di_F/dt	Figure 16: Typical Stored Charge vs. di_F/dt
	
Figure 17: Typical Stored Charge vs. di_F/dt	Figure 18: Maximum Avalanche Energy vs. Temperature



9.4Typical Characterisitics





Notes on Repetitive Avalanche Curves , Figures 14, 15:(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.

4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15). t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

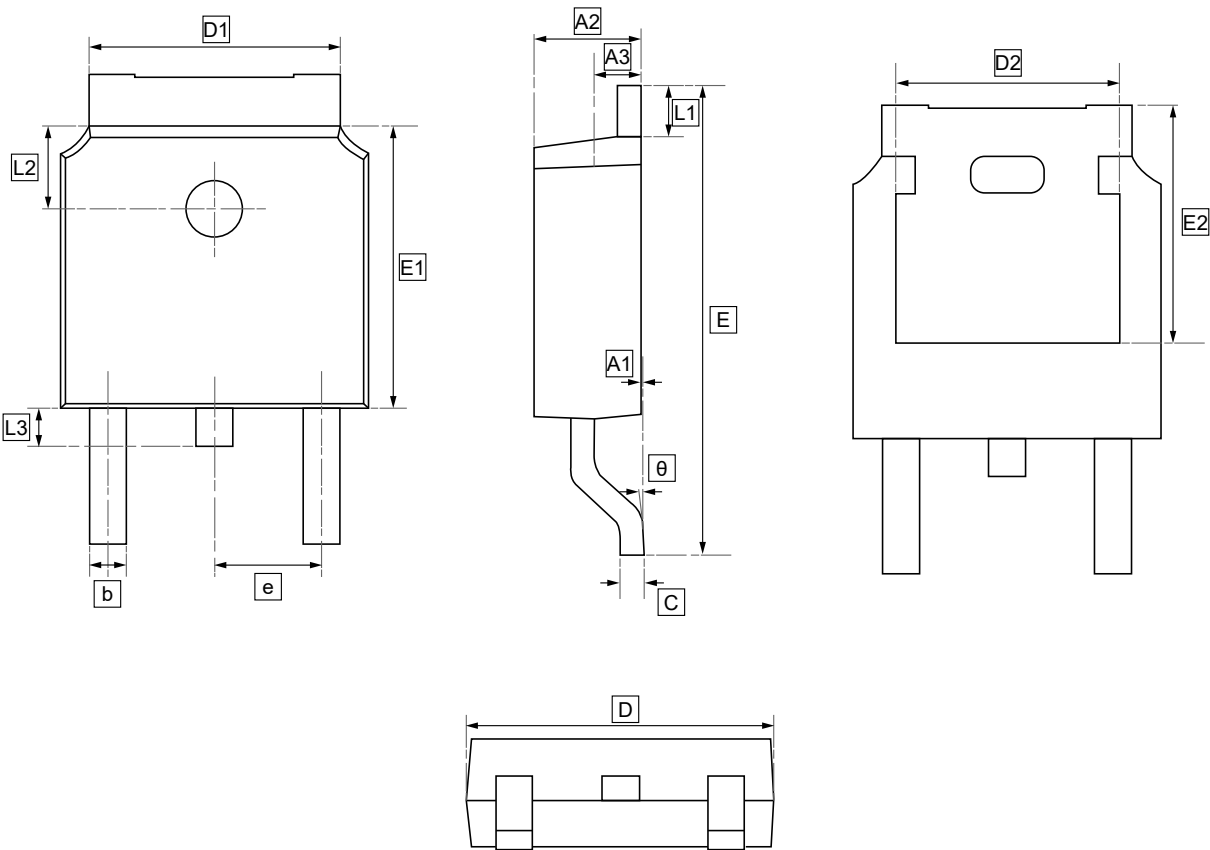
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



10.TO-252 Package Outline Dimensions

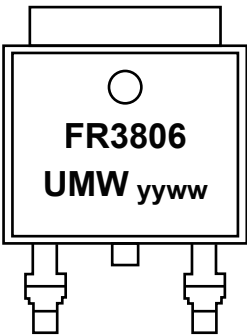


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286 BSC	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00



11.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFR3806TR	TO-252	2500	Tape and reel



12.Disclaimer

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