# I^2C-Compatible Serial E^2 PROM

Features

- Single Supply Voltage and High Speed Mode
  - Minimum operating voltage down to 1.7V
  - 400kHz/ 1MHz clock from 1.7V to 5.5V
- Low power CMOS technology
  - Read current 0.2mA (400kHz, typical)
  - Write current 0.8mA (400kHz, typical)
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Additional Write Lockable Pager
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - HBM: 4 kV
  - Latch up Capability: ±200 mA(25°C)
- Package: DIP-8, SOP-8, TSSOP-8, SOT-23-5,DFN-8, MSOP-8

DIP-8   SOP-8

MSOP-8   TSSOP-8

DFN-8 2*2/3*3   SOT-23-5
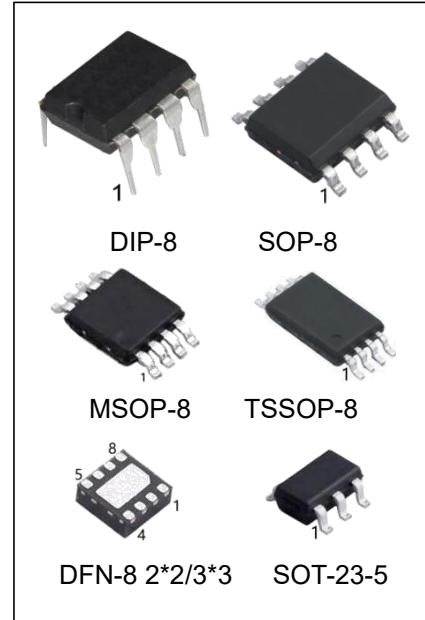
Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG24C08N	DIP-8	24C08	TUBE	2000pcs/box
HG24C08M/TR	SOP-8	24C08	REEL	2500pcs/reel
HG24C08MT/TR	TSSOP-8	24C08	REEL	2500pcs/reel
HG24C08MM/TR	MSOP-8	24C08	REEL	3000pcs/reel
HG24C08DQ3/TR	DFN-8 3*3	24C08	REEL	5000pcs/reel
HG24C08M5/TR	SOT-23-5	8CMU	REEL	3000pcs/reel
HG24C08DQ2/TR	DFN-8 2*2	24C08	REEL	4000pcs/reel
HG24C16N	DIP-8	24C16	TUBE	2000pcs/box
HG24C16M/TR	SOP-8	24C16	REEL	2500pcs/reel
HG24C16MT/TR	TSSOP-8	24C16	REEL	2500pcs/reel
HG24C16MM/TR	MSOP-8	24C16	REEL	3000pcs/reel
HG24C16DQ3/TR	DFN-8 3*3	24C16	REEL	5000pcs/reel
HG24C16M5/TR	SOT-23-5	ACMU	REEL	3000pcs/reel
HG24C16DQ2/TR	DFN-8 2*2	24C16	REEL	4000pcs/reel

1. General Description

The HG24C08/HG24C16 is I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 8 Kbits (1 Kbytes)/16 Kbits (2 Kbytes), which is 16 bytes per page.

Pin Configuration
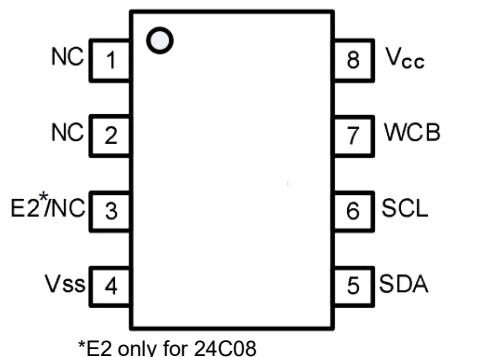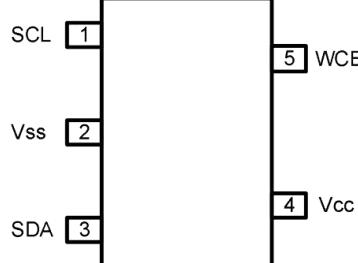
DIP-8/SOP-8/MSOP-8/TSSOP-8   SOT-23-5   DFN-8 3*3/DFN-8 2*2
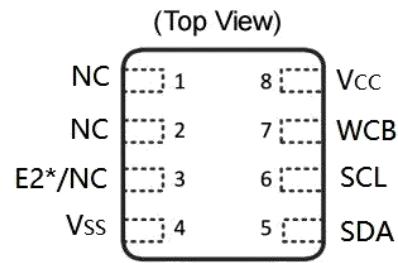
*E2 only for 24C08

Pin Definition

Table 1-1 Pin Definition for DIP8/SOP8/TSSOP8/DFN8/MSOP8 Packages

Pin		Name	Type	Description
24C08	24C16			
1	1	NC	/	
2	2	NC	/	
-	3	NC	/	
3	-	E2	Input	Slave Address Setting (only for 24C08)
4	4	Vss	Ground	Ground
5	5	SDA	I/O	Serial Data Input and Serial Data Output
6	6	SCL	Input	Serial Clock Input
7	7	WCB	Input	Write Control, Low Enable Write
8	8	VCC	Power	Power

Table 1-2 Pin Definition for SOT23-5 Packages

Pin	Name	Type	Description
1	SCL	Input	Serial Clock Input
2	Vss	Ground	Ground
3	SDA	I/O	Serial Data Input and Serial Data Output
4	VCC	Power	Power
5	WCB	Input	Write Control, Low Enable Write

Pin Descriptions

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-OR'ed with any number of other open-drain or open-collector devices.

Write Control (WCB): The Write Control input, when WCB is connected directly to VCC, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WCB pin will be internally pulled down to Vss.

Device Addresses (E2): The E2 pin is device address inputs. Typically, the E2 pin is for hardware addressing and a total of 2 devices can be connected on a single bus system. If these pins are left floating, the E2 pin will be internally pulled down to Vss, and the corresponding device address is fixed to 0.

Supply Voltage(V_{CC}): V_{CC} is the supply voltage.

Ground(Vss): Vss is the reference for the V_{CC} supply voltage.

2. Block Diagram
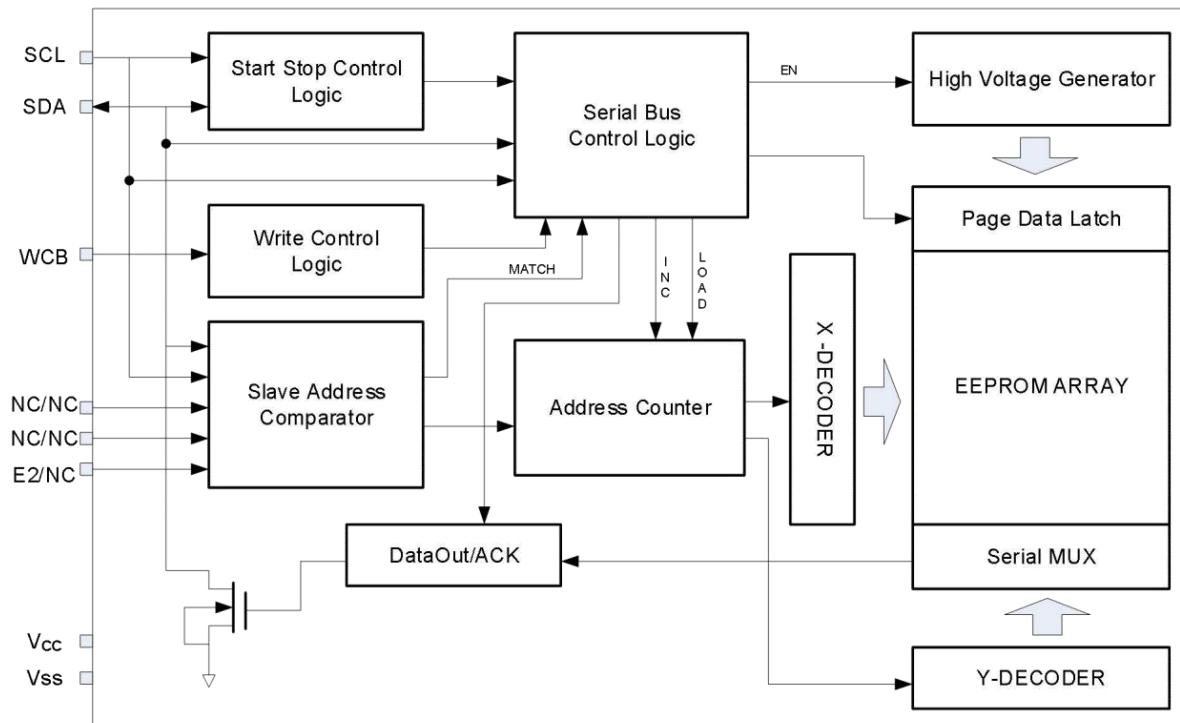
Figure 2-1 Block Diagram

3. Electrical Characteristics

Table 3-1 Absolute Maximum Ratings [1]

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-65	150	°C
T_A	Ambient operating temperature	-40	85	°C
V_{CC}	Supply Voltage	-0.5	6.5	V
V_{IO}	Input or output range	-0.5	6.5	V
I_{OL}	DC output current (SDA=0)	-	5	mA

Note: [1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

Table 3-2 Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$= Vss
C_{IN}	Input Capacitance (WCB, SCL)	6	pF	V_{IN}= Vss

Note: [1] Test Conditions: T_A = 25°C, f_{SCL} = 1MHz, Vcc = 5.0V.

Table 3-3 DC Characteristics （Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 85°C）

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{CC}	Supply Voltage	1.7	-	5.5	V	
		1.8	-	5.5	V	
		2.5	-	5.5	V	
I_{sb}	Standby Current	-	0.5	1.0	uA	Vcc = 1.7V
		-	0.8	2.0	uA	Vcc = 3.3V
		-	1.0	4.0	uA	Vcc = 5.5V
I_{CC1}	Supply Current	-	0.2	0.4	mA	Vcc=5.5V, Read at 400kHz
I_{CC2}	Supply Current	-	0.8	1.6	mA	Vcc=5.5V Write at 400kHz
I_{LI}	Input Leakage Current	-	0.10	1.0	µA	V_{IN} = V_{CC} or Vss
I_{LO}	Output Leakage Current	-	0.05	1.0	µA	V_{OUT} = V_{CC} or Vss
V_{IL}	Input Low Level	–0.5	-	$0.3V_{CC}$	V	
V_{IH}	Input High Level	$0.7V_{CC}$	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC} = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 0.15 mA
V_{OL2}	Output Low Level V_{CC} = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

Table 3-4 400kHz&1MHz AC Characteristics （Unless otherwise specified, V_{CC} = 1.7V to 5.5V, T_A = –40°C to 85°C, C_L=100pF, Test Conditions are listed in Notes [2] ）

Symbol	Parameter	1.7≤V_{CC}≤5.5 （400kHz）			1.7≤V_{CC}≤5.5 （1MHz）			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	µs
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	µs
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	µs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	µs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	µs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	µs
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	µs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	µs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	µs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	µs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	µs
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	µs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	µs
$t_{SU.WCB}$	WCB pin Setup Time	1.2	-	-	0.6	-	-	µs
$t_{HD.WCB}$	WCB pin Hold Time	1.2	-	-	0.6	-	-	µs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes: [1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

[3] RL (connects to V_{CC}): 1.3k (2.5V, 5.5V), 10k (1.7V)

- Input pulse voltages: 0.3 VCC to 0.7 VCC

- Input rise and fall times: ≤50ns

- Input and output timing reference voltages: 0.5VCC

Table 3-5 Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET[3]	Data retention	100			Years

Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C,3.3V, Page mode

[3] Test condition: T_A = 55°C
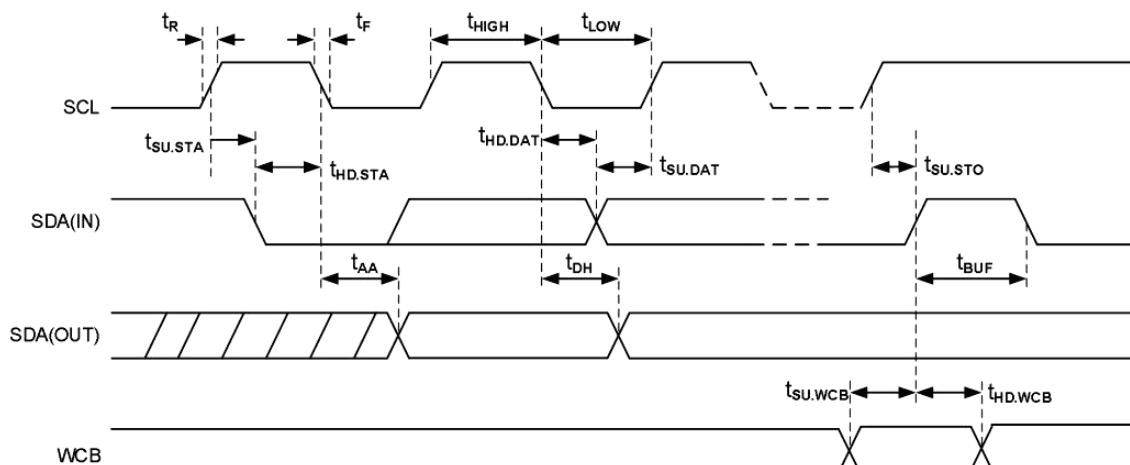
Figure 3-1 Bus Timing
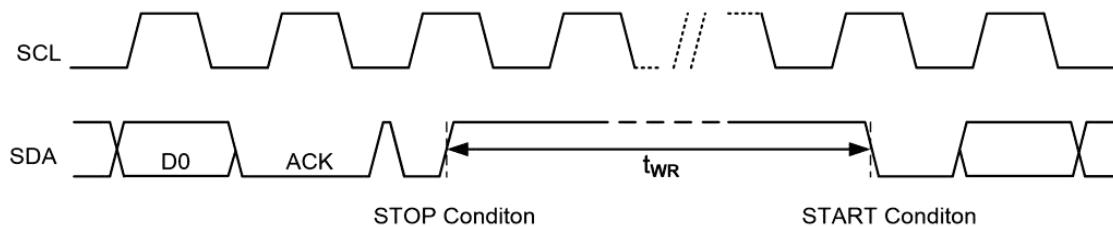
Figure 3-2 Write Cycle Timing

Note: [1] The write cycle time tWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Device Power-Up

The EEPROM has a built-in power-on-reset circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-reset circuit normally, the following conditions must be satisfied to raise the power supply voltage.

When initialization is successfully completed by the power-on-reset circuit, the EEPROM enters the standby status. tVSL is the time required to initialize the EEPROM. No instructions are accepted during this time.
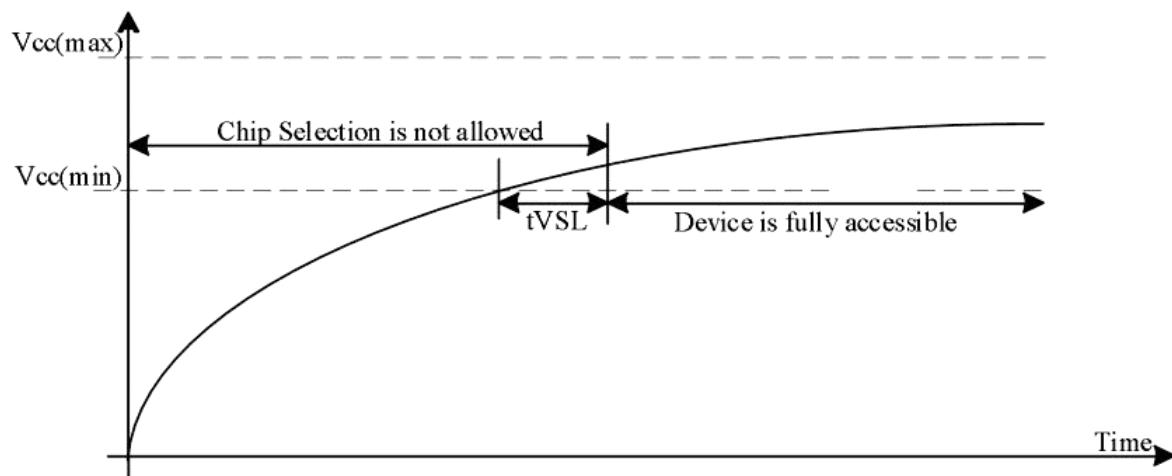
Figure 3-3 Power up Timing

Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of EEPROM device must below VPWD for at least tPWD timing. Please check the table below for more detail.
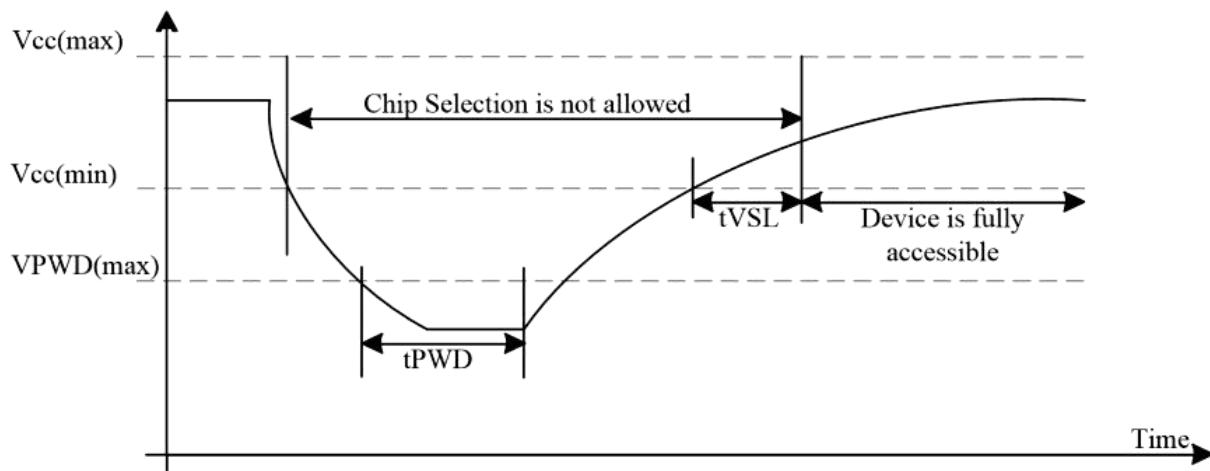
Figure 3-4 Power down-up Timing

Symbol	Parameter	min	max	unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.7	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	70		us
tVR	VCC Rise Time	1	500000	us/V

4. Device Operation

Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.
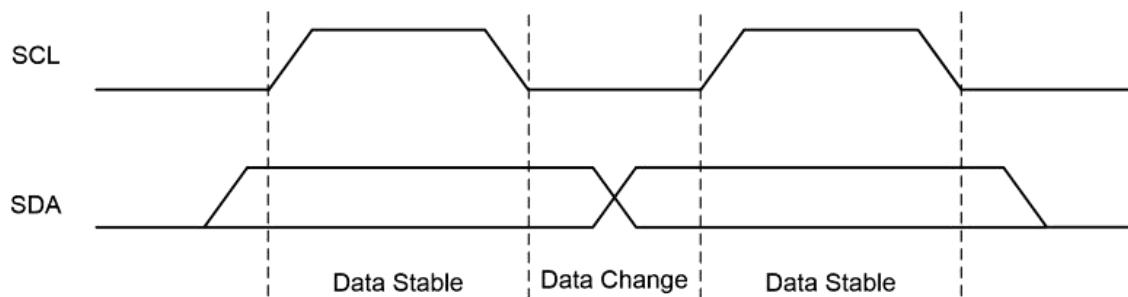
Figure 4-1 Data Validity

Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the HG24C08/HG24C16 in a standby mode (see Figure 4-2).
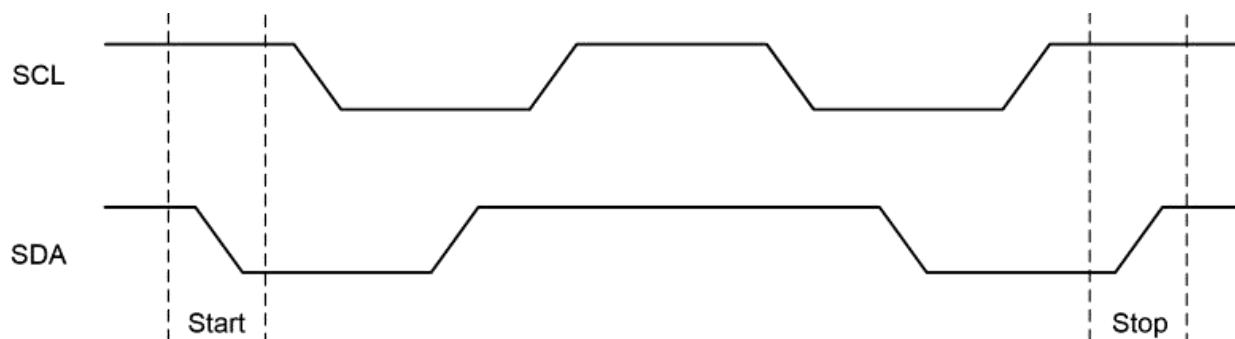

Figure 4-2 Start and Stop Definition

Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the HG24C08/HG24C16 in 8-bit words. The HG24C08/HG24C16 sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.
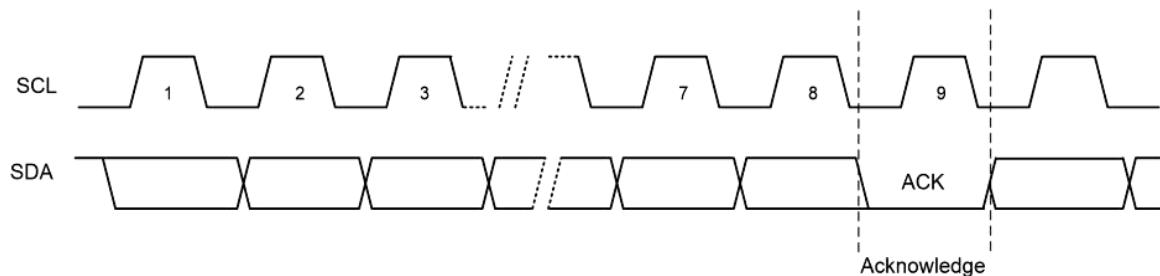
Figure 4-3 Output Acknowledge

Standby Mode

The HG24C08/HG24C16 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.
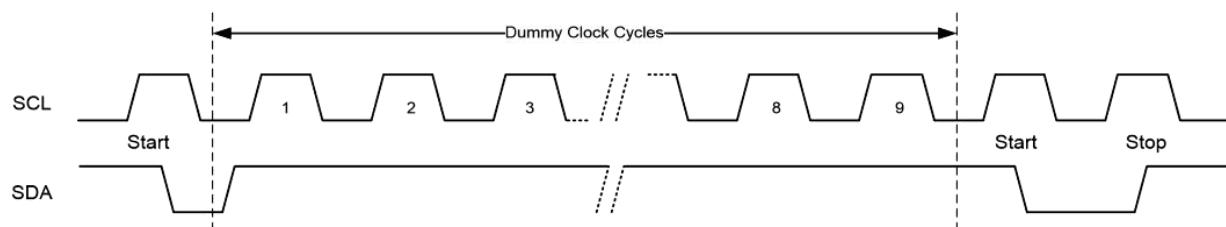
Figure 4-4 Soft Reset

Device Addressing

The HG24C08/HG24C16 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table below). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

Table 4-1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HG24C08	Normal Area	1	0	1	0	E2	A9	A8	R/W
	ID Page	1	0	1	1	E2	X	X	R/W
	Lock Bit	1	0	1	1	E2	X	X	R/W
	Serial Number	1	0	1	1	E2	X	X	1
HG24C16	Normal Area	1	0	1	0	A10	A9	A8	R/W
	ID Page	1	0	1	1	X	X	X	R/W
	Lock Bit	1	0	1	1	X	X	X	R/W
	Serial Number	1	0	1	1	X	X	X	1

Table 4-2 Word Address

Chip	Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HG24C08 HG24C16	Normal Area	A7	A6	A5	A4	A3	A2	A1	A0
	ID Page	0	0	X	X	A3	A2	A1	A0
	Lock Bit	X	1	X	X	X	X	X	X
	Serial Number	1	0	X	X	A3	A2	A1	A0

The E2 device address bits to allow as many as two devices on the same bus. These bits must compare to their corresponding hardwired input pins. The E2 pin uses an internal proprietary circuit that biases it to a logic low condition if the pin is floating. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

Data Security

The HG24C08/HG24C16 has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

5. Instructions

Write Operations

Byte Write

A write operation requires one 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the HG24C08/HG24C16 will again respond with a "0" and then clock in the first 8-bit data. Following receipt of the 8-bit data word, the HG24C08/HG24C16 will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the HG24C08/HG24C16 enters an internally timed write cycle, all inputs are disabled during this write cycle and the HG24C08/HG24C16 will not respond until the write is complete (see Figure 5-1).
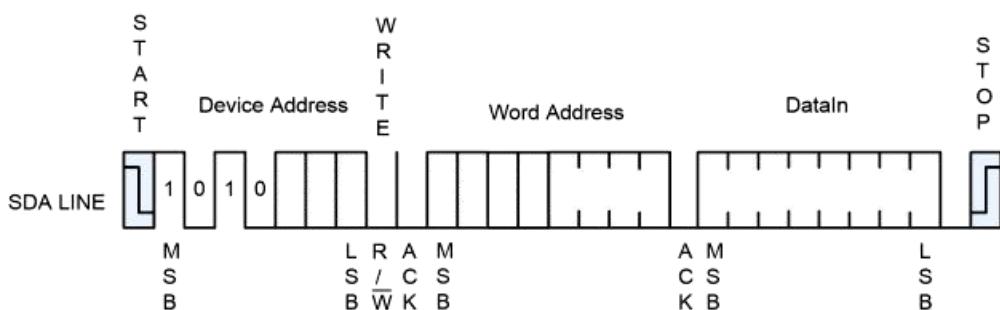

Figure 5-1 Byte Write

Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the HG24C08/HG24C16 acknowledges receipt of the first data word, the master can transmit more data words. The HG24C08/HG24C16 will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition.
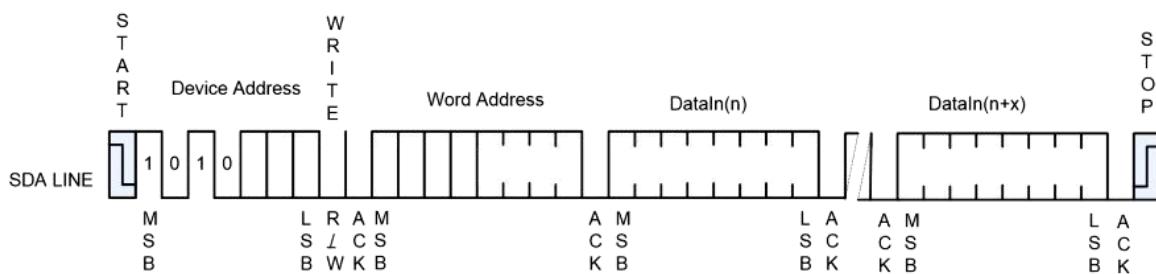
Figure 5-2 Page Write

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the HG24C08/HG24C16, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

Acknowledge Polling

Once the internally timed write cycle has started and the HG24C08/HG24C16 inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the HG24C08/HG24C16 respond with a "0", allowing the read or write sequence to continue.

Write Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

● Device type identifier = 1011b

● Address bit A7~A6 must be '00'.

● Address bits A3~A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

● Device type identifier = 1011b

● Address bit A6 must be '1'; all other address bits are don't care

● The data byte must be equal to the binary value xxxx xx1x, where x is don't care

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the HG24C08/HG24C16, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 5-3).
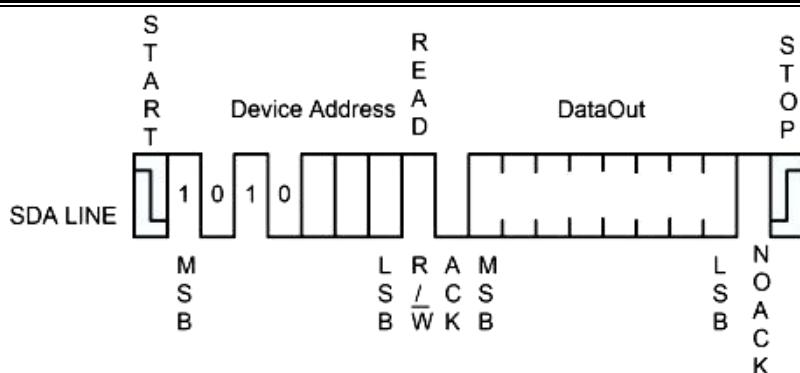
Figure 5-3 Current Address Read

Random Read

A Random Read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the HG24C08/HG24C16, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The HG24C08/HG24C16 acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-4).
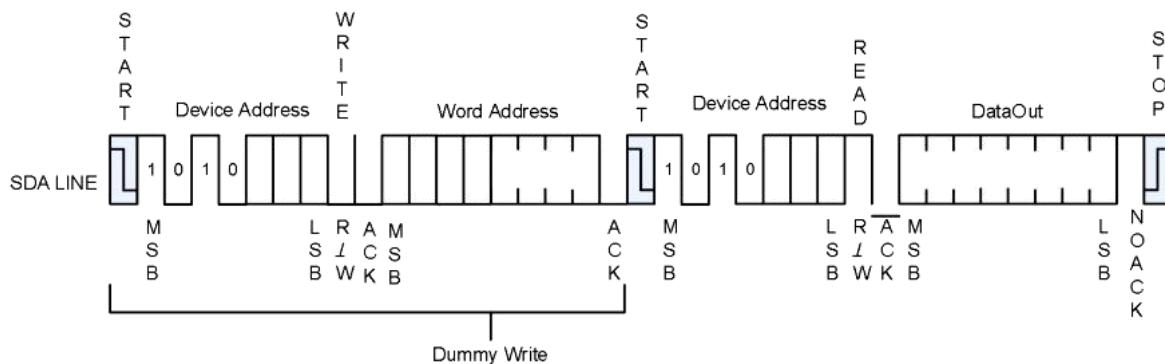
Figure 5-4 Random Read

Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the HG24C08/HG24C16 receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 5-5)
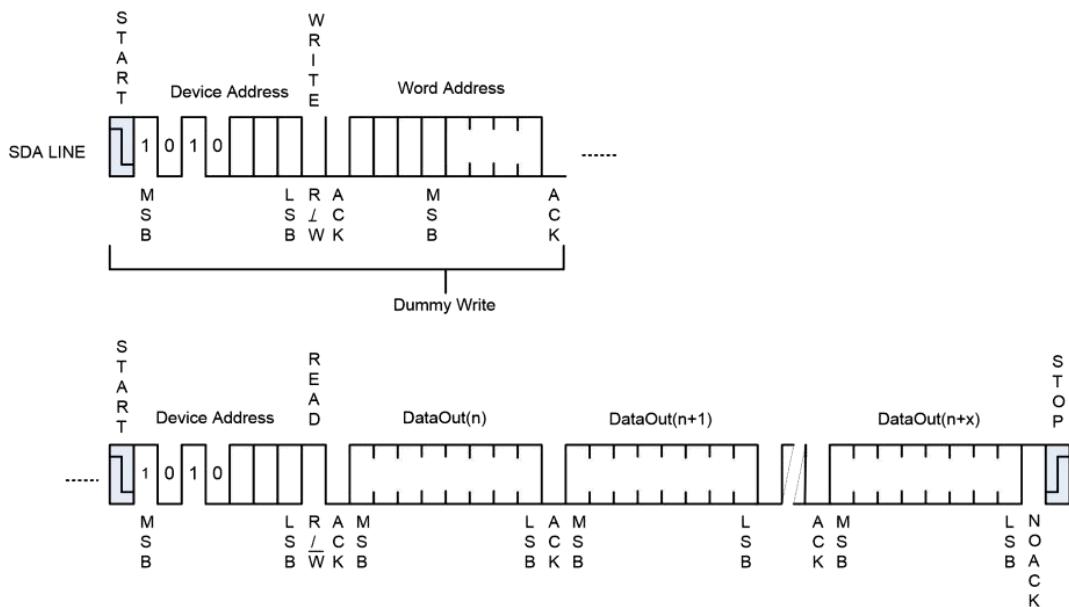
Figure 5-5 Sequential Read

Read Identification Page

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bit A7~A6 must be '00', and the LSB address bits A3~A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 6, as the ID page boundary is 16 bytes).

Read the Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.
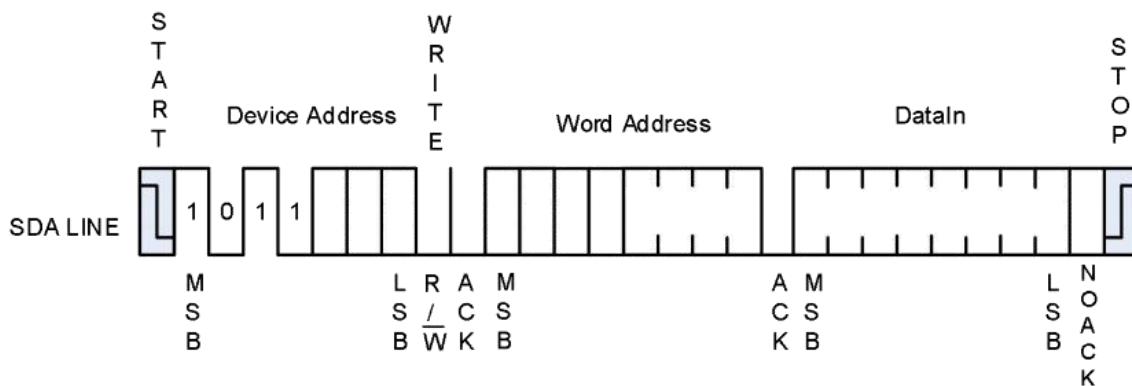
Figure 5-6 Lock Status Read (When Identification page locked, return NoACK after one data byte)

Serial Number Read

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 4-1, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a '10' sequence in bit A7 and A6 of the word address, regardless of the intended address as depicted in Table 4-2. If a word address other than '10' is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 5-7)
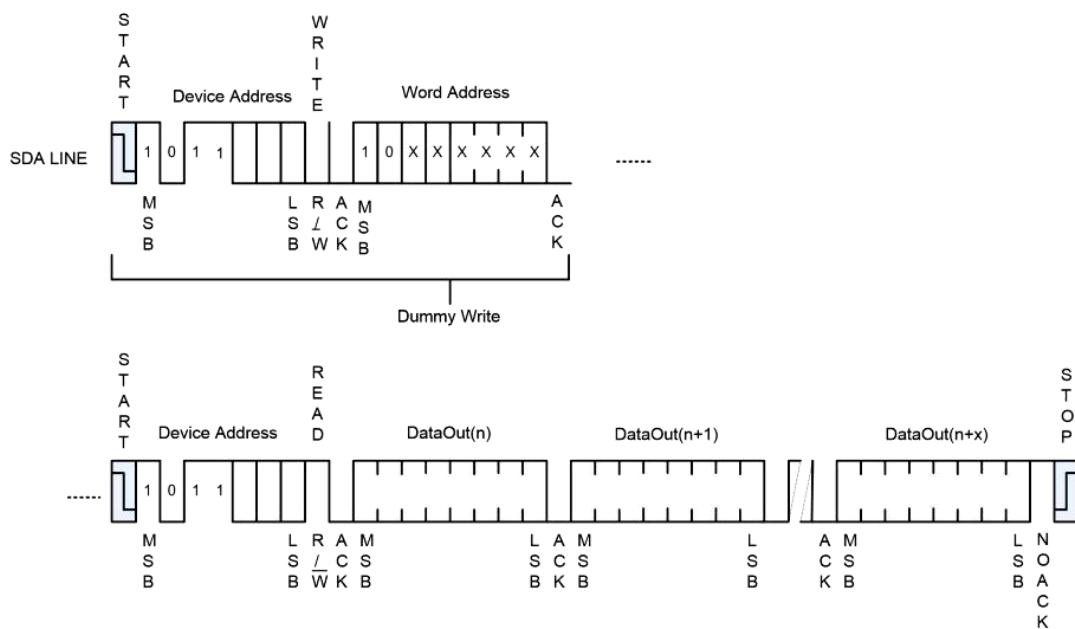

Figure 5-7 Serial Number Read

Physical Dimensions

DIP-8
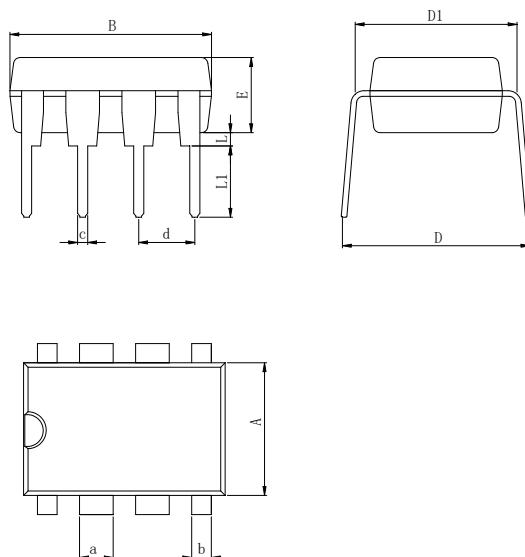
| Dimensions In Millimeters(DIP-8)										
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP-8
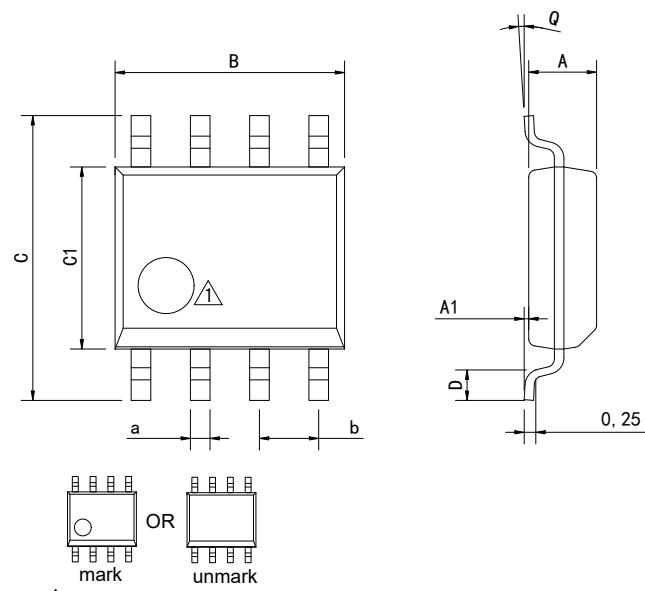
△ Package top mark may be in lower left corner or unmark

| Dimensions In Millimeters(SOP-8)								
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

MSOP-8
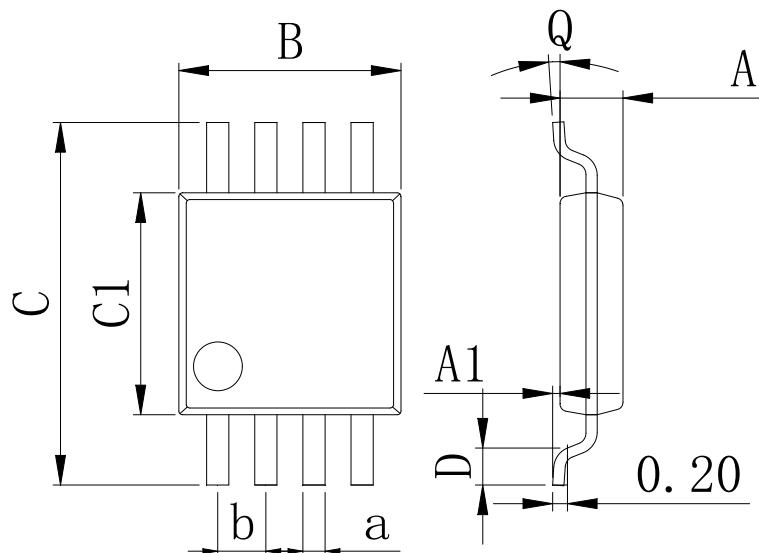
| Dimensions In Millimeters(MSOP-8)								
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

TSSOP-8 (4.4*3.0)
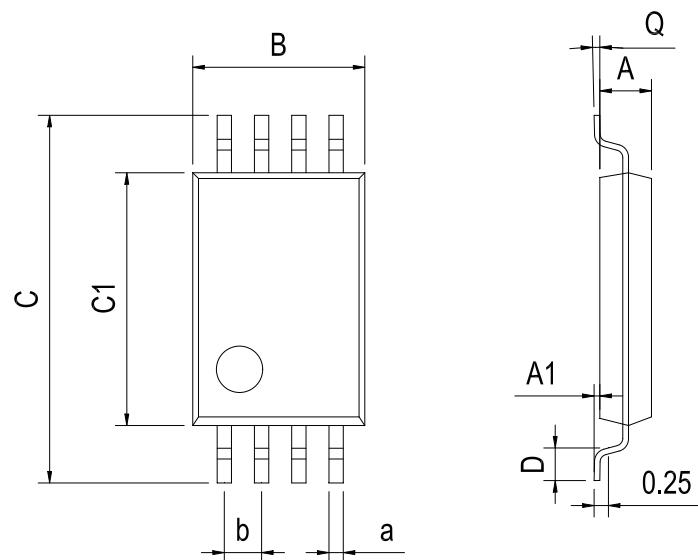
| Dimensions In Millimeters(TSSOP-8)								
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	2.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	3.10	6.60	4.50	0.80	8°	0.25	

Physical Dimensions

DFN-8 3*3
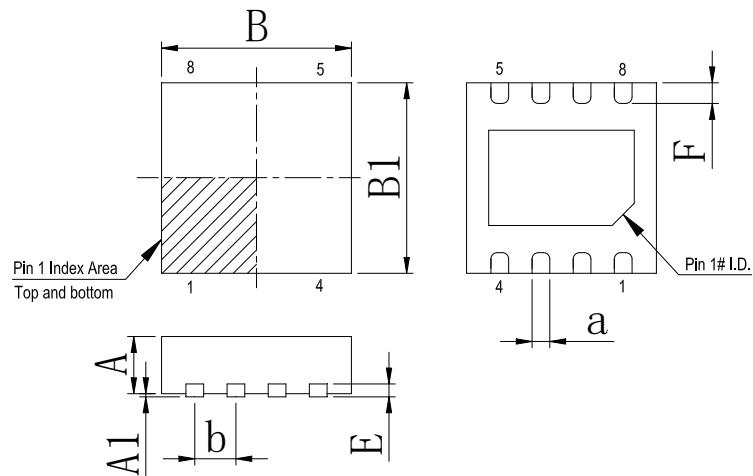
Dimensions In Millimeters(DFN-8 3*3)

Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65 BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

SOT-23-5
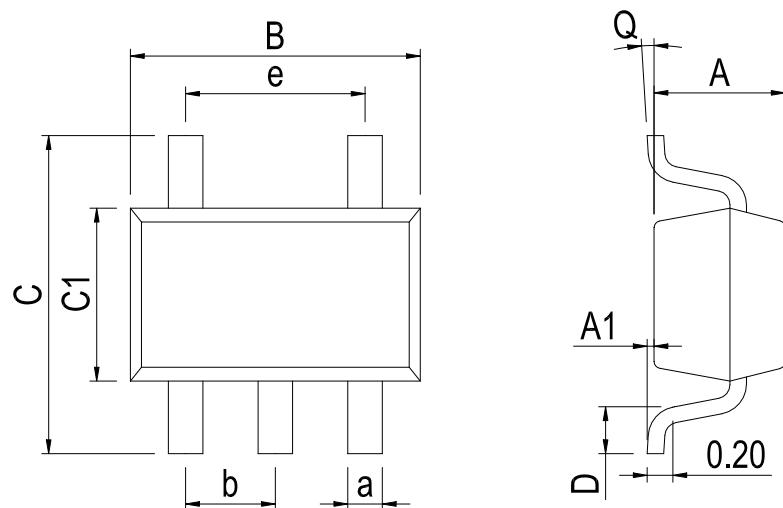
Dimensions In Millimeters(SOT-23-5)

Symbol:	A	A1	B	C	C1	D	Q	a	b	e
Min:	1.00	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95 BSC	1.90 BSC
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.50		

Physical Dimensions

DFN-8 2*2
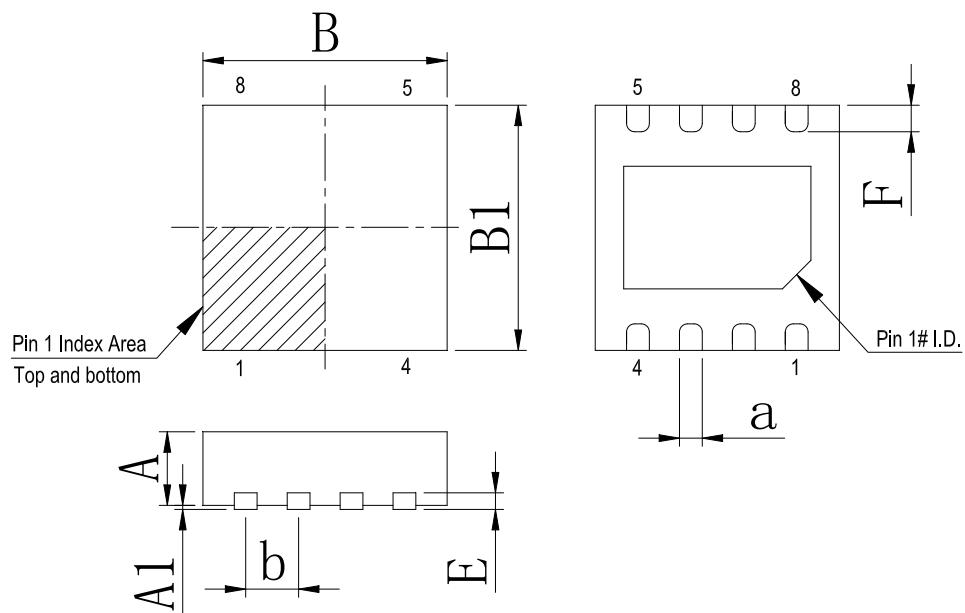
| Dimensions In Millimeters(DFN-8 2*2)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	1.90	1.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	2.10	2.10	0.25	0.45	0.30	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2020-3	New	1-21
V1.1	2025-10	Document Reformatting	1-21

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change products and services offered without prior notice. Customers should obtain the latest relevant information before placing orders and verify that such information is current and complete. Huaguan Semiconductor assumes no responsibility or liability for altered documents.

Customers are responsible for complying with safety standards and implementing safety measures when using Huaguan Semiconductor products in system design and end-product manufacturing. You assume full responsibility for: selecting the appropriate Huaguan Semiconductor products for your application; designing, validating, and testing your application; and ensuring that your application complies with applicable standards and all other safety, security, or other requirements. This is to prevent potential risks that may lead to personal injury or property damage.

Huaguan Semiconductor products are not approved for use in life support, military, aerospace, or other high-risk applications. Huaguan products are neither intended nor warranted for use in such systems or equipment. Any failure or malfunction may lead to personal injury or severe property damage. Such applications are deemed "Unsafe Use." Unsafe Use includes, but is not limited to: surgical and medical equipment, nuclear energy control equipment, aircraft or spacecraft instruments, control or operation of vehicle power, braking, or safety systems, traffic signal instruments, all types of safety devices, and any other applications intended to support or sustain life. Huaguan Semiconductor shall not be liable for consequences resulting from Unsafe Use in these fields. Users must independently evaluate and assume all risks. Any issues, liabilities, or losses arising from the use of products beyond their approved applications shall be solely borne by the user. Users may not claim any compensation from Huaguan Semiconductor based on these terms. If any third party claims against Huaguan Semiconductor due to such Unsafe Use, the user shall compensate Huaguan Semiconductor for all resulting damages and liabilities.

Huaguan Semiconductor provides technical and reliability data (including datasheets), design resources (including reference designs), application or other design advice, web tools, safety information, and other resources for its semiconductor products. However, no guarantee is made that these resources are free from defects, and no express or implied warranties are provided. The use of testing and other quality control techniques is limited to Huaguan Semiconductor's quality assurance scope. Not all parameters of each device are tested.

Huaguan Semiconductor's documentation authorizes you to use these resources only for developing applications related to the products described herein. You are not granted rights to any other intellectual property of Huaguan Semiconductor or any third party. Any other reproduction or display of these resources is strictly prohibited. You shall fully indemnify Huaguan Semiconductor and its agents against any claims, damages, costs, losses, and liabilities arising from your use of these resources. Huaguan Semiconductor shall not be held responsible.