UMW FDN5630

60V N-Channel MOSFET

1.Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers

2.Features

- $V_{DS(V)}$=60V
- I_D=1.9A
- $R_{DS(ON)}$<85mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<96mΩ(V_{GS}=4.5V)

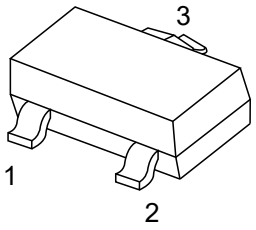
3.Applications

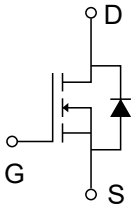
- Battery Switch
- DC/DC Converter

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





5.Maximum ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Ratings	Units
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current - Continuous	(Note 1a)	I_D	1.9	A
- Pulsed			10	A
Power Dissipation for Single Operation	(Note 1a)	P_D	0.5	W
	(Note 1b)		0.46	W
Operating and Storage Junction Temperature Range		T_J,T_{STG}	-55 to 150	°C

6.Thermal Characteristics

Parameter		Symbol	Ratings	Units
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	250	°C/W
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	75	°C/W

7.Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{DS}=0V, I_D=250μA	60			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D=250μA		55		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		3	V
Gate-Source Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
		V_{DS}=60V, V_{GS}=0V, T_J=55°C			10	
On-State Drain Current[a]	$I_{D(ON)}$	V_{DS}≥5V, V_{GS}=10V	8			A
Drain-Source On-State Resistance[a]	$R_{DS(ON)}$	V_{GS}=10V, I_D=1.9A		75	85	mΩ
		V_{GS}=4.5V, I_D=1.7A		86	96	
Forward Transconductance[a]	g_{FS}	V_{DS}=15V, I_D=1.9A		5		S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V, f=1MHz		180		pF
Output Capacitanc	C_{oss}			22		
Reverse Transfer Capacitance	C_{rss}			13		
Total Gate Charge	Q_g	V_{DS}=30V, V_{GS}=10V		4.2	6.1	nC
		I_D=1.9A		2.1	3.2	
Gate Source Charge	Q_{gs}	V_{DS}=30V, V_{GS}=4.5V		0.7		
Gate Drain Charge	Q_{gd}	I_D=1.9A		1		
Gate Resistance	R_g	f=1MHz	0.6	2.2	5.1	Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD} =30V, R_L=20Ω		4	6	ns
Rise Time	t_r	I_D=1.5A, V_{GEN}=10V		10	15	
Turn-Off DelayTime	$t_{D(off)}$	R_g=1Ω		10	15	
Fall Time	t_f			7	10.5	

Turn-On Delay Time	$t_{D(on)}$	V_{DD}=30V, R_L=20Ω I_D=1.5V,V_{GEN}=4.5V Rg=1Ω		15	23	ns
Rise Time	t_r			16	24	ns
Turn-Off Delay Time	$t_{D(off)}$			11	17	ns
Fall Time	t_f			11	17	ns
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C=25°C			2.19	A
Pulse Diode Forward Current [a]	I_{SM}				7	A
Body Diode Voltage	V_{SD}	I_S=1.5A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=1.5A, dI/dt=100A/μs T_J=25°C		15	23	ns
Body Diode Reverse Recovery Charge	Q_{rr}			10	15	nC
Reverse Recovery Fall Time	t_a			12		ns
Reverse Recovery Rise Time	t_b			3		ns

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

b. Guaranteed by design, not subject to production testing.

8.1Typical Characterisitics

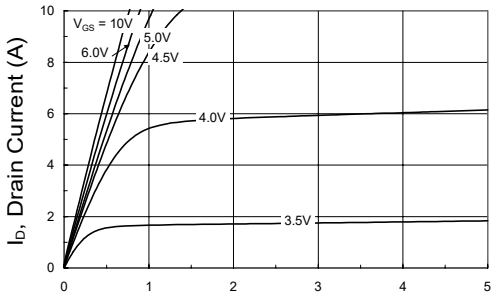


Figure 1. Output Characteristics

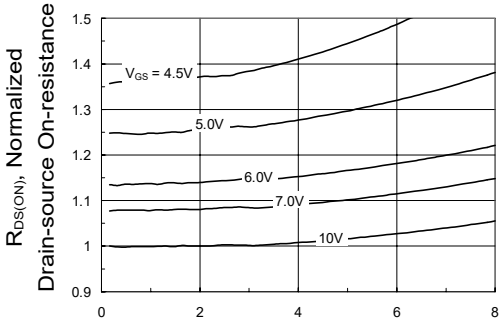


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

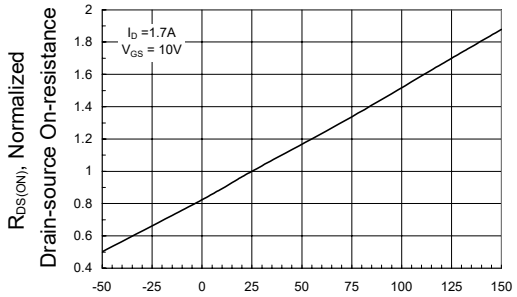


Figure 3. On-Resistance Variation with Temperature

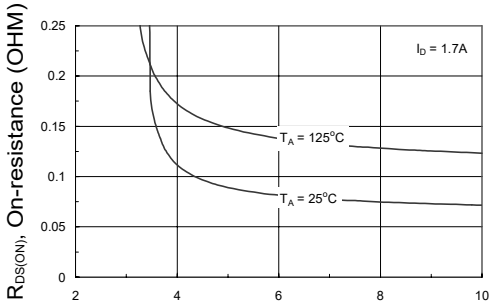


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

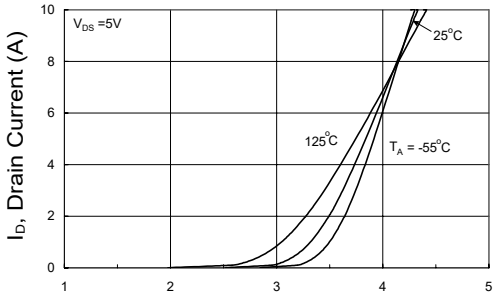


Figure 5. Transfer Characteristics

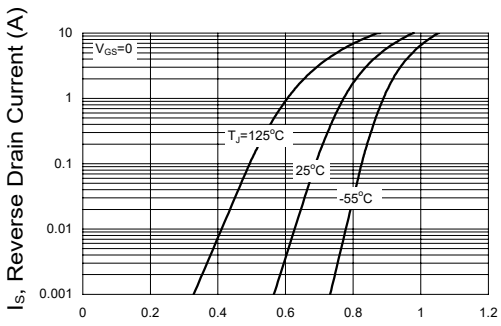
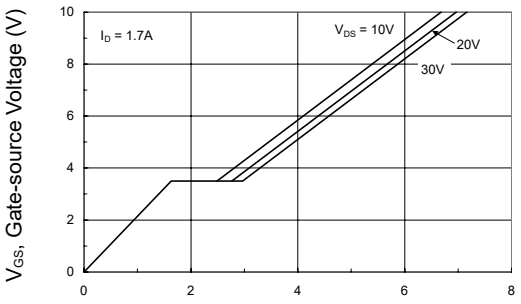


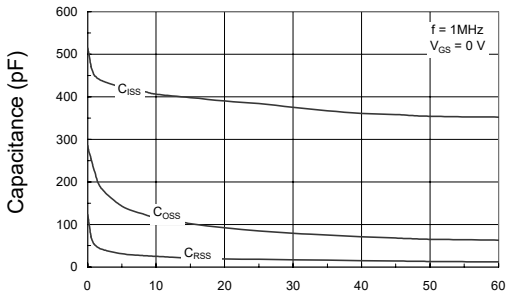
Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

8.2Typical Characterisitics



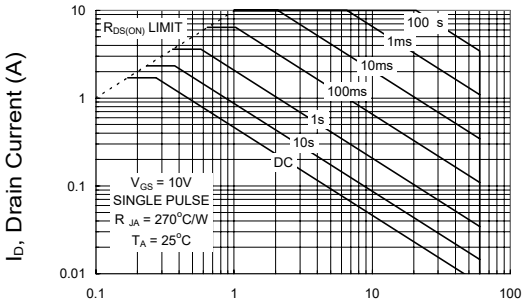
Q_g, Gate Charge (nC)

Figure 7. Gate Charge Characteristics



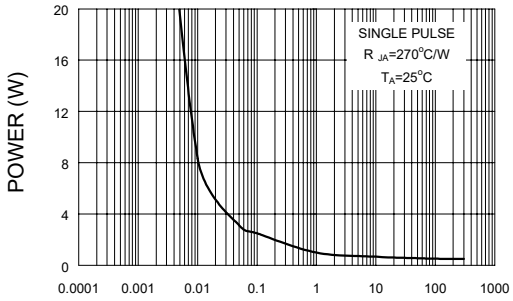
V_{DS}, Drain To Source Voltage (V)

Figure 8. Capacitance Characteristics



V_{DS}, Drain-source Voltage (V)

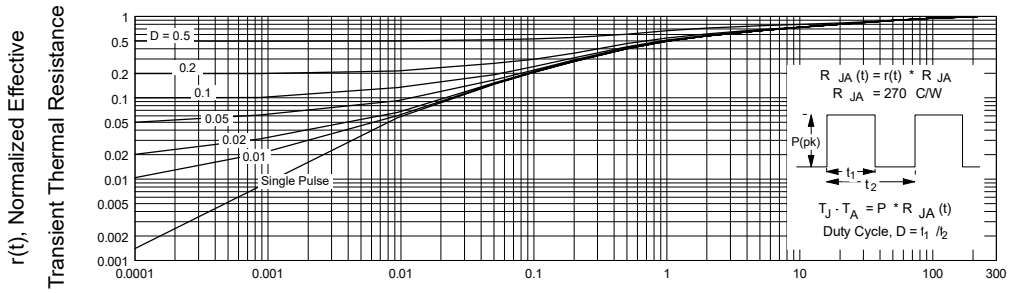
Figure 9. Maximum Safe Operating Area



Single Pulse Time (SEC)

Figure 10. Single Pulse Maximum Power Dissipation

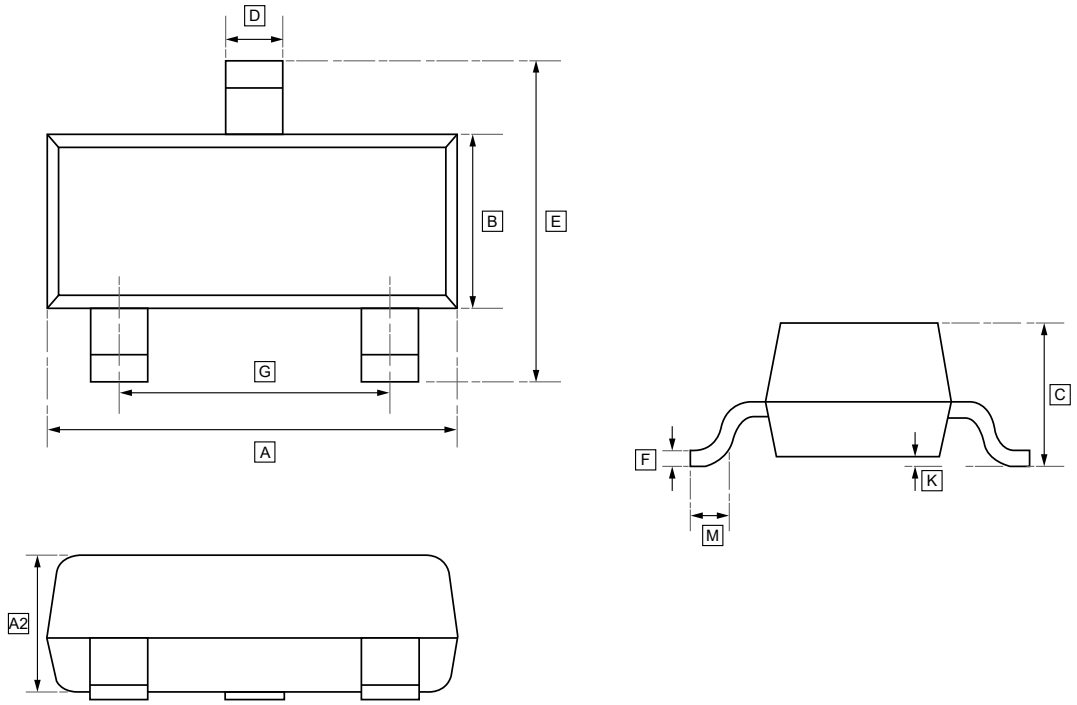
Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.



t_1, TIME (sec)

Figure 11. Transient Thermal Response Curve

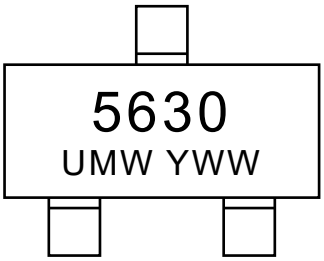
9.SOT-23 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	D	E	G	K	M	A2	F
Min	2.85	1.20	0.90	0.40	2.25	1.80	0.00	0.30	0.95	0.095
Max	3.04	1.40	1.10	0.50	2.55	2.00	0.10	-	1.05	0.115

10.Ordering information



YWW: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDN5630	SOT-23	3000	Tape and reel

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