UMW AOSP21321

-30V P-Channel MOSFET

1.Features

- V_{DS}=-30V
- I_D=-11A(V_{GS}=-10V)
- $R_{DS(ON)}$<17mΩ (V_{GS}=-10V)
- $R_{DS(ON)}$ <30mΩ(V_{GS}=-4.5V)

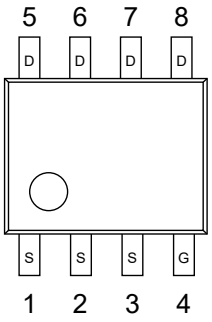
2.Description

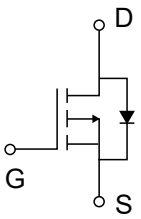
- Latest Advanced Trench Technology
- Low $R_{DS(ON)}$
- High Current Capability
- RoHS and Halogen-Free Compliant

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_A=25°C	I_D	-11	A
	T_A=70°C		-8.5	
Pulsed Drain Current [C]		I_{DM}	-56	
Avalanche Current [C]		I_{AS}	-33	A
Avalanche energy	L=0.1mH [C]	E_{AS}	54	mJ
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		59	75	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	°C/W

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±25V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.3	-1.8	-2.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-11A		14	17	mΩ
		T_J=125°C		20	24	mΩ
		V_{GS}=-4.5V, I_D=-8A		23.5	30	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-11A		42		S
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.7	-1	V
Maximum Body-Diode Continuous Current	I_S				-4	A
DYNAMIC PARAMETERS						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz		2050		pF
Output Capacitance	C_{oss}			330		pF
Reverse Transfer Capacitance	C_{rss}			300		pF
Gate resistance	R_g	f=1MHz		3.2	6.4	Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_g(-10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-11A		40	60	nC
Total Gate Charge	Q_g(-4.5V)			20	30	nC
Gate Source Charge	Q_{gs}			6		nC
Gate Drain Charge	Q_{gd}			10		nC

Turn-On DelayTime	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V R_L=1.05Ω,R_{GEN}=3Ω		11		ns
Turn-On Rise Time	t_r			10		ns
Turn-Off DelayTime	$t_{D(off)}$			40		ns
Turn-Off Fall Time	t_f			18		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F=-11A, dI/dt=500A/μs		14		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=-11A, dI/dt=500A/μs		25		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300ms pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

7.1Typical Characterisitics

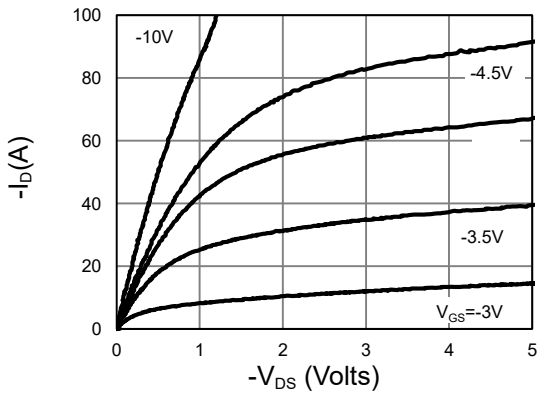


Fig 1: On-Region Characteristics (Note E)

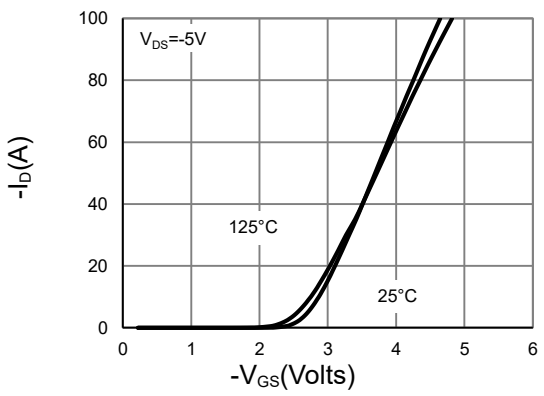


Figure 2: Transfer Characteristics (Note E)

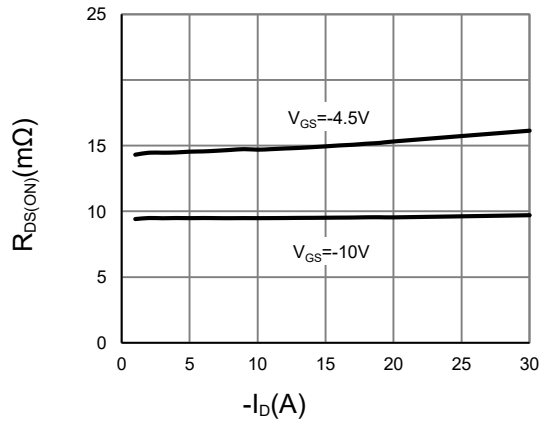


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

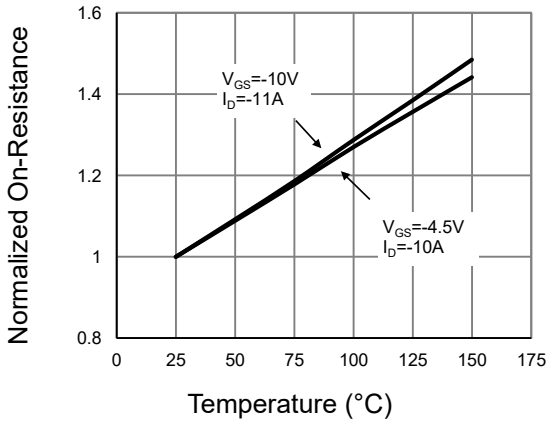


Figure 4: On-Resistance vs. Junction Temperature (Note E)

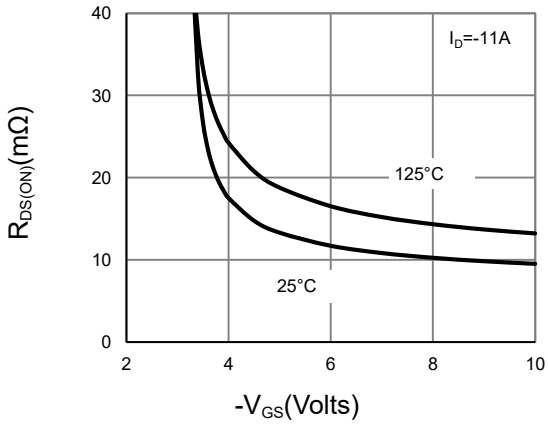


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

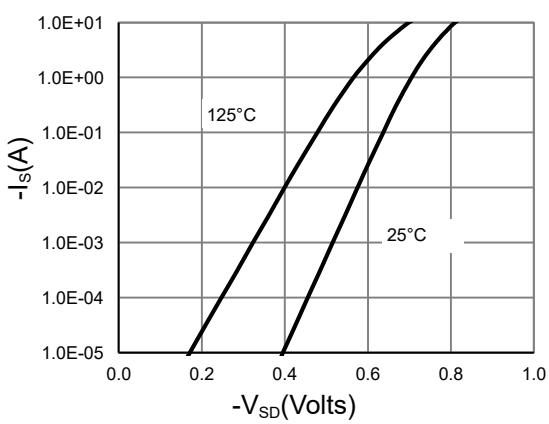


Figure 6: Body-Diode Characteristics(Note E)

7.2Typical Characterisitics

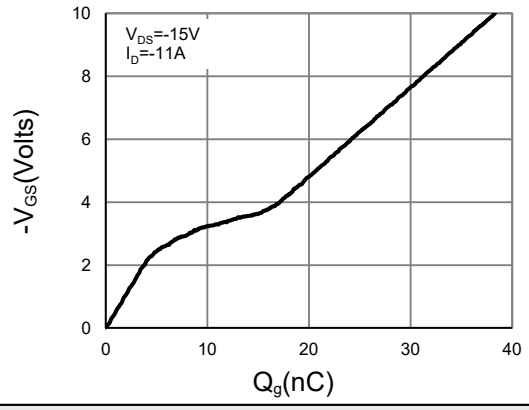


Figure 7: Gate-Charge Characteristics

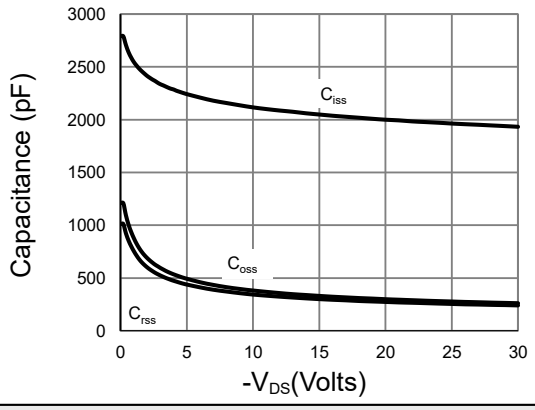


Figure 8: Capacitance Characteristics

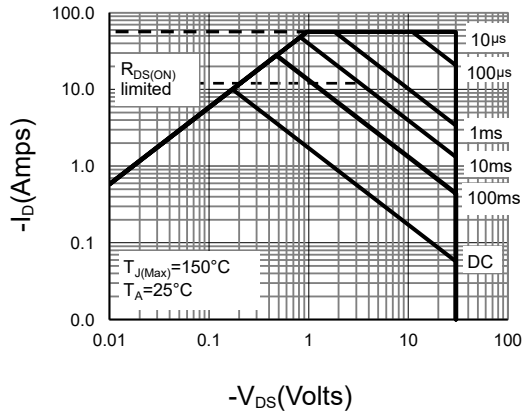


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

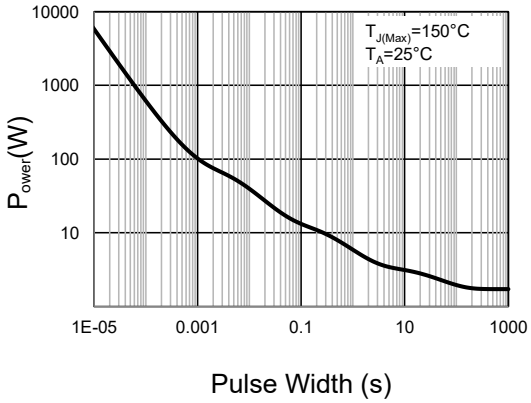


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

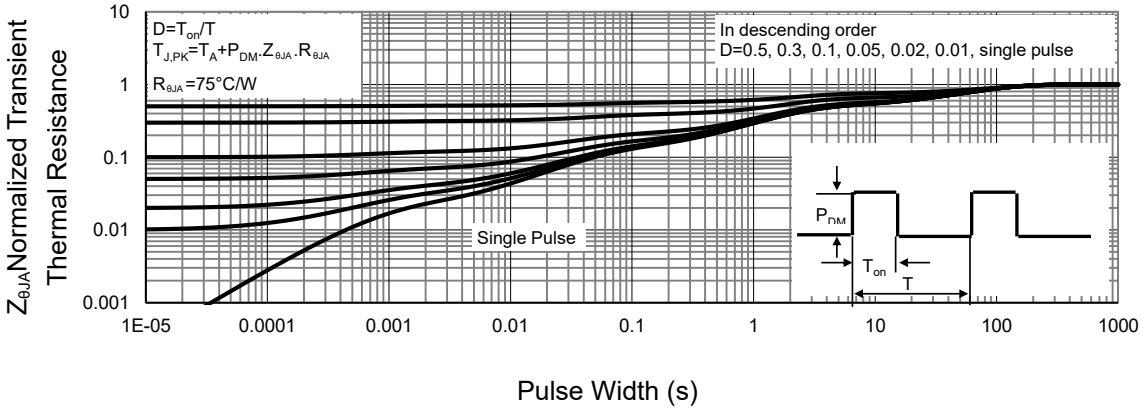
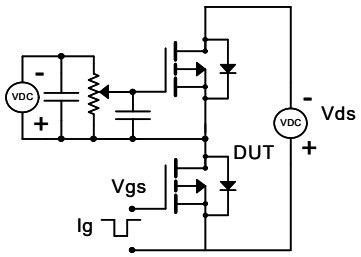
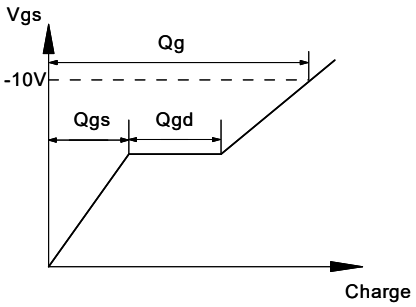


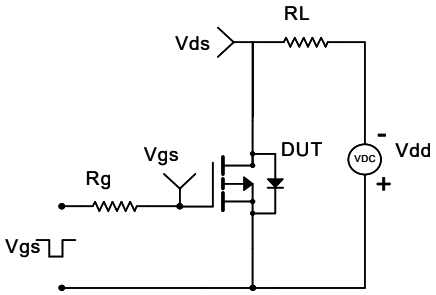
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

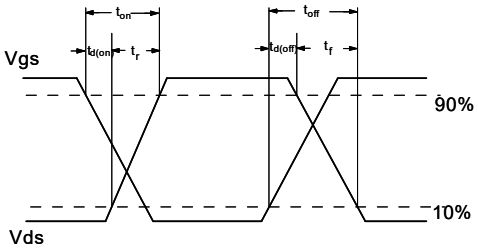
Gate Charge Test Circuit & Waveform



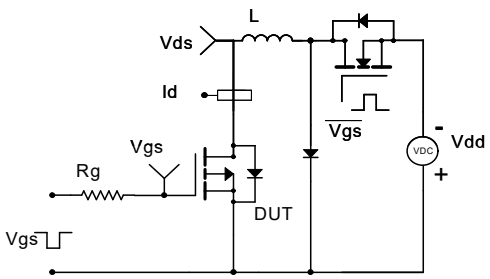


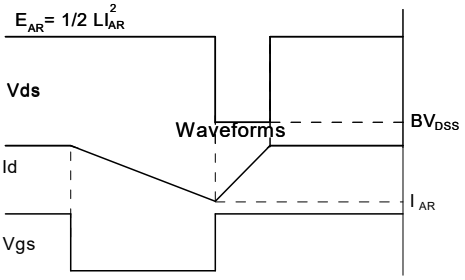
Resistive Switching Test Circuit & Waveforms



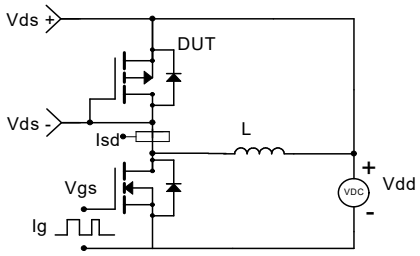


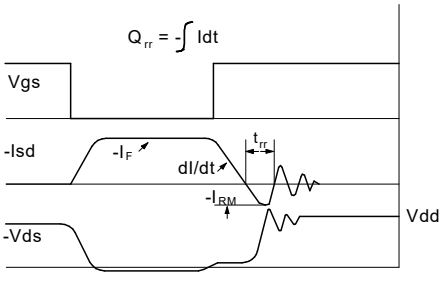
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



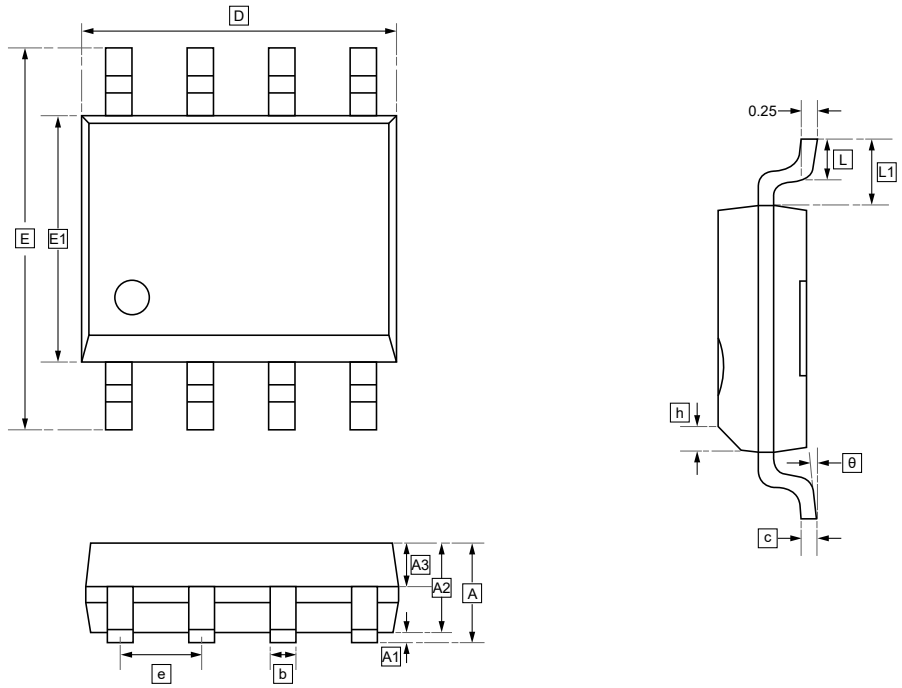


Diode Recovery Test Circuit & Waveforms





8.SOP-8 Package Outline Dimensions

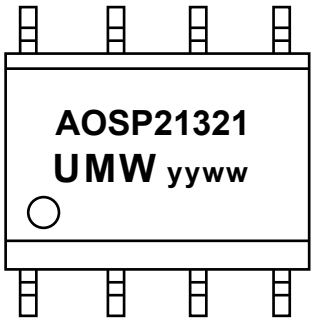


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AOSP21321	SOP-8	3000	Tape and reel

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