1.Description

The OPAx277 series of precision operational amplifiers replace the industry standard OP-177. The OPAx277 devices offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common□mode rejection, and high power supply rejection.

The OPAx277 operate from ±2-V to ±18-V supplies with excellent performance. Unlike most op amps that are specified at only one supply voltage,the OPAx277 series is specified for real-world applications; a single limit applies over the ±5-V (10-V) to ±15-V (30-V) supply range. High performance is maintained as the amplifiers swing to the specified limits. Because the initial offset voltage (±20 μV, maximum) is so low, user adjustment is usually not required. However, the single version (OPA277) provides external trim pins for special applications.

The OPAx277 are easy to use and free from phase inversion and the overload problems found in some other op amps. These devices are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

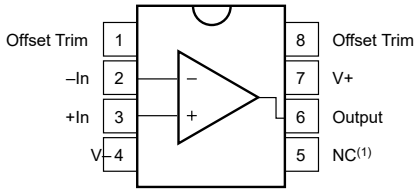
2.Features

- Ultra-low offset voltage: 10 μV
- Ultra-low drift: ±0.1 μV/°C
- High open-loop gain: 134 dB
- High common-mode rejection: 140 dB
- High power-supply rejection: 130 dB
- Low bias current: 1-nA maximum
- Wide supply range: ±2 V to ±18 V
- Low quiescent current: 800 μA/amplifier
- Single, dual, and quad versions
- Replaces OP-07, OP-77, and OP-177
- For similar performance with ±40-V overvoltage protection

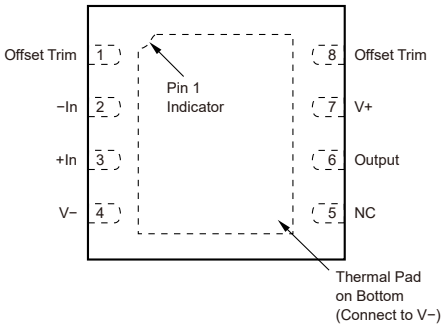
3.Applications

- Analog input module
- Weigh scale
- Temperature transmitter
- Pressure transmitter
- Data acquisition (DAQ)
- Lab and field instrumentation
- Battery test

4.1 Pinning Information (OPA277)



OPA277 P Package, 8-Pin PDIP and D Package, 8-Pin SOIC (Top View)

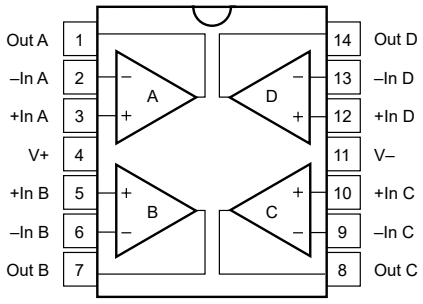


OPA277 DRM Package, 8-Pin VSON (Top View)

Pin Functions

Pin		Type	Description
Number	Name		
2	-In	Input	Inverting input
3	+In	Input	Noninverting input
5	NC	-	No internal connection (can be left floating)
1	Offset Trim	-	Input offset voltage trim (leave floating if not used)
8	Offset Trim	-	Input offset voltage trim (leave floating if not used)
6	Output	Output	Output
4	V-	-	Negative (lowest)power supply
7	V+	-	Positive (highest) power supply

4.2 Pinning Information (OPA4277)



OPA4277 P Package, 14-Pin PDIP and D Package
14-Pin SOIC (Top View)

Pin Functions

Pin		Type	Description
Number	Name		
2	-In A	Input	Inverting input channel A
6	-In B	Input	Inverting input channel B
9	-In C	Input	Inverting input channel C
13	-In D	Input	Inverting input channel D
3	+In A	Input	Noninverting input channel A
5	+In B	Input	Noninverting input channel B
10	+In C	Input	Noninverting input channel C
12	+In D	Input	Noninverting input channel D
1	Out A	Output	Output channel A
7	Out B	Output	Output channel B
8	Out C	Output	Output channel C
14	Out D	Output	Output channel D
4	V+	-	Positive (highest) power supply
11	V-	-	Negative (lowest) power supply

5.Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter	Symbol	Min	Max	Units
Supply voltage, V_S=(V+) – (V–)	V_S		36	V
Input voltage (2)		(V–) – 0.7	(V+) + 0.7	V
Output short circuit (3)	I_{SC}	Continuous		
Junction temperature	T_J		150	°C
Storage temperature	T_{STG}	-55	125	°C

Note:

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Limit input signals that can swing more than 0.7 V beyond the supply rails to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package.

6.Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Units
Supply voltage, V_S=(V+) – (V–)	Single supply	V_S	4	30	36	V
	Dual supply		±2	±15	±18	V
Ambient temperature		T_A	-40		85	°C

7.1 Thermal Information (OPA277)

Thermal Metric (1)	Symbol	SOP-8	Units
		8 Pins	
Junction-to-ambient thermal resistance	$R_{\theta JA}$	110.1	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	52.2	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	52.3	°C/W
Junction-to-top characterization parameter	ψ_{JT}	10.4	°C/W
Junction-to-board characterization parameter	ψ_{JB}	51.5	°C/W
Junction-to-case(bottom)thermal resistance	$R_{\theta JC(bot)}$	N/A	°C/W

7.2 Thermal Information (OPA4277)

Thermal Metric (1)	Symbol	SOP-14	Units
		14 Pins	
Junction-to-ambient thermal resistance	$R_{\theta JA}$	86.5	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	38.5	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	43.5	°C/W
Junction-to-top characterization parameter	ψ_{JT}	7.4	°C/W
Junction-to-board characterization parameter	ψ_{JB}	42.9	°C/W
Junction-to-case(bottom)thermal resistance	$R_{\theta JC(bot)}$	N/A	°C/W

8.Electrical Characteristics

At T_A=+25°C, V_S=10V to 30V, V_{CM}=V_{OUT}=V_S/2 and R_L=2kΩ, Connected to V_S/2 (unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input offset voltage	V_{OS}	OPA277			±10	±20	μV
		OPAx277UA			±20	±50	μV
		T_A=-40°C to 85°C	OPA277			±30	μV
			OPAx277UA			±100	μV
Input offset voltage drift	dV_{OS}/dT	T_A=-40°C to 85°C	OPA277		±0.1	±0.15	μV/°C
			OPAx277UA		±0.15	±1	μV/°C
Long-term drift					0.2		μV/mo
Power-supply rejection ratio	PSRR	V_S=±2V to ±18V	OPA277		±0.3	±0.5	μV/V
			OPAx277UA		±0.3	±1	μV/V
		V_S=±2V to ±18V T_A=-40°C to 85°C	OPA277			±0.5	μV/V
			OPAx277UA			±1	μV/V
Channel separation (dual, quad)		dc			0.1		μV/V
Input bias current	I_B	OPAx277UA			±0.5	±1	nA
		T_A=-40°C to 85°C	OPA277			±2	nA
			OPAx277UA			±4	nA
Input offset current	I_{OS}	OPAx277UA			±0.5	±1	nA
		T_A=-40°C to 85°C	OPA277			±2	nA
			OPAx277UA			±4	nA
Input voltage noise		f=0.1Hz to 10Hz			0.22		$μV_{PP}$
Input voltage noise density	e_n	f=10Hz			12		nV/√Hz
		f=100Hz			8		nV/√Hz
		f=1kHz			8		nV/√Hz
		f=10kHz			8		nV/√Hz
Input current noise density	i_n	f=1kHz			0.2		pA/√Hz
Common-mode voltage range	V_{CM}			(V-)+2		(V+)-2	V

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Common-mode rejection ratio	CMRR	V_{CM}=(V-)+2V to (V+)-2V	OPA277	130	140		dB
			OPAx277UA	115	140		dB
		V_{CM}=(V-)+2V to (V+)-2V T_A=-40°C to 85°C	OPA277	128			dB
			OPAx277UA	115			dB
Differential	Z_{ID}				100||3		MΩ||pF
Common-mode	Z_{IC}	V_{CM}=(V-)+2V to (V+)-2V			250||3		GΩ||pF
Open-loop voltage gain	A_{OL}	V_O=(V-)+0.5V to (V+)-1.2V, R_L=10kΩ			140		dB
		V_O=(V-)+1.5V to (V+)-1.5V		126	134		dB
		R_L=2Ω	T_A=-40°C to 85°C	126			dB
Gain-bandwidth product	GBW				1		MHz
Slew rate	SR				0.8		V/μs
Settling time	t_s	V_S=±15V, G=1,10V phase step	Reaches 0.1%		14		μs
			Reaches 0.01%		16		μs
Overload recovery time	t_{OR}	V_{IN} × G=V_S			3		μs
Total harmonic distortion+noise		G=1, f=1kHz, V_O=3.5V_{RMS}			0.002		%
Voltage output	V_O	R_L=10kΩ		(V-)+0.5		(V+)-1.2	V
			T_A=-40°C to 85°C	(V-)+0.5		(V+)-1.2	V
		R_L=2kΩ		(V-)+1.5		(V+)-1.5	V
			T_A=-40°C to 85°C	(V-)+1.5		(V+)-1.5	V
Short-circuit current	I_{SC}				±35		mA
Capacitive load drive	C_L						
Open-loop output impedance	Z_O	f=1MHz			40		Ω
Quiescent current per amplifier	I_Q	I_O=0A			±790	±825	μA
			T_A=-40°C to 85°C			±900	μA

9.1 Typical Characteristic

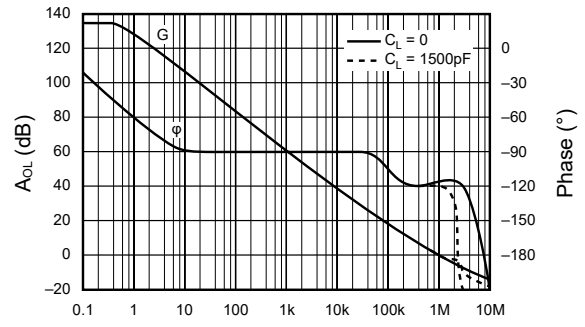


Figure 1: Open-Loop Gain and Phase vs Frequency

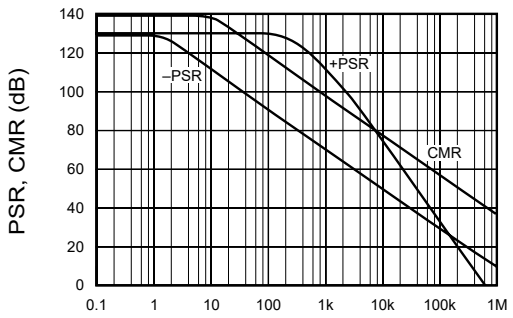


Figure 2: Power Supply and Common-Mode Rejection vs Frequency

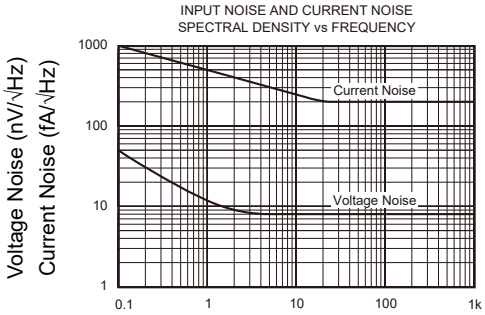


Figure 3: Input Noise and Current Noise Spectral Density vs Frequency

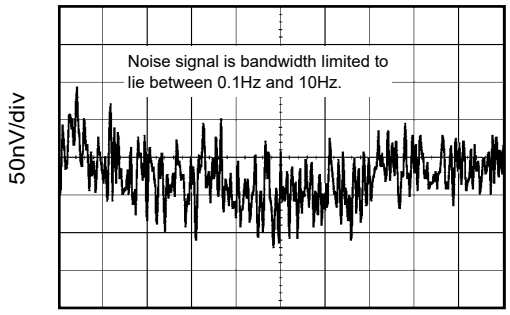


Figure 4: Input Noise Voltage vs Time

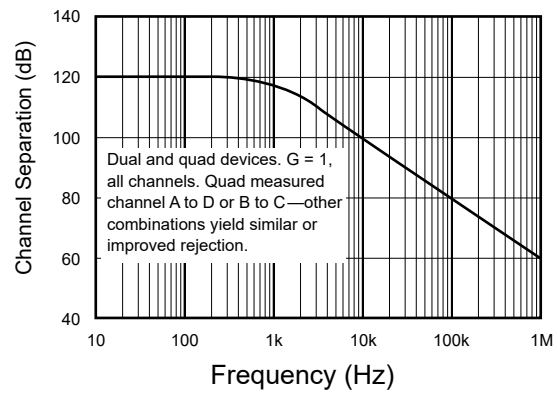


Figure 5: Input Noise and Current Noise Spectral Density vs Frequency

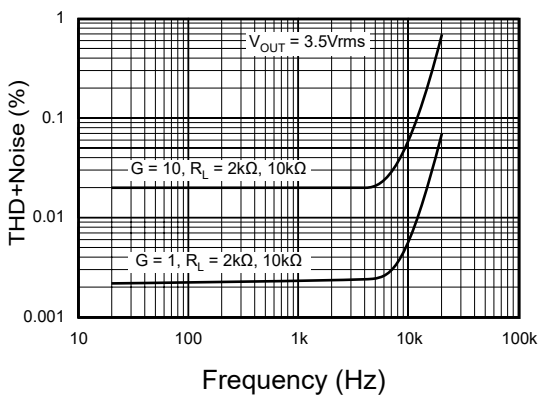


Figure 6: Total Harmonic Distortion + Noise vs Frequency

9.2 Typical Characteristic

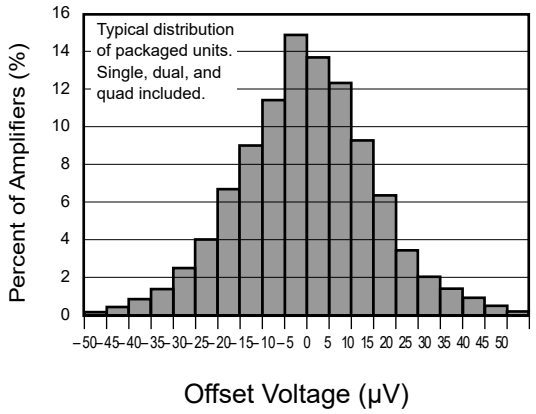


Figure 7: Offset Voltage Production Distribution

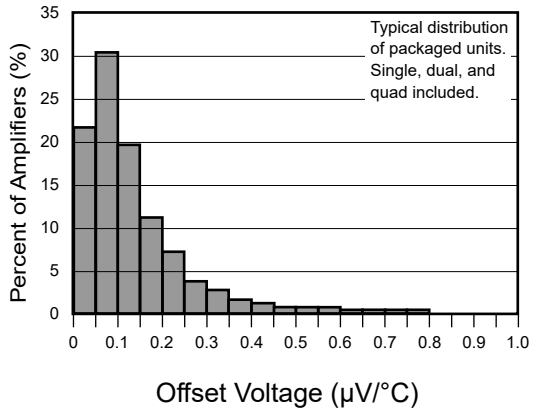


Figure 8: Offset Voltage Drift Production Distribution

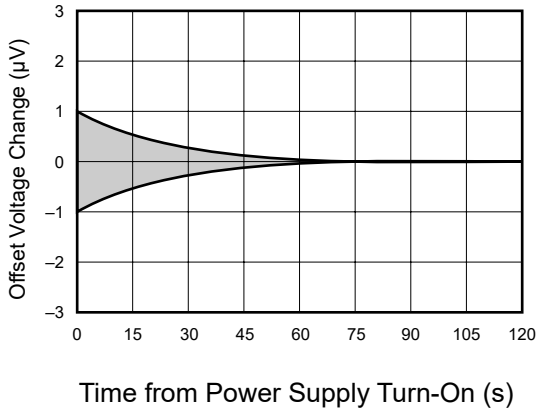


Figure 9: Warm-Up Offset Voltage Drift

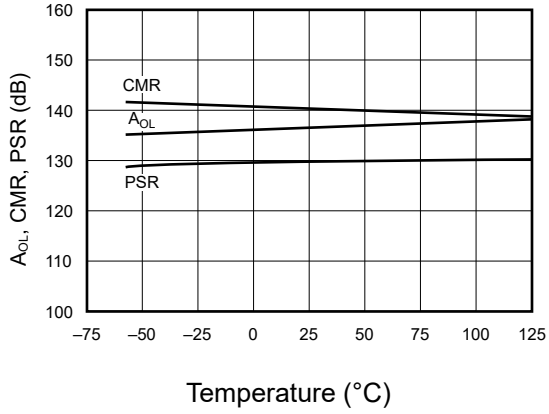


Figure 10: A_{OL}, CMR, PSR vs Temperature

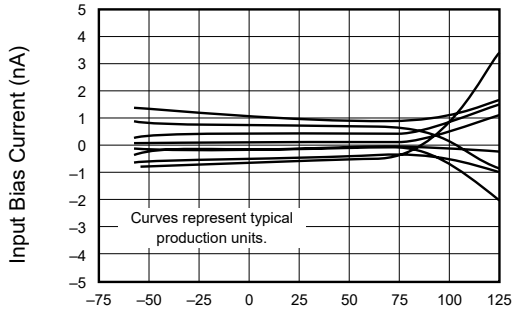


Figure 11: Input Bias Current vs Temperature

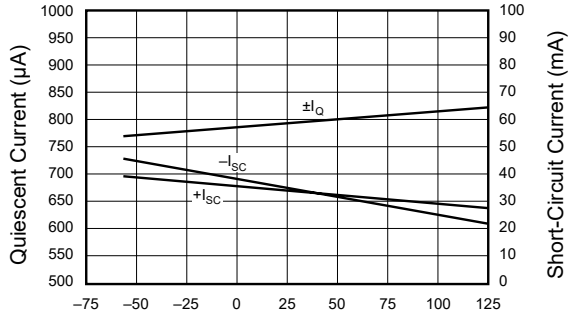


Figure 12: Quiescent Current and Short-Circuit Current vs Temperature

9.3 Typical Characteristic

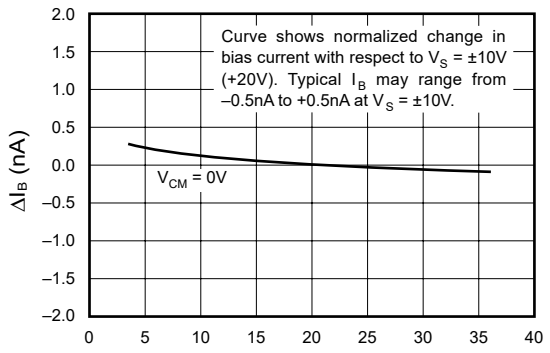


Figure 13: Change in Input Bias Current vs Power-Supply Voltage

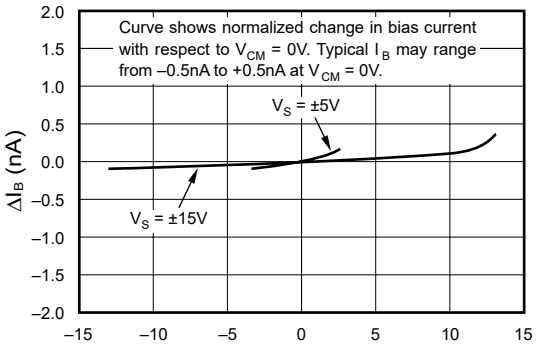


Figure 14: Change in Input Bias Current vs Common-Mode Voltage

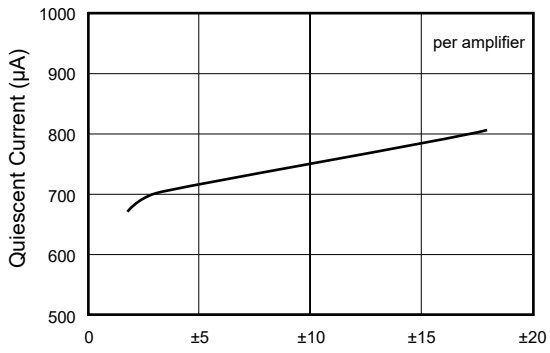


Figure 15: Quiescent Current vs Supply Voltage

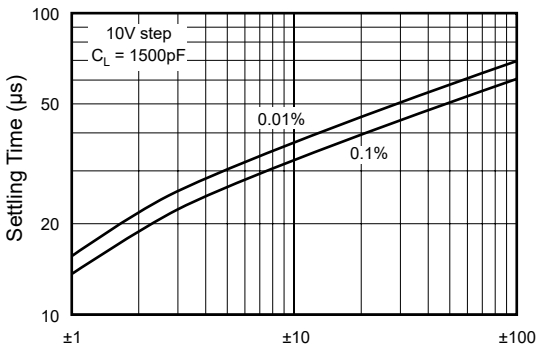


Figure 16: Settling Time vs Closed-Loop Gain

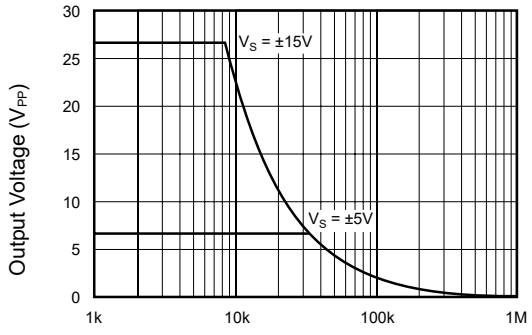


Figure 17: Maximum Output Voltage vs Frequency

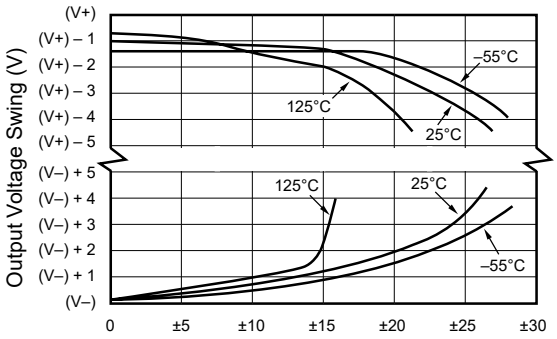
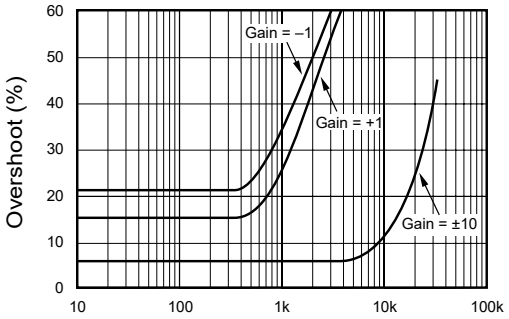


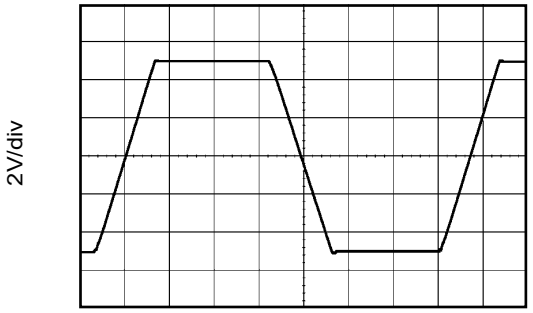
Figure 18: Output Voltage Swing vs Output Current

9.4 Typical Characteristic



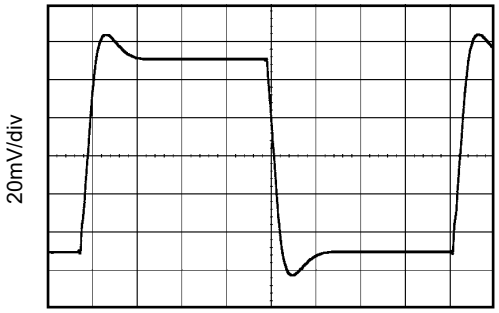
Load Capacitance (pF)

Figure 19: Small-Signal Overshoot vs Load Capacitance



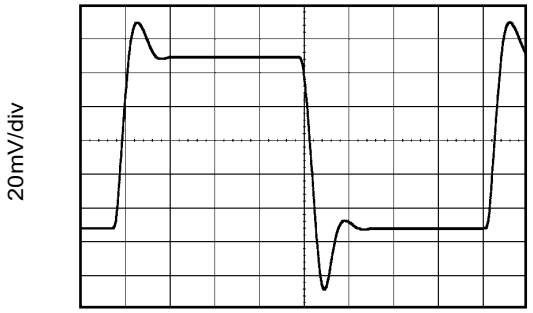
10μs/div, G=1, C_L=1500pF, V_S=±15V

Figure 20: Large-Signal Step Response



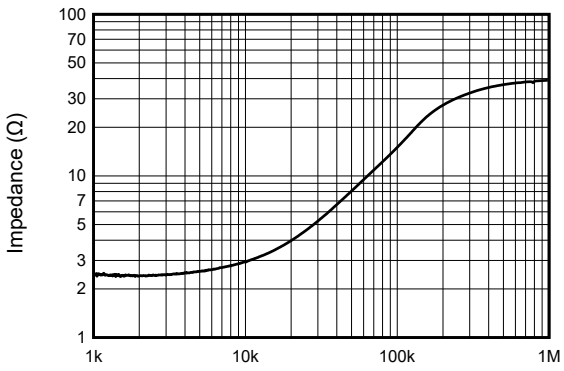
1μs/div, G=1, C_L= 0, V_S=±15V

Figure 21: Small-Signal Step Response



1s/div, G=1, C_L=1500pF, V_S=±15V

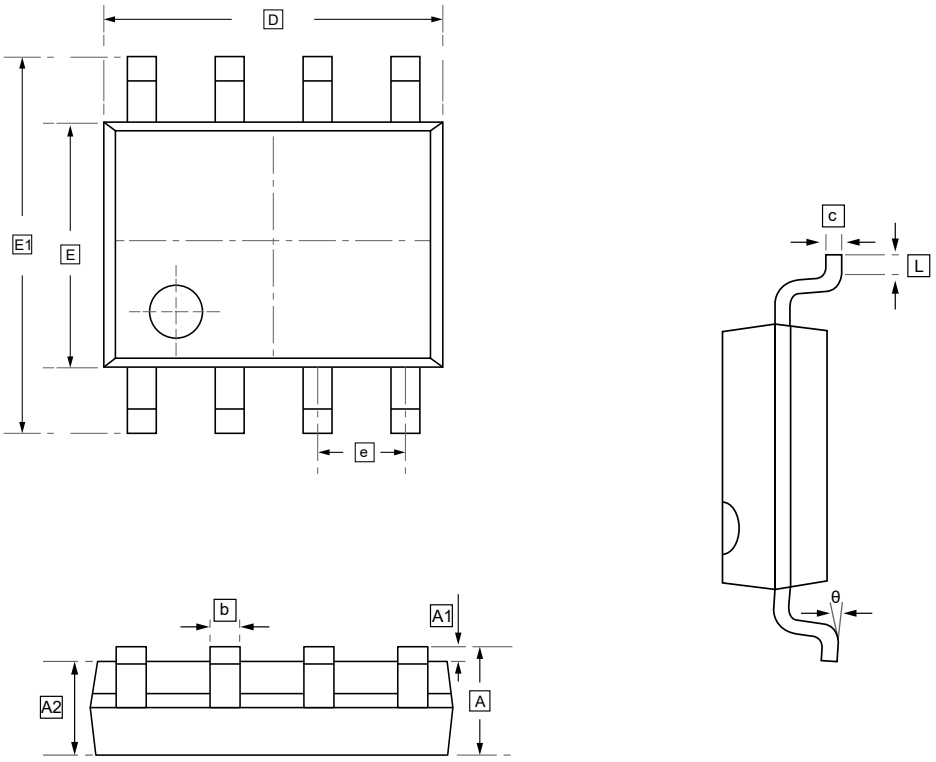
Figure 22: Small-Signal Step Response



Frequency (Hz), V_S=±15V

Figure 23: Open-Loop Output Impedance

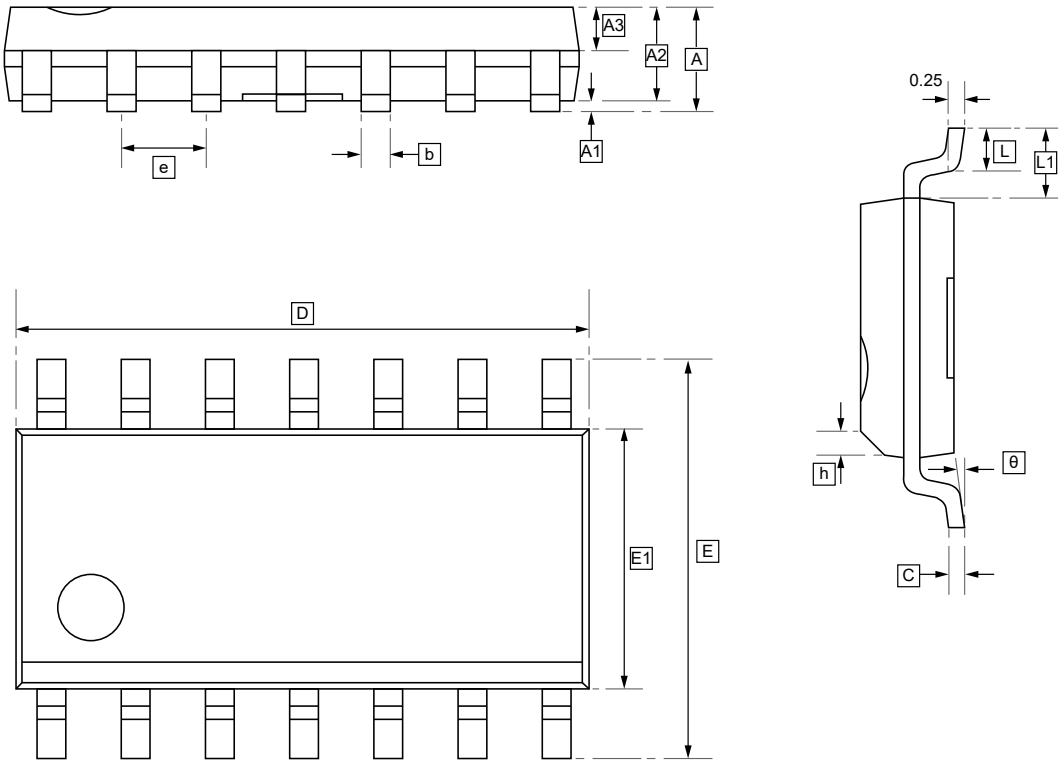
10.1 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

10.2 SOP-14 Package Outline Dimensions

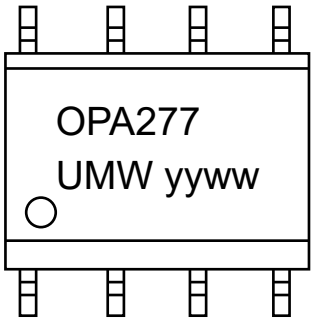


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	C	D	E	E1	e	h	L
Min	-	0.05	1.35	0.65	0.203	0.17	8.45	5.80	3.80	1.24	0.25	0.40
Max	1.75	0.25	1.55	0.75	0.305	0.25	8.85	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

11.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW OPA277UA	OPA277	SOP-8	2500	Tape and reel
UMW OPA4277UA	OPA4277	SOP-14	2500	Tape and reel

12.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.