UMW IRFR7546TR

60V N-Channel MOSFET

1.Features

- $V_{DS(V)}$=60V
- I_D=71A
- $R_{DS(ON)}$<7.9mΩ(V_{GS}=5V)

2.1Applications

- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits

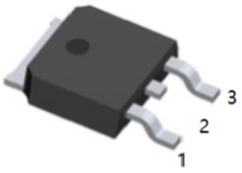
2.2Applications

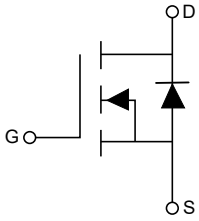
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters

3.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view





4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS} @ 10V(Silicon Limited)	T_C=25°C	I_D	71 ①	A
Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	T_C=100°C		50 ①	A
Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	T_C=25°C		56	A
Pulsed Drain Current ②		I_{DM}	280	A
Maximum Power Dissipation	T_C=25°C	P_D	99	W
Linear Derating Factor			0.66	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Operating Junction andStorage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)			300	°C

Single Pulse Avalanche Energy ③	$E_{AS(Thermally\ limited)}$	120	mJ
Single Pulse Avalanche Energy ⑨	$E_{AS(Thermally\ limited)}$	178	mJ
Avalanche Current ②	I_{AR}	See Fig 21,17, 23a, 23b	A
Repetitive Avalanche Energy ②	E_{AR}		mJ
Junction-to-Case ⑧	$R_{\theta JC}$	1.52	°C/W
Junction-to-Ambient (PCB Mount)	$R_{\theta JA}$	50	°C/W
Junction-to-Ambient	$R_{\theta JA}$	100	°C/W

5.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	60			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=1mA, Reference to 25°C		47		mV/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=43A		6.6	7.9	mΩ
		V_{GS}=6V, I_D=21A		8.5		mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=100μA	2.1		3.7	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
		V_{DS}=60V, V_{GS}=0V, T_J=125°C			150	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=20V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-20V			-100	nA
Gate Resistance	R_g			1.5		Ω
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=43A	56			S
Total Gate Charge	Q_g	I_D=43A, V_{DS}=30V, V_{GS}=10V		58	87	nC
Gate-to-Source Charge	Q_{gs}			14		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			18		nC
Total Gate Charge Sync.(Q_g-Q_{gd})	Q_{sync}			26		nC
Tum-On Delay Time	$t_{D(on)}$	V_{DD}=30V, I_D=43A R_G=2.7Ω, V_{GS}=10V ⑤		8.1		ns
Rise Time	t_r			28		ns
Turn-Off Delay Time	$t_{D(off)}$			36		ns
Fall Time	t_f			20		ns
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V See Fig. 7, f=1MHz		3020		pF
Output Capacitance	C_{oss}			280		pF
Reverse Transfer Capacitance	C_{rss}			180		pF
Effective Output Capacitance (Energy Related)	C_{oss}eff.(ER)	V_{GS}=0V, V_{DS}=0V to 48V ⑦		290		pF
Effective Output Capacitance (Time Related)	C_{oss}eff.(TR)	V_{GS}=0V, V_{DS}=0V to 48V ⑥		370		pF

Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			71①	A
Pulsed Source Current (Body Diode) ②	I_{SM}				280	A
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=43A,V_{GS}=0V ⑤			1.2	V
Peak Diode Recovery dv/dt	dv/dt	T_J=175°C,I_S=43A,V_{GS}=60V ④		12		V/ns
Reverse Recovery Time	t_{rr}	T_J=25°C, V_{DD}=51V		26		ns
		T_J=125°C, I_F=43A		29		ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, di/dt=100A/μs ⑤		22		nC
		T_J=125°C		30		nC
Reverse Recovery Current	I_{RRM}	T_J=25°C		1.5		A

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140).

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L =130μH, R_G = 50Ω, I_{AS} = 43A, V_{GS} =10V.

④ I_{SD} ≤ 43A, di/dt ≤ 1020A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

⑨ Limited by TJmax starting T_J = 25°C, L= 1mH, R_G = 50Ω, I_{AS} = 19A, V_{GS} =10V.

6.1Typical Characterisitics

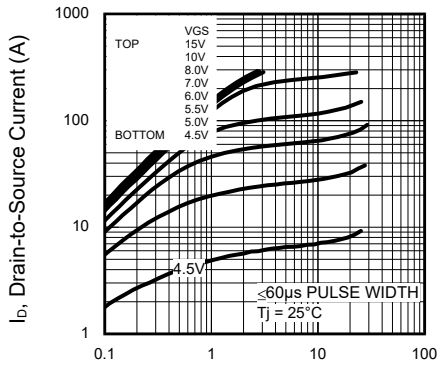


Figure 1: Typical On-Resistance vs. Gate Voltage

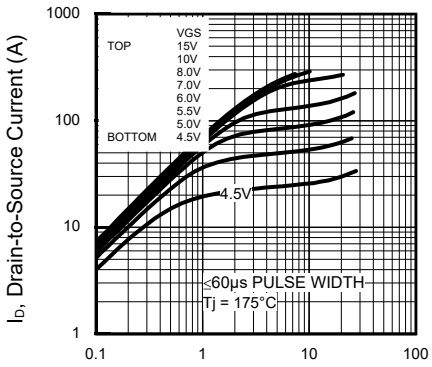


Figure 2: Typical Output Characteristics

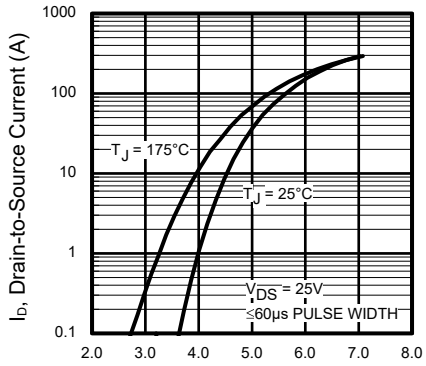


Figure 3: Typical Output Characteristics

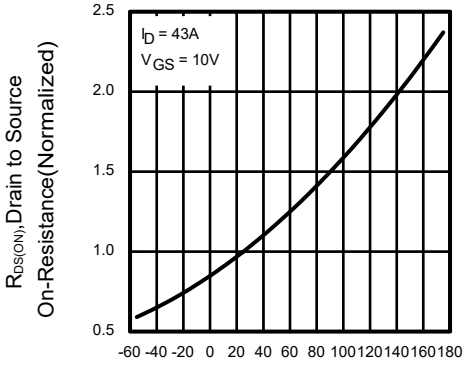


Figure 4: Normalized On-Resistance vs. Temperature

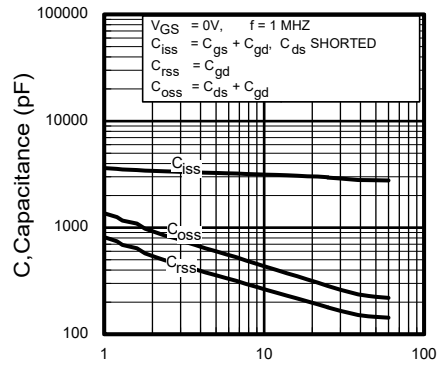


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

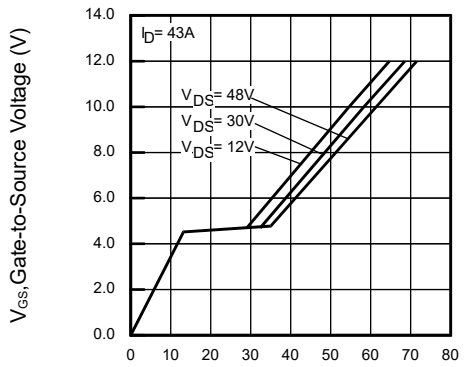


Figure 6: Typical Gate Charge vs.

6.2Typical Characterisitics

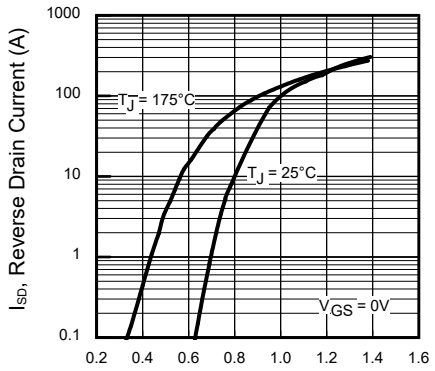


Figure 7: Typical Capacitance vs. Drain-to-Source Voltage

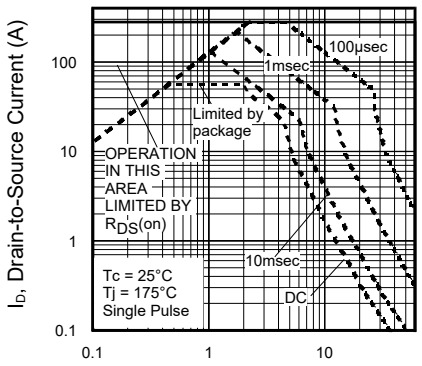


Figure 8: Maximum Safe Operating Area

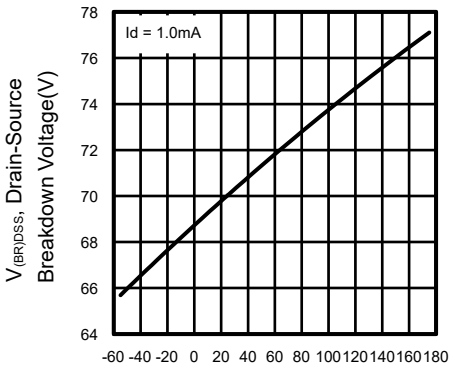


Figure 9: Drain-to-Source Breakdown Voltage

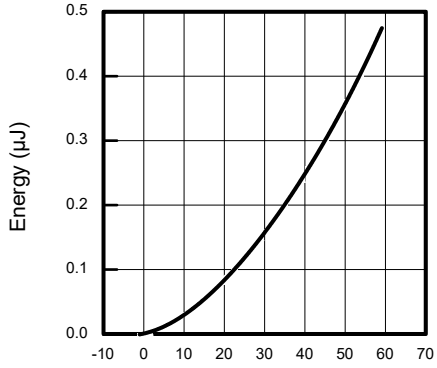


Figure 10: Typical C_{oss} Stored Energy

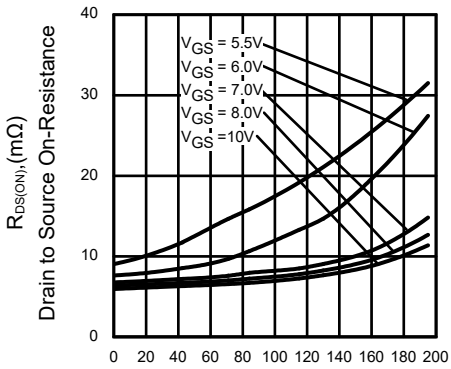


Figure 11: Typical On-Resistance vs. Drain Current

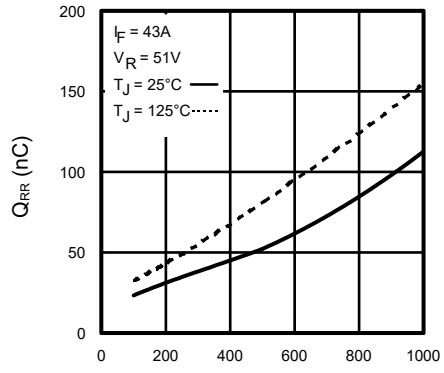


Figure 12: Typical Stored Charge vs. dif/dt

6.3Typical Characterisitics

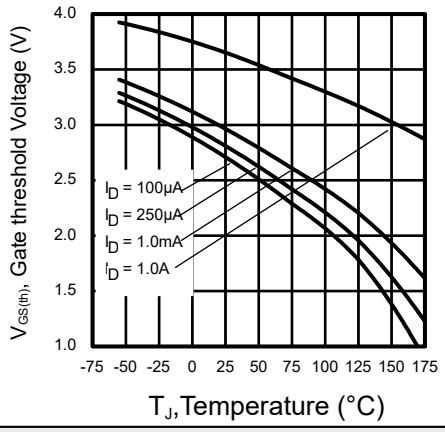


Figure 13: Threshold Voltage vs. Temperature

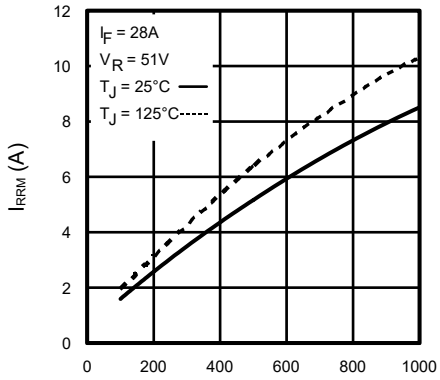


Figure 14: Typical Recovery Current vs. dif/dt

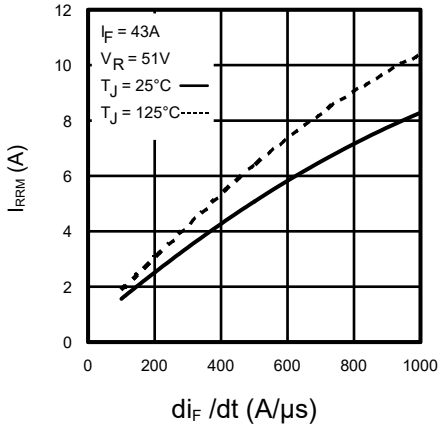


Figure 15: Typical Recovery Current vs. dif/dt

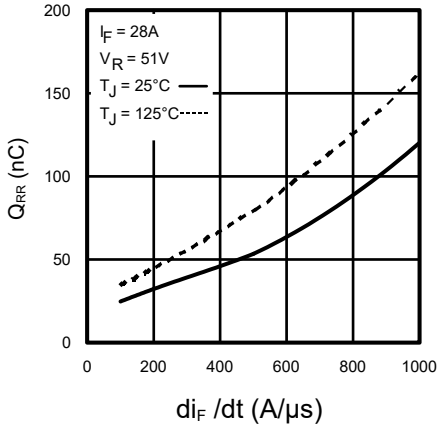


Figure 16: Typical Stored Charge vs. dif/dt

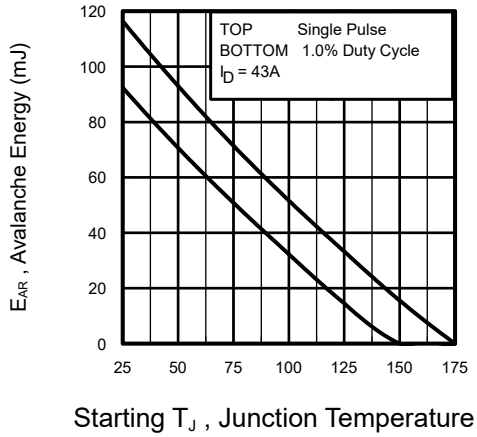


Figure 17: Maximum Avalanche Energy vs. Temperature

6.4Typical Characterisitics

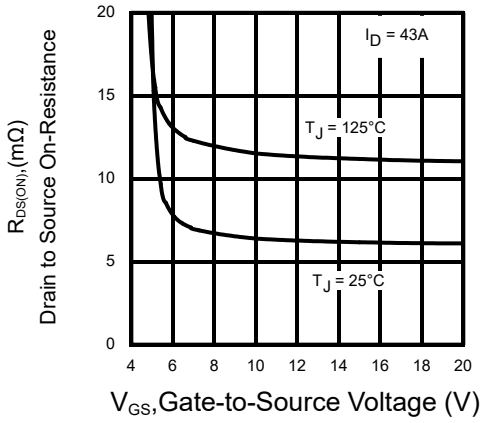


Figure 18: Typical On-Resistance vs. Gate Voltage

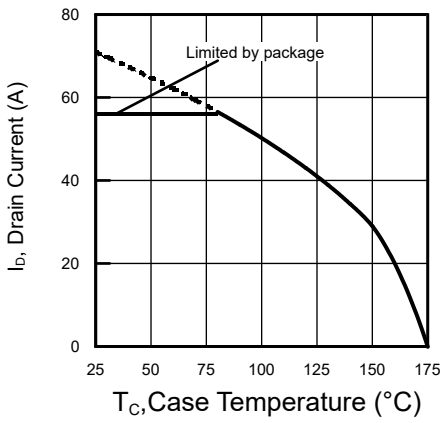


Figure 19: Maximum Drain Current vs. Case Temperature

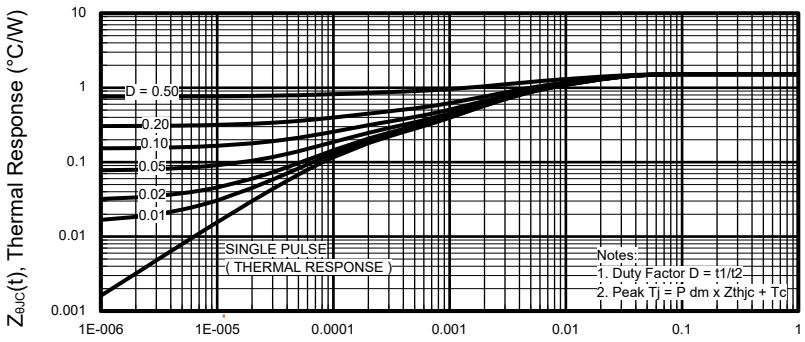


Figure 20: Maximum Effective Transient Thermal Impedance, Junction-to-Case

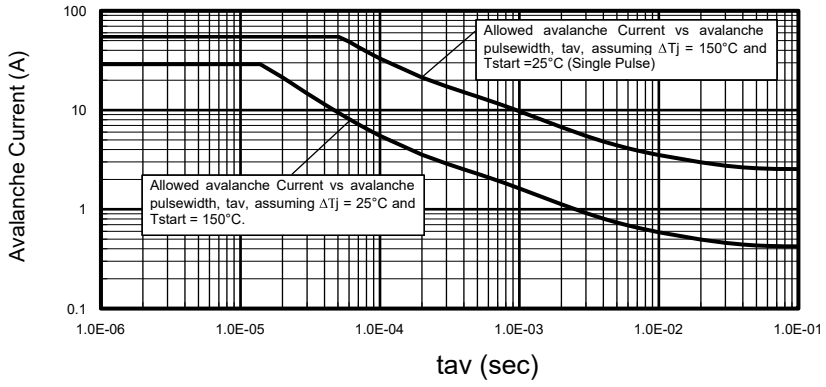


Figure 21: Typical Avalanche Current vs.Pulse width

Notes on Repetitive Avalanche Curves , Figures 21, 17:

1.Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}.

This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 20, 21).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = t_{av} ·f

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 18)

P_D (ave) = 1/2 (1.3·BV·I_{av}) = ΔT/ Z_{thJC}

I_{av} = 2ΔT/ [1.3·BV·Zth]

$E_{AS\ (AR)}$ = P_D (ave)·t_{av}

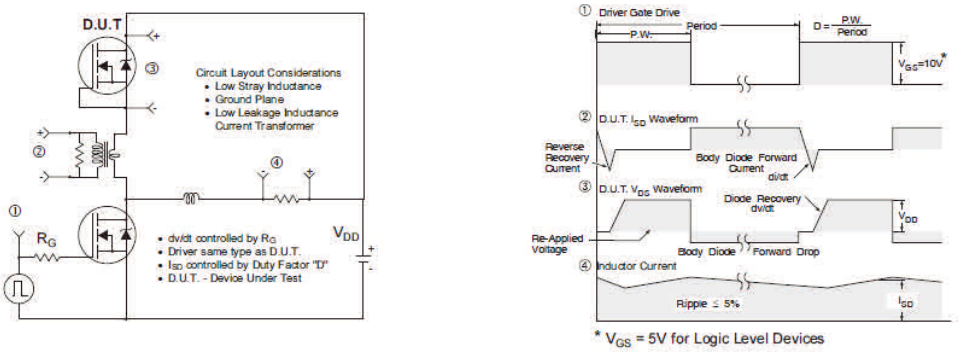


Figure 22: Peak Diode Recovery dv/dt Test Circuit for N-Channel Power MOSFETs

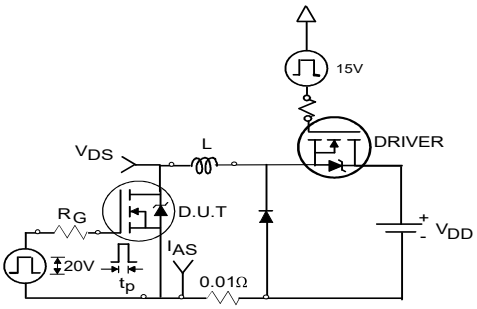


Figure 23a: Unclamped Inductive Test Circuit

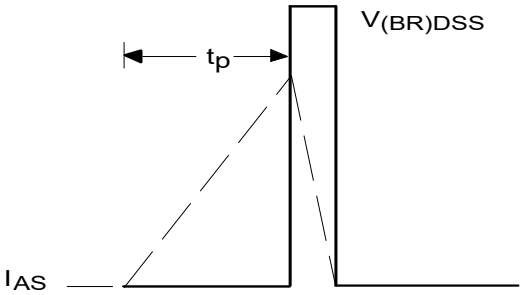


Figure 23b: Unclamped Inductive Waveforms

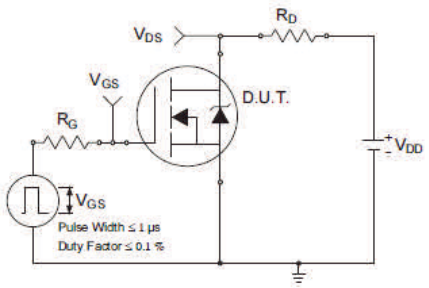


Figure 24a: Switching Time Test Circuit

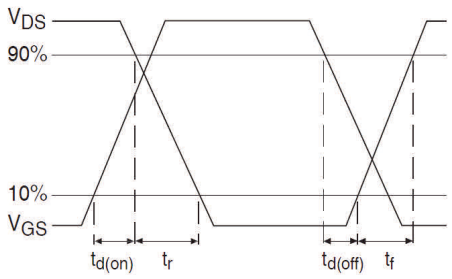


Figure 24b: Switching Time Waveforms

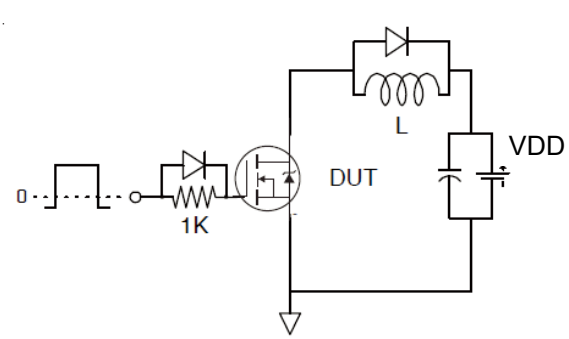


Figure 25a: Gate Charge Test Circuit

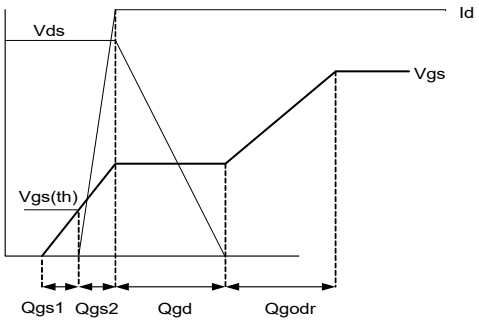
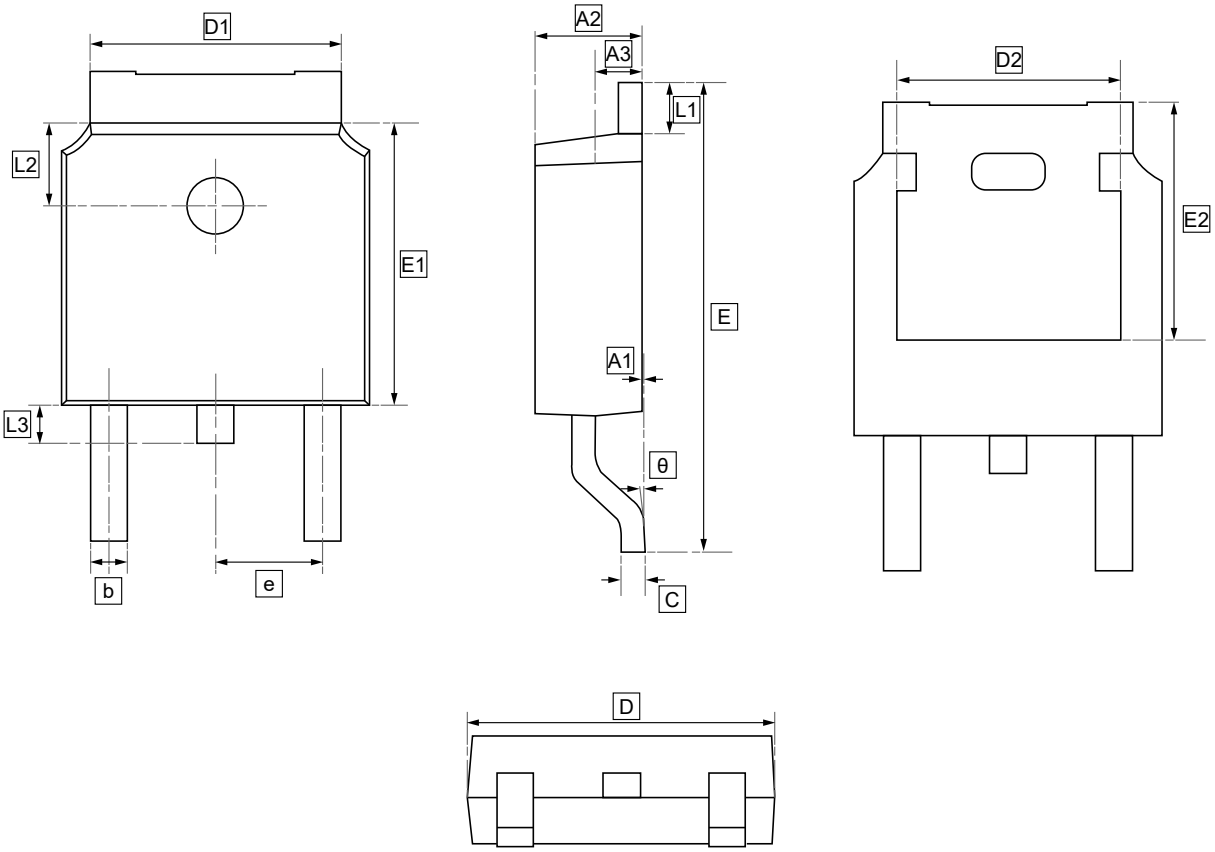


Figure 25b: Gate Charge Waveform

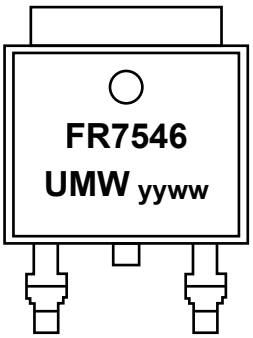
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFR7546TR	TO-252	2500	Tape and reel

9.Disclaimer

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