UMW NTD20N06LT4G

60V N-Channel MOSFET

1.Features

- $V_{DS\ (V)}$=60V
- I_D=12A
- $R_{DS(ON)}$<35mΩ(V_{GS}=5V)
- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

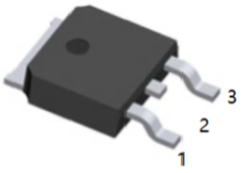
2.Applications

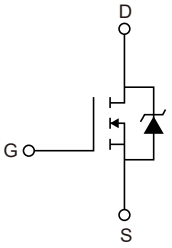
- Tighter V_{SD} Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- Lower $R_{DS(ON)}$
- Lower $V_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	SOURCE
3	S	DRAIN

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_J= 25°C

Parameter	Symbol	Rating	Units
Drain-to-Source Voltage	V_{DSS}	60	V_{dc}
Drain−to−Gate Voltage (R_{GS}=1MΩ)	V_{DGR}	60	V_{dc}
Gate−to−Source Voltage, Continuous	V_{GS}	±15	V_{dc}
− Non−Repetitive (tp≤10 ms)	V_{GS}	±20	V_{dc}
Drain Current − Continuous @ T_A=25°C	I_D	12	A_{dc}
− Continuous @ T_A=100°C	I_D	10	A_{dc}
− Single Pulse (t_p≤10 μs)	I_{DM}	45	A_{pk}

Total Power Dissipation @ T_A = 25°C	P_D	48	W
Derate above 25°C		0.32	W/°C
Total Power Dissipation @ T_A = 25°C (Note 1)		2.1	W
Total Power Dissipation @ T_A = 25°C (Note 2)		1.5	W
Operating and Storage Temperature Range	T_J,T_{STG}	−55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy-Starting Tj= 25°C (V_{DD}=25Vdc, V_{GS}=5Vdc $I_{L(pk)}$=11A,L=1mH, V_{DS}=60Vdc)	E_{AS}	61	mJ
Thermal Resistance-Junction-to-Case	$R_{\theta JC}$	3.13	°C/W
-Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W
-Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	°C/W
Maximum Lead Temperature for SolderingPurposes, 1/8 in. from case for10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in pad size (Cu area = 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu area = 0.412 in^2)

5.Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0Vdc, I_D=250μAdc	60	71.3		Vdc
(Temperature Coefficient Positive) (Note 3)				71.2		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60Vdc, V_{GS}=0Vdc			1	μAdc
		V_{DS}=60Vdc,V_{GS}=0Vdc,T_J=150°C			10	μAdc
Gate−Body Leakage Current	I_{GSS}	V_{GS}=±15Vdc, V_{DS}=0Vdc			±100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage(Note 3)	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μAdc	1	1.6	2	Vdc
(Negative Temperature Coefficient)				4.6		mV/°C
Static Drain−Source On−State Resistance	$R_{DS(ON)}$	V_{GS}=4.5Vdc, I_D=10Adc		35	45	mΩ
Static Drain−to−Source	$V_{DS(ON)}$	V_{GS}=5Vdc,I_D=20Adc		0.81	1.66	Vdc
On−Resistance (Note 3)		V_{GS}=5Vdc,I_D=10Adc,T_J=150°C		0.72		Vdc
Forward Transconductance (Note 3)	g_{FS}	V_{DS}=4Vdc, I_D=10Adc		17.5		Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS}=25Vdc, V_{GS}=0Vdc f=1MHz		707	990	pF
Output Capacitance	C_{oss}			224	320	pF
Transfer Capacitance	C_{rss}			72	105	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=30Vdc, I_D=20Adc V_{GS}=5Vdc, R_G=9.1Ω(Note 3)		9.6	20	ns
Rise Time	t_r			98	200	ns
Turn-Off Delay Time	$t_{D(off)}$			25	50	ns
Fall Time	t_f			62	120	ns
Gate Charge	Q_T	V_{DS}=48Vdc, I_D=20Adc V_{GS}=5Vdc(Note 3)		16.6	32	nC
	Q_1			5.5		nC
	Q_2			8.5		nC

DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward On−Voltage	V_{SD}	I_S=20Adc, V_{GS}=0V(Note 3)		0.97	1.2	Vdc
		I_S=20Adc, V_{GS}=0V, T_J=150°C		0.85		Vdc
Reverse Recovery Time	t_{rr}	I_S=20A, dI_S/dt=100 A/μs(Note 3) V_{GS}=0Vdc		42		ns
	t_a			30		ns
	t_b			12		ns
Reverse Recovery Stored Charge	Q_{rr}			0.66		μC

Notes:

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

6.1Typical Characterisitics

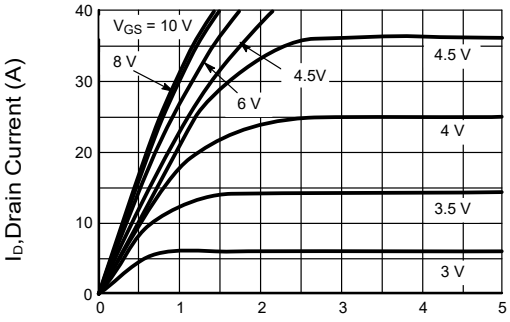


Figure 1: On−Region Characteristics

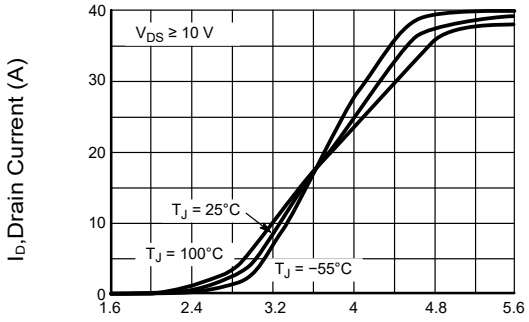


Figure 2: Transfer Characteristics

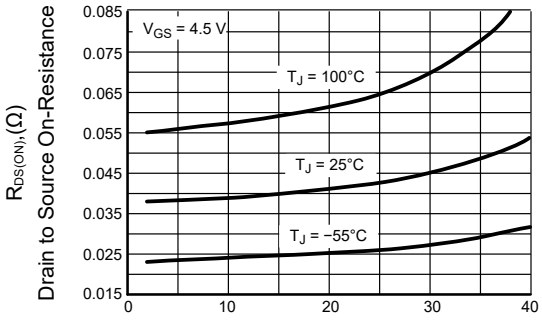


Figure 3: On−Resistance versus Drain Current and Temperature

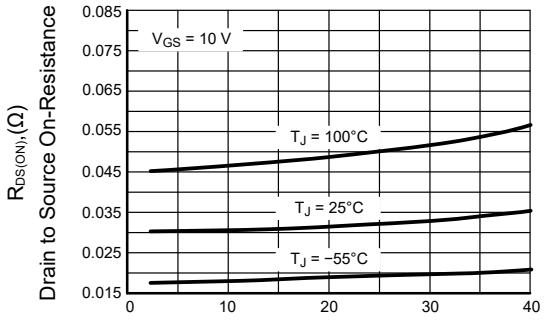


Figure 4: On−Resistance versus Drain Current and Gate Voltage

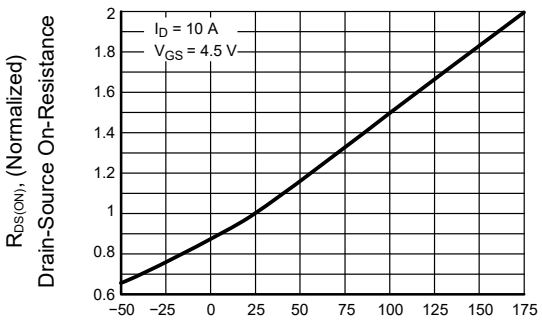


Figure 5: On−Resistance Variation with Temperature

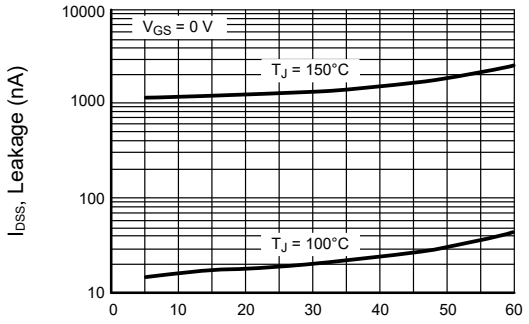


Figure 6: . Drain−To−Source Leakage Current versus Voltage

6.2Typical Characterisitics

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (t) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG} R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an R_C network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on-state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex.The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

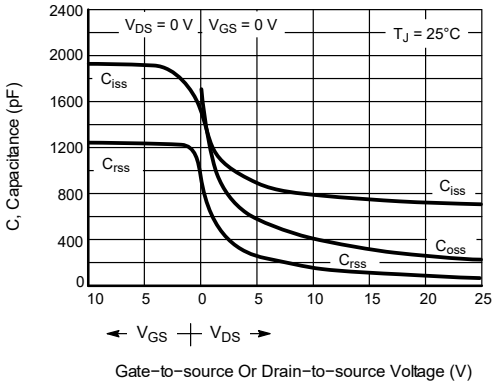
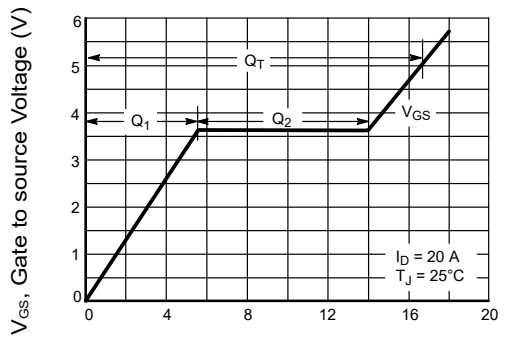


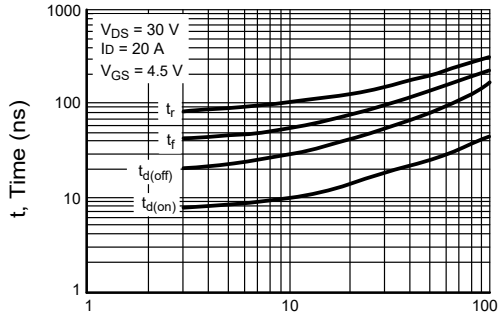
Figure 7. Capacitance Variation

6.3Typical Characterisitics



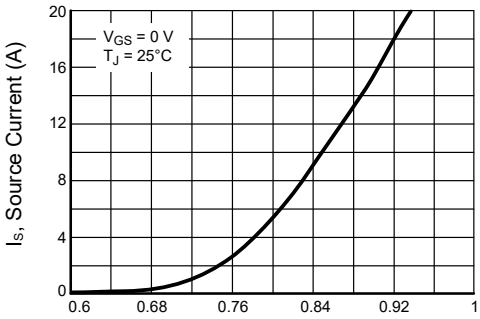
Q_G, Total Gate Charge (nC)

Figure 13: Gate−To−Source and Drain−To−Source Voltage versus Total Charge



R_G, Gate Resistance (OHMS)

Figure 14: Resistive Switching Time Variation versus Gate Resistance



V_{SD},Source to Drain Voltage (V)

Figure 15: Diode Forward Voltage versus Current

6.4Typical Characterisitics

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance - General Data and Its Use.”

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (tr,tf) do not exceed 10 s. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)}$ - T_C)/(R_{JC}).

A Power MOSFET designated E -FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous ID can safely be assumed to equal the values indicated.

6.5Typical Characterisitics

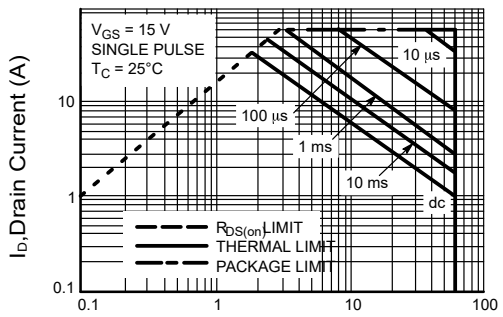


Figure 11: Maximum Rated Forward Biased Safe Operating Area

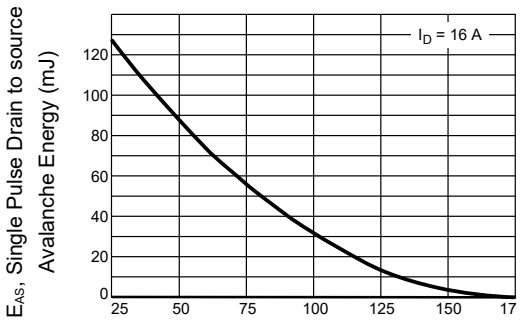


Figure 12: Maximum Avalanche Energy versus Starting Junction Temperature

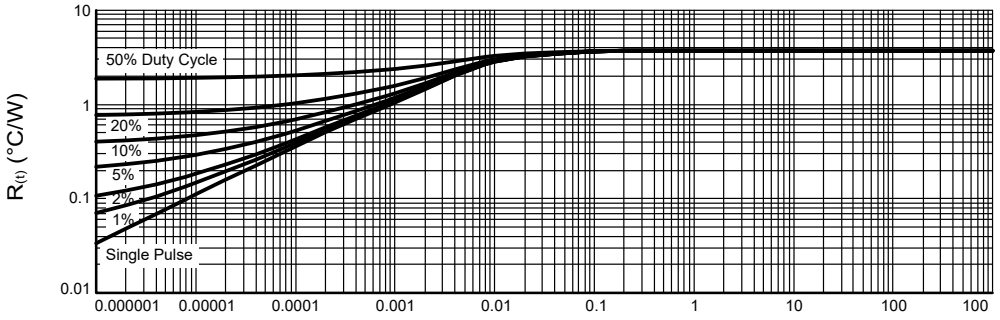


Figure 13: Thermal Respons

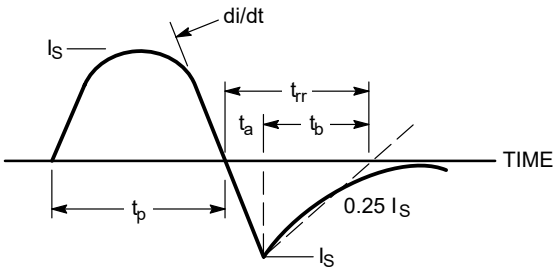
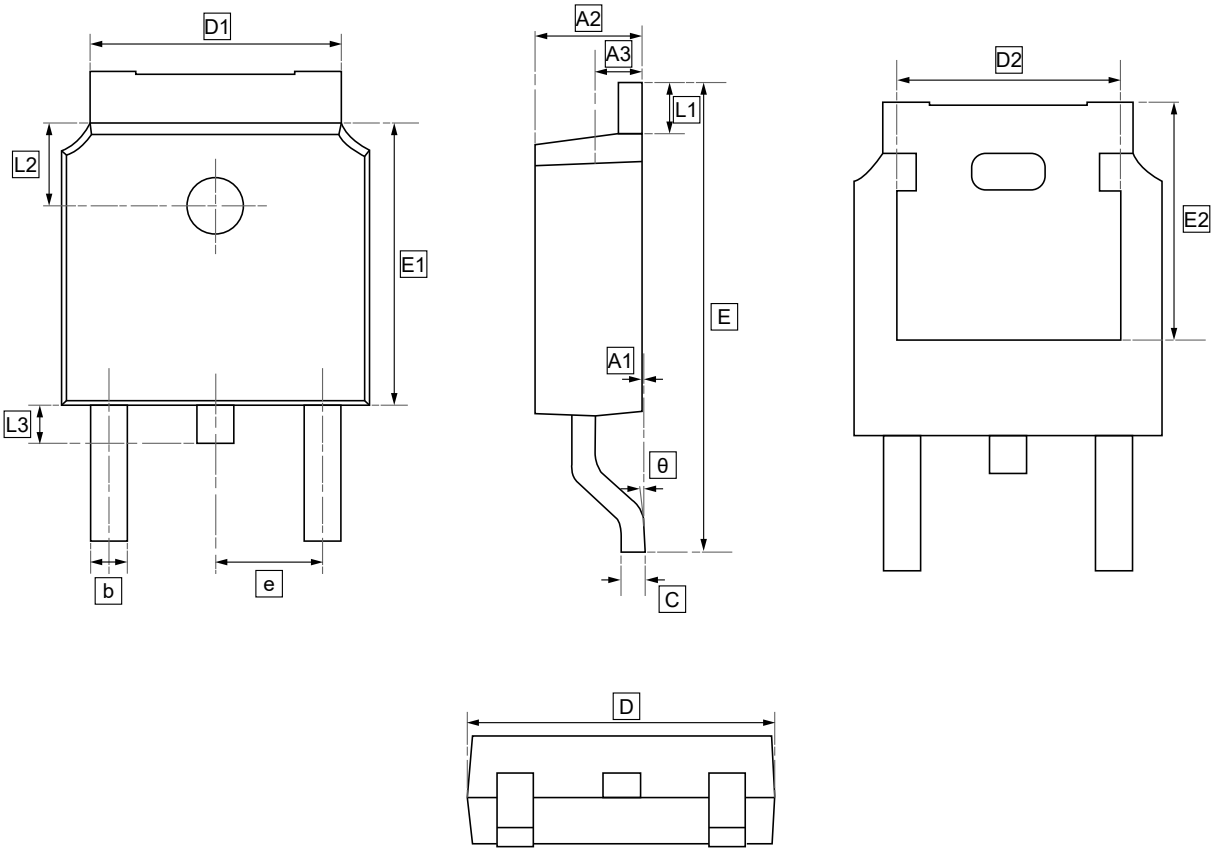


Figure 14: Diode Reverse Recovery Waveform

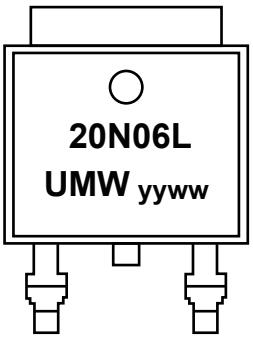
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NTD20N06LT4G	TO-252	2500	Tape and reel

9.Disclaimer

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