

1. Description

These dual N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching.

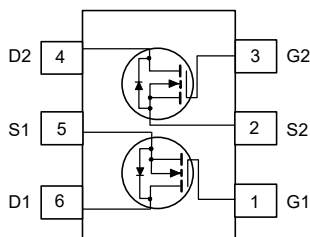
2. Features

- $V_{DS(V)}=50V$
- $I_D=0.51A$
- $R_{DS(ON)}=1\Omega(V_{GS}=10V)$
- High density cell design for low $R_{DS(ON)}$
- High saturation current
- Proprietary SOT23-6 package design using copper lead frame for superior thermal and electrical capabilities.

3. Pinning information

Pin	Symbol	Description
1,3	G1,G2	GATE
2,5	S1,S2	SOURCE
4,6	D1,D2	DRAIN

SOT23-6



4. Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	50	V
Gate-Source Voltage	V_{GSS}	20	V
Drain Current - Continuous (Note 1a)	I_D	0.51	A
-Pulsed		1.5	A
Power Dissipation for Single Operation (Note 1a)	P_D	0.96	W
(Note 1b)		0.9	W
(Note 1c)		0.7	W
Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$



5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	130	°C/W
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	60	°C/W



6. Electrical Characteristic ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	50			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$ $T_J=125^\circ\text{C}$			1	μA
					500	μA
Gate - Body Leakage, Forward	I_{GSSF}	$V_{GS}=20V, V_{DS}=0V$			100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	$V_{GS}=-20V, V_{DS}=0V$			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$ $T_J=125^\circ\text{C}$	1	1.9	2.5	V
			0.8	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=0.51A$ $T_J=125^\circ\text{C}$		1	2	Ω
		$V_{GS}=4.5V, I_D=0.35A$		1.7	3.5	Ω
On-State Drain Current	$I_{D(on)}$	$V_{GS}=10V, V_{DS}=10V$	1.5			A
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=0.51A$		400		mS
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1\text{MHz}$		20		pF
Output Capacitance	C_{oss}			13		pF
Reverse Transfer Capacitance	C_{rss}			5		pF
Turn - On Delay Time	$t_{D(on)}$	$V_{DD}=25V, I_D=0.25A$ $V_{GS}=10V, R_{GEN}=25\Omega$		6	20	ns
Turn - On Rise Time	t_r			6	20	ns
Turn - Off Delay Time	$t_{D(off)}$			11	20	ns
Turn - Off Fall Time	t_f			5	20	ns
Total Gate Charge	Q_g	$V_{DS}=25V, I_D=0.51A, V_{GS}=10V$		1		nC
Gate-Source Charge	Q_{gs}			0.19		nC
Gate-Drain Charge	Q_{gd}			0.33		nC
Maximum Continuous Source Current	I_S				0.51	A
Maximum Pulse Source Current (Note 2)	I_{SM}				1.5	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=0.51A$ (Note 2)		0.8	1.2	V



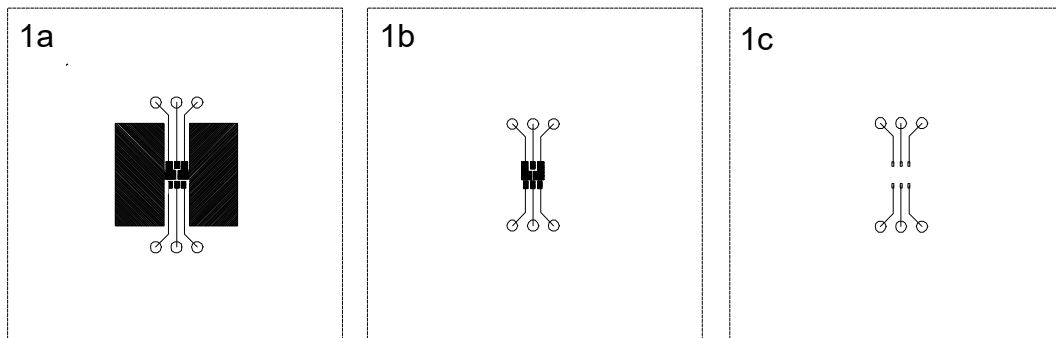
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA(t)}} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA(t)}} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 130°C/W when mounted on a 0.125 in² pad of 2oz copper.
- 140°C/W when mounted on a 0.005 in² pad of 2oz copper.
- 180°C/W when mounted on a 0.0015 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.



7.1 Typical characteristic

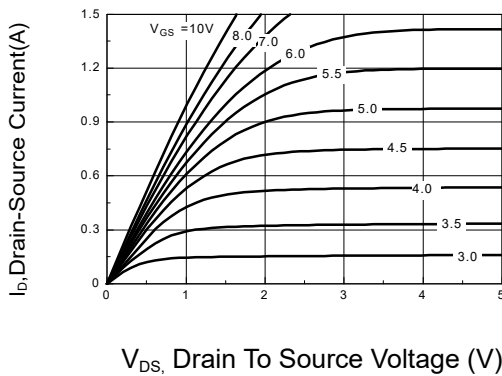


Figure 1: On-Region Characteristics

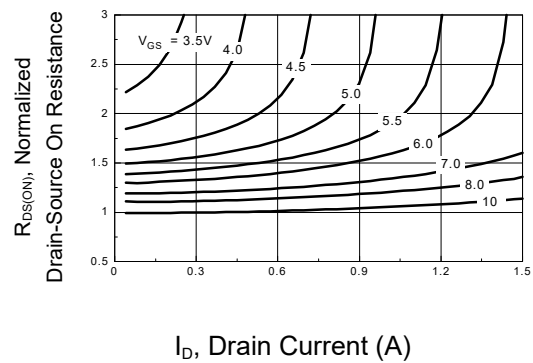


Figure 2: On-Resistance Variation with Gate Voltage and Drain Current

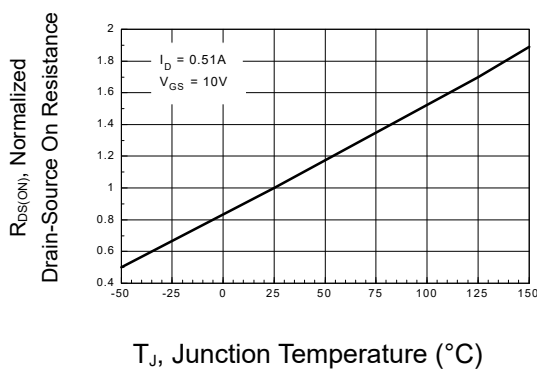


Figure 3: On-Resistance Variation with Temperature

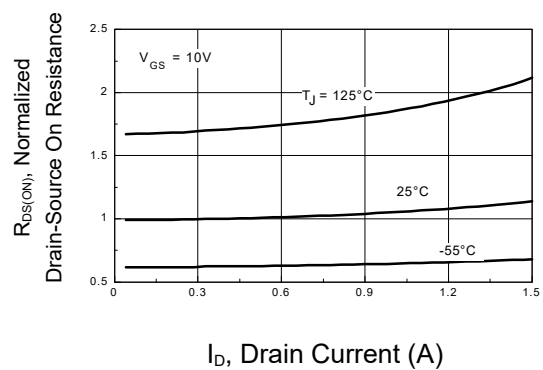


Figure 4: On-Resistance Variation with Drain Current and Temperature.

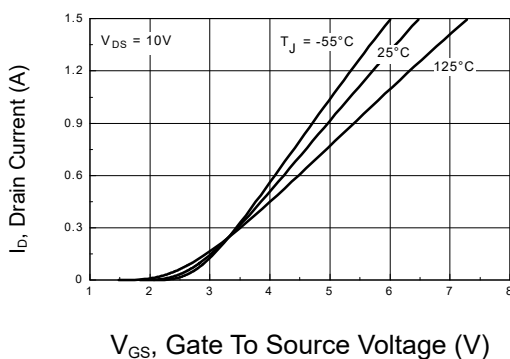


Figure 5: Transfer Characteristics

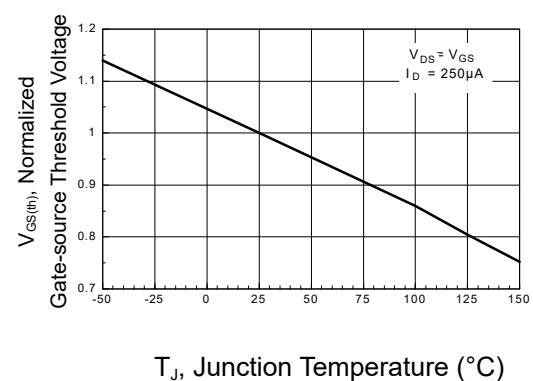
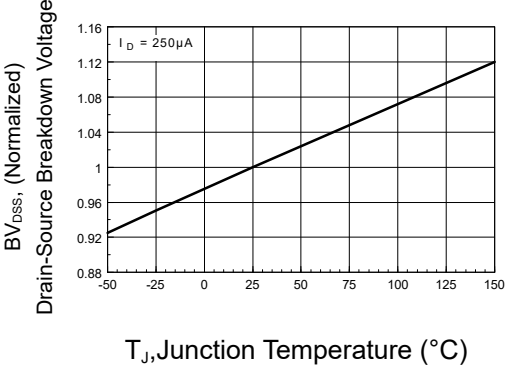
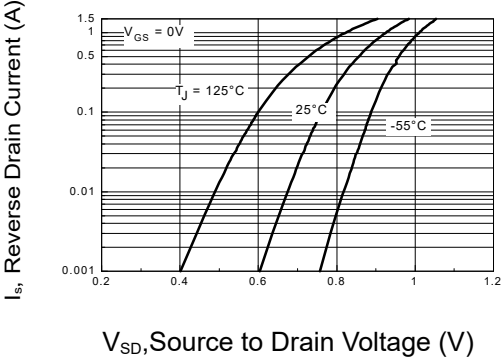
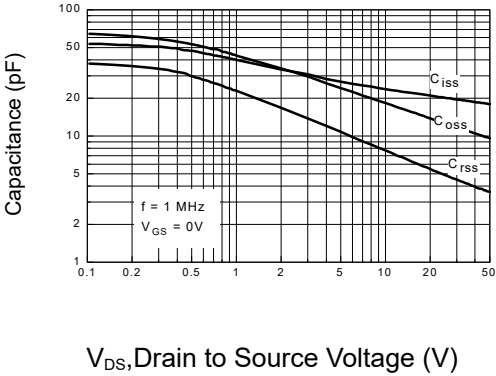
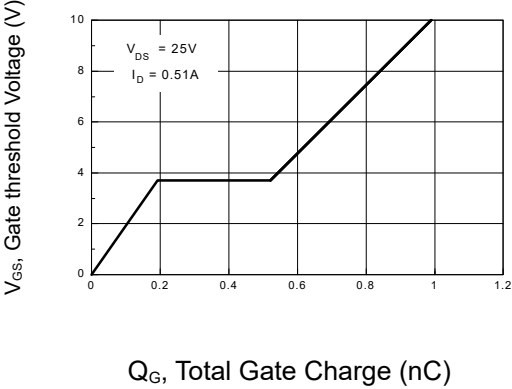
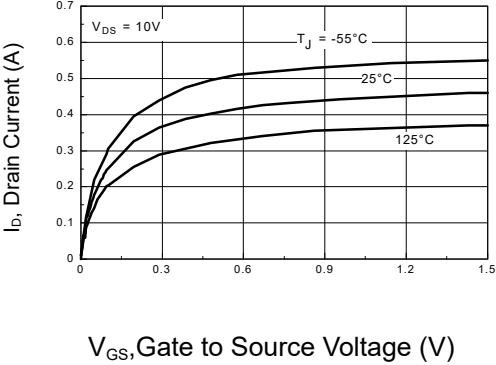
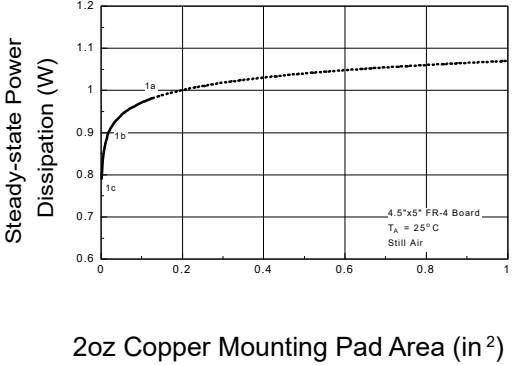


Figure 6: Gate Threshold Variation with Temperature.

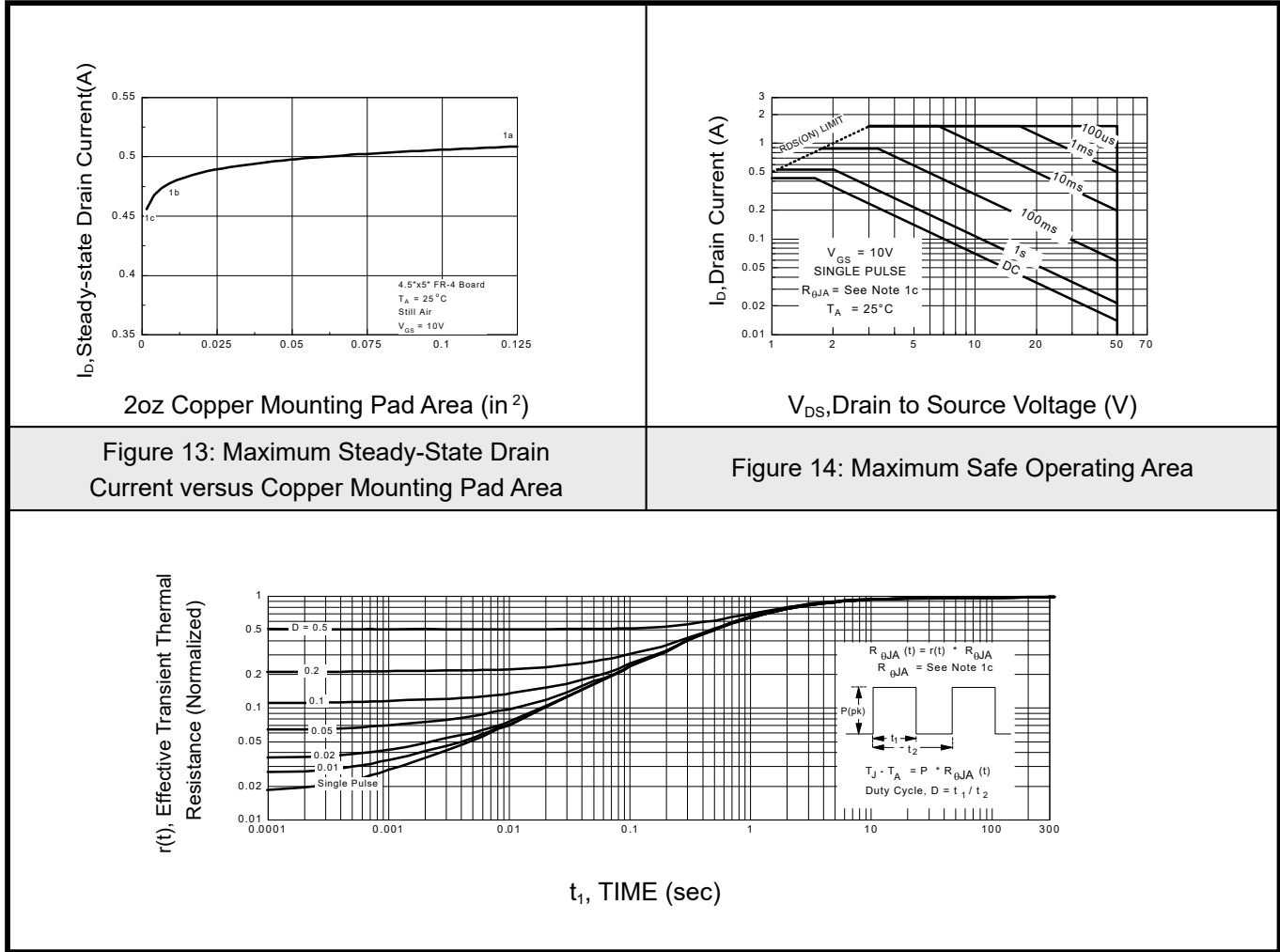


7.2Typical characteristic

 Figure 7: Breakdown Voltage Variation with Temperature	 Figure 8: Body Diode Forward Voltage Variation with Current and Temperature
 Figure 9: Capacitance Characteristics	 Figure 10: Gate Charge Characteristics
 Figure 11: Transconductance Variation with Drain Current and Temperature	 Figure 12: SOT23-6 Dual Package Maximum

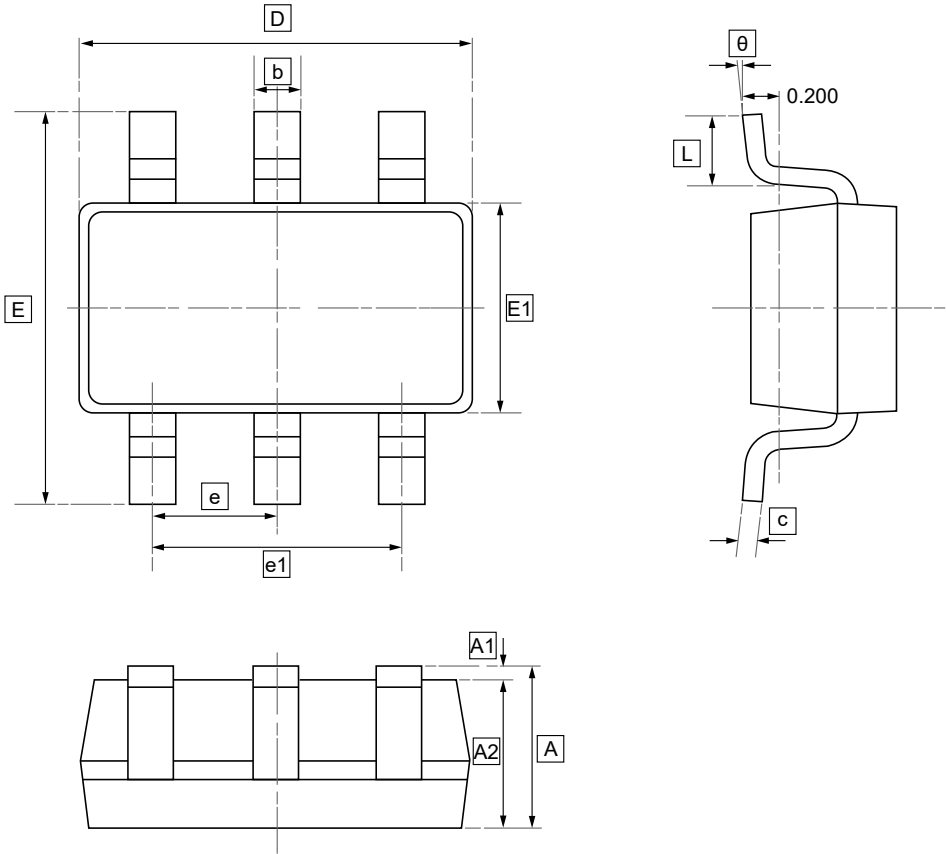


7.3Typical characteristic





8.SOT23-6 Package Outline Dimensions

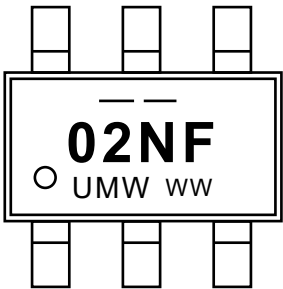


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°



9.Ordering information



ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NDC7002N	SOT23-6	3000	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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