

1.Features

- $V_{DS(V)}=40V$
- $R_{DS(ON)}<17m\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<21m\Omega(V_{GS}=4.5V)$

3.Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

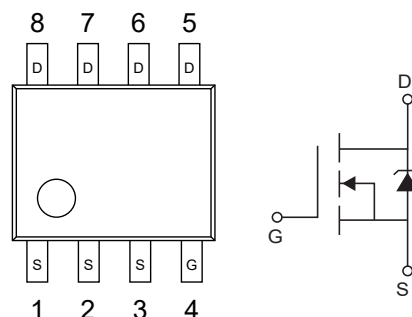
2.Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter		Symbol	Rating	Units
Drain- Source Voltage		V_{DS}	40	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current, $V_{GS}=10V$	$T_A=25^{\circ}C$	I_D	9	A
Continuous Drain Current, $V_{GS}=10V$	$T_A=70^{\circ}C$		7.3	A
Pulsed Drain Current ①		I_{DM}	73	A
Maximum Power Dissipation ③	$T_A=25^{\circ}C$	P_D	2.5	W
Maximum Power Dissipation ③	$T_A=70^{\circ}C$		1.6	W
Linear Derating Factor			0.02	mW/ $^{\circ}C$
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}C$



6. Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Drain Lead	$R_{\theta JL}$		20	°C/W
Junction-to-Ambient ④	$R_{\theta JA}$		50	°C/W

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J=25^{\circ}\text{C}$, $L=8.1\text{mH}$, $R_G=25\Omega$, $I_{AS}=7.2\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.



7. Electrical Characteristics $T_J=25^{\circ}\text{C}$

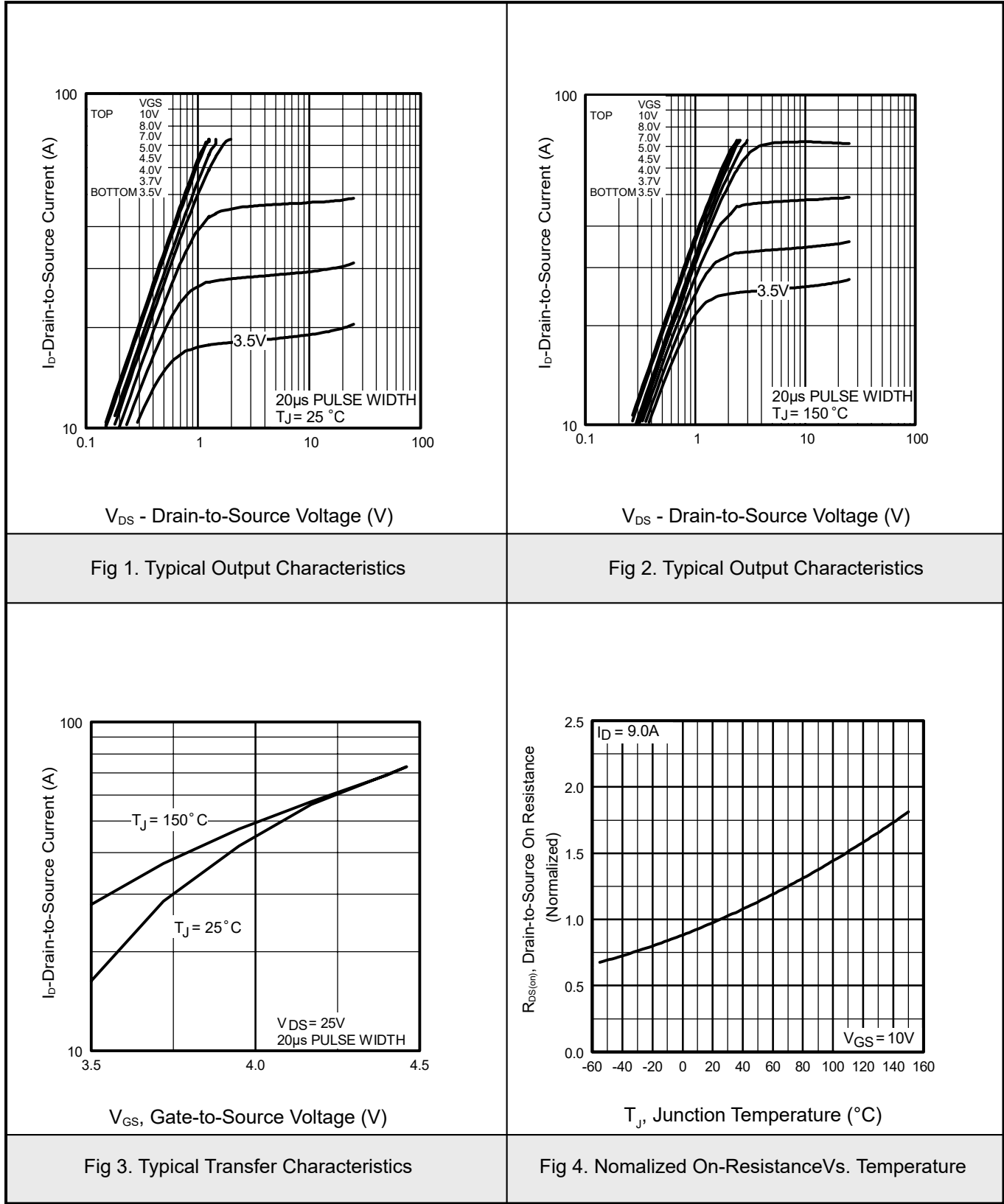
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	I _D =250μA, V _{GS} =0V	40			V
Breakdown Voltage Temp. Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D =1mA,Reference to 25°C		0.04		V/°C
Static Drain-to-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =9A ③		12	17	mΩ
		V _{GS} =4.5V, I _D =7.2A ③		15.5	21	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1		3	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =32V, V _{GS} =0V			20	μA
		V _{DS} =32V, V _{GS} =0V, T _J =125°C			100	μA
Gate-to-Source Forward Leakage	I _{GSS}	V _{GS} =16V			200	nA
Gate-to-Source Reverse Leakage		V _{GS} =-16V			-200	nA
Dynamic						
Forward Transconductance	g _{FS}	V _{DS} =20V, I _D =7.2A	17			S
Total Gate Charge	Q _g	I _D =7.2A V _{DS} =20V V _{GS} =4.5V ③		15	23	nC
Gate-to-Source Charge	Q _{gs}			7	11	nC
Gate-to-Drain ("Miller") Charge	Q _{gd}			5	8	nC
Output Gate Charge	Q _{oss}	V _{GS} =0V, V _{DS} =16V		16	24	nC
Turn-On Delay Time	t _{D(on)}	V _{DD} =20V I _D =7.2A R _G =1.8Ω V _{GS} =4.5V ③		11		ns
Rise Time	t _r			2.2		ns
Turn-Off Delay Time	t _{D(off)}			14		ns
Fall Time	t _f			3.5		ns
Input Capacitance	C _{iss}	V _{GS} =0V		2000		pF
Output Capacitance	C _{oss}	V _{DS} =20V		480		pF
Reverse Transfer Capacitance	C _{rss}	f=1.0MHz		28		pF
Avalanche Characteristics						
Single Pulse Avalanche Energy ②	E _{AS}				210	mJ
Avalanche Current ①	I _{AR}				7.2	A



Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			2.3	A
Pulsed Source Current (Body Diode) ①	I_{SM}				73	
Diode Forward Voltage	V_{SD}	$T_J=25^{\circ}\text{C}, I_S=7.2\text{A}, V_{GS}=0\text{V}$ ③		0.8	1.3	V
		$T_J=125^{\circ}\text{C}, I_S=7.2\text{A}, V_{GS}=0\text{V}$ ③		0.65		V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, I_F=7.2\text{A}, V_R=15\text{V}$ $dI/dt=100\text{A}/\mu\text{s}$ ③		47	71	ns
Reverse Recovery Charge	Q_{rr}			91	140	nC
Reverse Recovery Time	t_{rr}	$T_J=125^{\circ}\text{C}, I_F=7.2\text{A}, V_R=20\text{V}$ $dI/dt=100\text{A}/\mu\text{s}$ ③		77	120	ns
Reverse Recovery Charge	Q_{rr}			150	230	nC

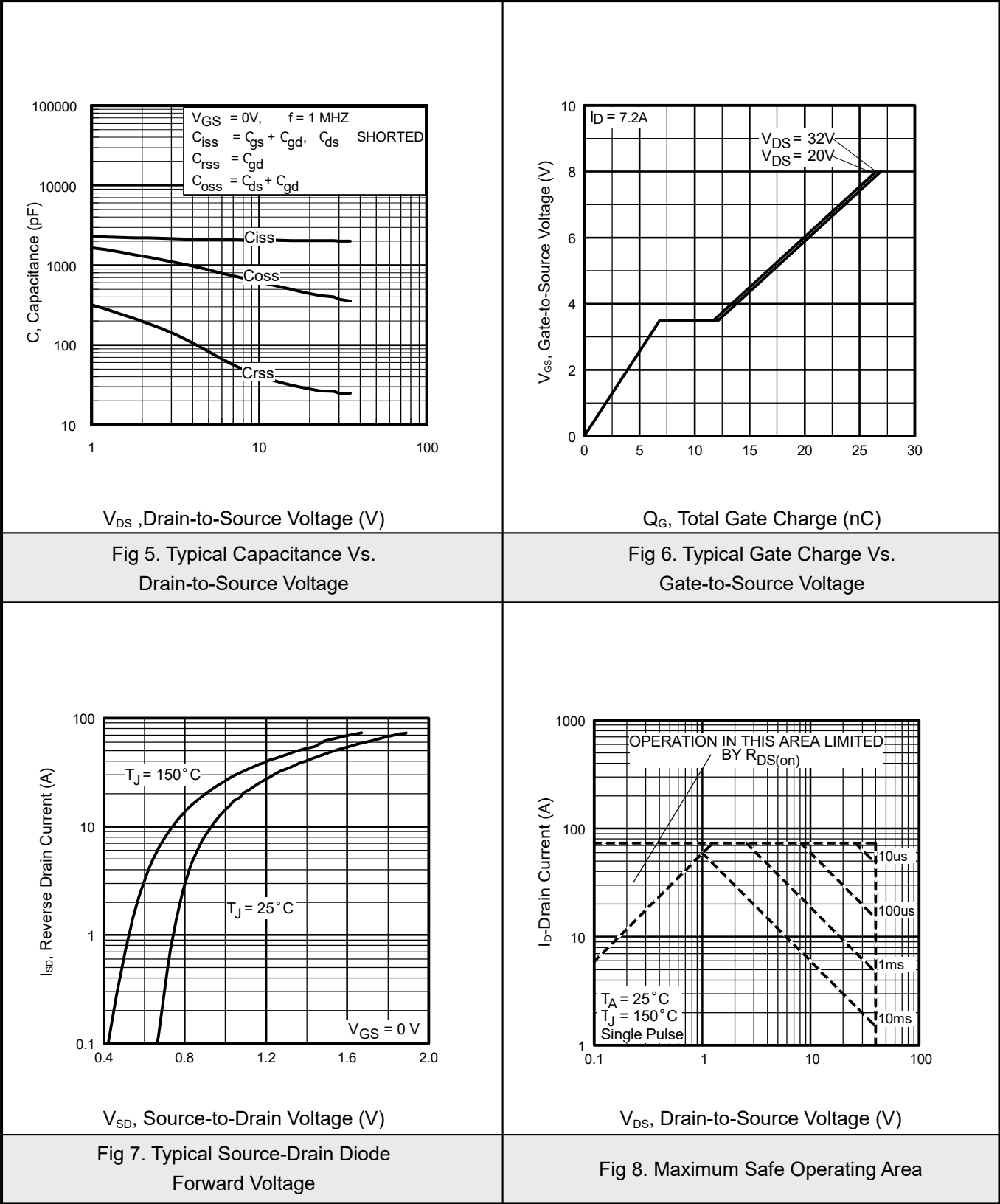


8.1Typical Characteristics



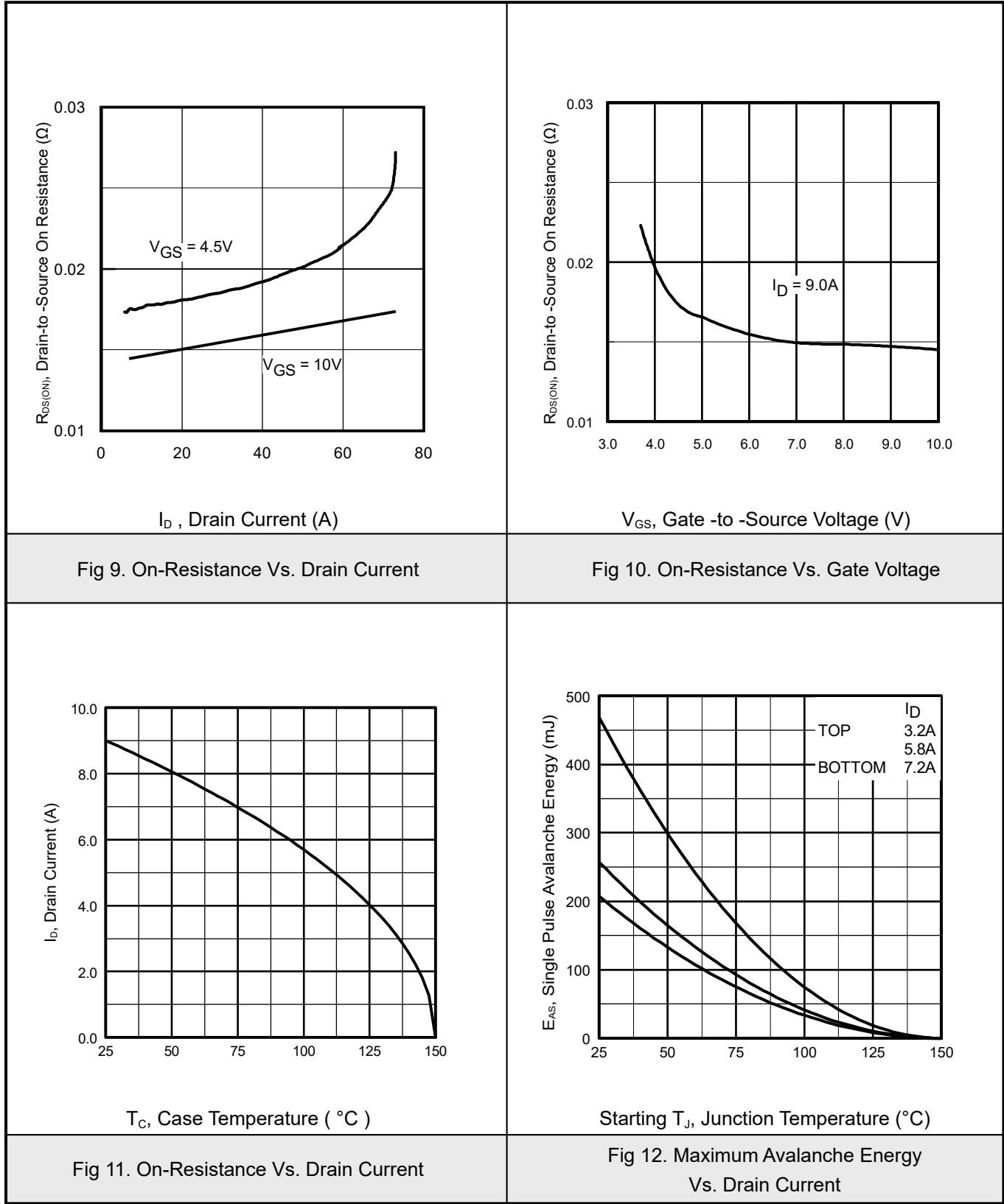


8.2Typical Characteristics





8.3Typical Characterisitics





8.4 Typical Characteristics

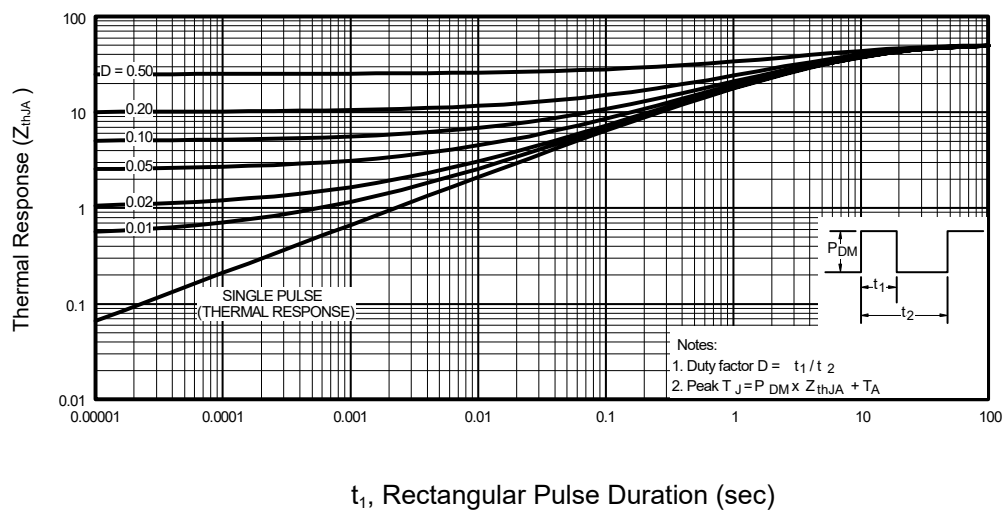


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

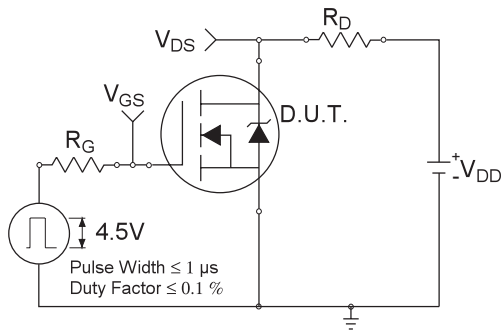


Fig 14a. Switching Time Test Circuit

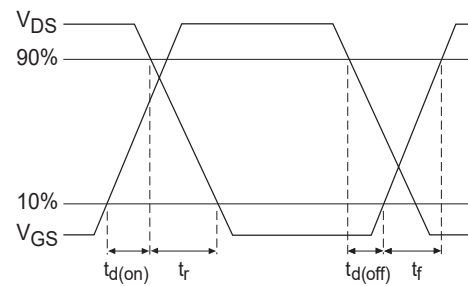


Fig 14b. Switching Time Waveforms

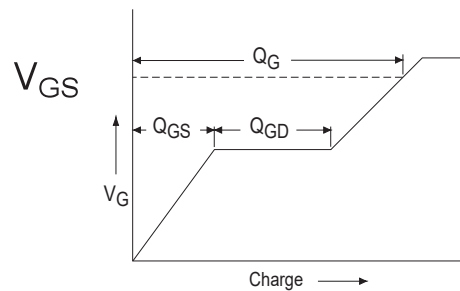
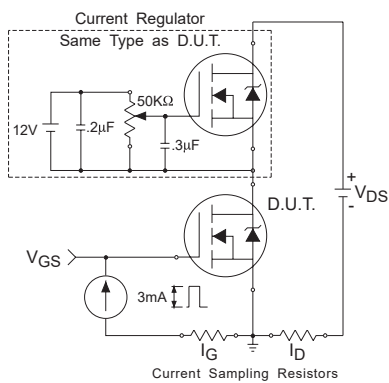


Fig 15a&b. Basic Gate Charge Test Circuit and Waveform

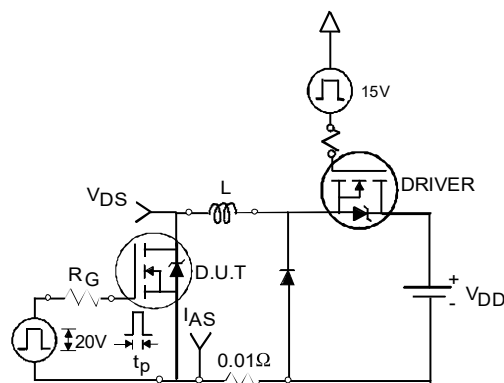
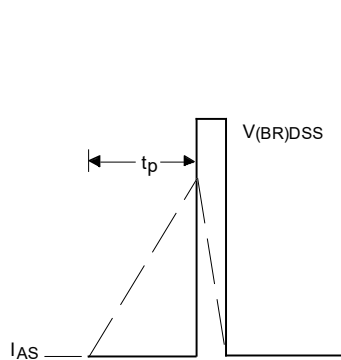
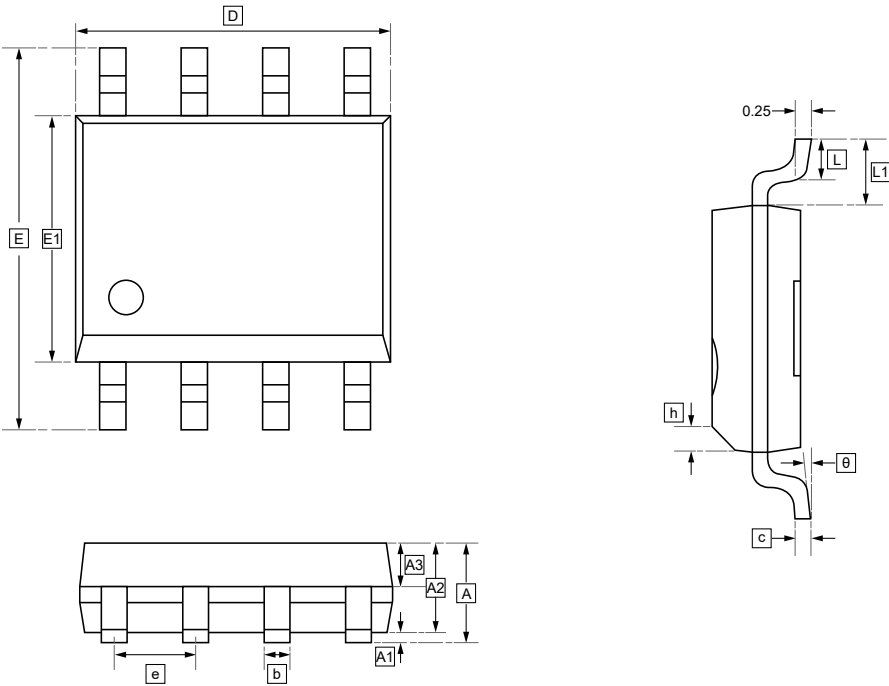


Fig 16a&b. Unclamped Inductive Test circuit and Waveforms



9.SOP-8 Package Outline Dimensions



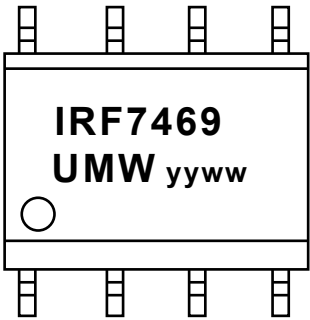
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7469TR	SOP-8	3000	Tape and reel



11.Disclaimer

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