



钜地半导体
Tudi Semiconductor

Product Specification

TUDI-SP490/SP491

Enhanced Full-Duplex RS-485 Transceivers

网址 www.sztdbdt.com

用芯智造 · 卓越品质

**semiconductor device
manufacturer**

- Design
- research and development
- production
- and sales



Features

- 5V only
- Low power BiCMOS
- Driver/receiver enable (SP491E)
- RS-485 and RS-422 drivers/receivers
- Improved ESD specifications:
±15kV Human Body Model
±15kV IEC61000-4-2 Air Discharge

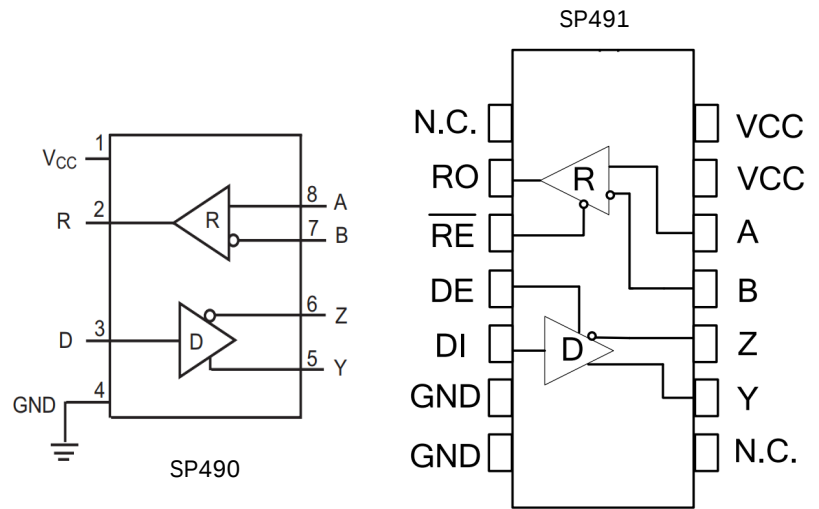


Figure 1 Pin diagram

Description

The SP490 is a low power differential line driver/receiver meeting RS-485 and RS-422 standards up to 10Mbps. The SP491 is identical to the SP490 with the addition of driver and receiver tri-state enable lines. Both products feature $\pm 200\text{mV}$ receiver input sensitivity, over wide common mode range. The SP490 is available in 8-pin NSOIC packages for operation over the commercial and industrial temperature ranges. The SP491E is available in 14-pin NSOIC packages for operation over the commercial and industrial temperature ranges.

SP490 Pin description

Pin number	Pin name	Pin function
1	VCC	Power supply: $4.5\text{V} \leq \text{VCC} \leq 5.5\text{V}$
2	R	Receiver output.
3	D	Driver Input
4	GND	Landing
5	Y	Driver in-phase output terminal
6	Z	Driver inverting output
7	B	Receiver inverting input
8	A	Receiver in-phase input



SP491 Pin description

Pin number	Pin name	Pin function
1	NC	No internal connections required
2	RO	Receiver output.When RE is low,the RO output is high if A-B is $\geq -10\text{mV}$,and low if A-B is $\leq -200\text{mV}$.
3	/RE	Receiver output enable control.When /RE is low,the receiver output is enabled and RO is active;when /RE is high,the receiver output is disabled and RO is in high-impedance state.When RE is at a high level and DE is at a low level,the device enters low-power shutdown mode
4	DE	The driver output enables the control.When DE is at high level, the driver outputs effectively;when DE is low,it outputs high-impedance state.When /RE is high and DE is low,the device enters low-power shutdown mode.
5	DI	DI driver input.When DE is high,the low level on DI makes the in-phase output A of the driver low and the in-phase output B high;the high level on DI makes the in-phase output high and the in-phase output B low.
6	GND	Landing
7	GND	Landing
8	NC	No internal connections required
9	Y	Driver in-phase output terminal
10	Z	Driver inverting output
11	B	Receiver inverting input
12	A	Receiver in phase input
13	VCC	This pin can be connected to power or left unconnected
14	VCC	Power connection



Extreme parameter

Parameter	Symbol	Unit	size
Continuous power consumption	SOP	mW	600
	DIP	mW	700
Power supply voltage	VCC	V	+7
working temperature range			-40~125
Storage temperature range			-60~150
Welding temperature range			300
Control port voltage	DI	V	-0.3~VCC+0.3
Bus side input voltage	A、B	V	-8~13
Receiver output voltage	RO	V	-0.3~VCC+0.3

The maximum limit parameters are values beyond which the device can be damaged in an irreversible manner. Operation of the device under these conditions is not intended to be normal and may affect the reliability of the device if operated continuously at the maximum rated limit. All voltages are referenced to ground.

ESD Protect

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
A、B、Y、Z		Human bodymodel		±15		KV
Other ports		Human bodymodel		±6		KV



Receiver Switching Characteristics

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Acceptor	tRPLH	See Figure 7 and Figure 8	20	60	90	ns
Input to output propagation delay from low to high						
The propagation delay from receiver input to output is from high to low	tRPHL	$V \geq 2.0V$; rising and falling edge time $V_{ID} \leq 15ns$	20	60	90	ns
$ tRPLH - tRPHL $	tsKEW2			7	10	ns
Enable low time out	tRPZL	CL=15pF See Figures 7 and 8		20	50	ns
Enable to output high time	tRPZH	CL=15pF See Figures 7 and 8		20	50	ns
Time from output low to disable	tpRLZ	CL=15pF See Figures 7 and 8		20	45	ns
Time from output high to disable	tpRHZ	CL=15pF See Figures 7 and 8		20	45	ns
Off state Enable to output high time	tRPSH	CL=15pF See Figures 7 and 8		200	1400	ns
Off state Enable low time out	tRPSL	CL=15pF See Figures 7 and 8		200	1400	ns
Time to turn off	tsHDN	NOTE2	80		300	ns

(If not otherwise, $V_{CC} = 3V \sim 5.5V$, Temp = $T_{MIN} \sim T_{MAX}$, typical value at Temp = 25) NOTE 1: ΔV_{OD} and ΔV_{OC} is the change in V_{OD} and V_{OC} amplitude caused when the DI state of the input signal changes, respectively.



DC electrical characteristics of the driver

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Driver differential output (non-loaded)	VoD ₁			4.5	VCC	V
Drive differential output	VoD ₂	graph 2, RL=27Ω	1.5	2.3	VCC	V
		graph 2, RL=50Ω	2	2.8	VCC	
Variation in the amplitude of the output voltage (NOTE1)	VoD	graph 2, RL=27Ω			0.2	V
Output common mode voltage	Voc	graph 2, RL=27Ω			3	V
Amplitude Variation of Common Mode Output Voltage(NOTE1)	Voc	graph 2, RL=27Ω			0.2	V
High-level input	V _H	DI	2.0			V
Low level input	V _π	DI			0.8	V
Logic input current	IN1	DI	-2		2	uA
Output the current during a short circuit, with high short-circuit	I _{osD1}	Short circuit to OV~12V	35		250	mA
Output the current during a short circuit, down to low	I _{osD2}	Short circuit to -7V~0V	-250		-35	mA

(If not otherwise, VCC=3V~5.5V, Temp = TMIN ~ TMAX, typical value at Temp = 25) NOTE 1: Vo D and? VOC is the change in VOD and VOC amplitude caused when the DI state of the input signal changes, respectively.



drive switch characteristics

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input to output propagation delay (low to high)	tDPLH	RDIFF=54 Ω , CL ₁ =CL ₂ =100pF(see Figure 3 and Figure 4)		12	35	ns
Input to output propagation delay (high to low)	tDPHL			12	35	ns
tDPLH-tDPHL	tsKEW1			6	10	ns
Rise time /fall time	tDR,tDF			9	25	ns
Enable to high output	tpZH	R=110 Ω (see Figure 5 and 6)		20	90	ns
Enable to output low	tpZL			20	90	ns
Input low to disable	tpLZ	R=110 Ω (see Figure 5 and 6)		20	80	ns
Enable high input	tpHZ			20	80	ns
Enable high output under off condition	tDSH	R=110 Ω (see Figure 5 and 6)		500	900	ns
Enable low output under shutdown conditions	tDSL	RL=110 Ω (see Figure 5 and 6)		500	900	ns

Supply Current

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Supply current	Icc1	/RE=0V, DE=0V		220	400	μ A
	Icc2	/RE=VCC, DE=VCC		240	400	μ A
Turn-off current	IsHDN	/RE=VCC, DE=0V		0.5	10	μ A



DC Electrical Characteristics of the Receiver

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input current(A,B)	IN2	VCC=0 or 3.3V VIN=12V			125	uA
		VCC=0 or 3.3V VIN=-7V	-100			uA
Forward input threshold voltage	VIT+	$-7V \leq V_{cm} \leq 12V$			-10/-50	mV
Reverse input threshold voltage	VIT-	$-7V \leq V_{cm} \leq 12V$	-200			mV
Input hysteresis voltage	Vhys	$-7V \leq V_{cm} \leq 12V$	10	30		mV
High level output voltage	VoH	IoUT=-4mA, VID=+200 mV	VCC-1.5			V
Low level output voltage	VoL	IoUT=+4mA, VID=-200 mV			0.4	V
Three state input leakage cur-rent	IozR	$0.4V < V_o < 2.4V$			±1	uA
Input resistance of receiver	RIN	$-7V \leq V_{cM} \leq 12V$	96			kΩ
Receiver short circuit curr-ent	IosR	$0V \leq V_o \leq VCC$	±7		±95	mA



Drive switch characteristics						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input to output propagation delay (low to high)	tDPLH	RDIF=54 Q,CL1=CL2=100pF(see Figure 10 and Figure 11)		12	35	ns
Input to output propagation delay (high to low)	tDPHL			12	35	ns
tDPLH-tDPHLI	tsKEW1			7	10	ns
Rise time/fall time	tDR,tDF			10	25	ns
Receiver switch characteristic						
Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Propagation delay from receiver input to	tRPLH	See Figure 12 and Figure 13 VD ≥ 2.0V; rising and falling edge time Vm ≤ 15ns	20	60	90	ns
The propagation delay from receiver	tRPHL		20	60	90	ns
tRPLH-tRPHL	tsKEW2			7	10	ns



Function table

Receiving function table			
control		input	output
/RE	DE	A-B	RO
0	X	$\geq -10\text{mV}$	H
0	X	$\leq -200\text{mV}$	L
0	X	Open/short circuit	H
1	X	X	Z
X: any level; Z: high impedance.			

Send function table				
control		input	output	
/RE	DE	DI	Y	Z
X	1	1	H	L
X	1	0	L	H
0	0	X	Z	Z
1	0	X	Z(shutdown)	
X: any level; Z: high impedance.				

Additional description

Introduction

The 490/491 is a full-duplex high-speed transceiver for RS-485/RS-422 communication, containing a driver and a receiver. It has fail-safe, overvoltage protection, and overcurrent protection. The 490/491 achieves error-free transmission up to 12Mbps.

fail-safe

The 490/491 guarantees a logic high receiver output if the receiver input is short-circuited or open-circuited, or drivers connected to the terminated transmission line are disabled (idle). This is achieved by setting the receiver input thresholds to -10mV and -200mV , respectively. RO is logic high if the differential receiver input voltage $(A-B) \geq -10\text{mV}$, and RO is logic low if the voltage $(A-B) \leq -200\text{mV}$. Logic high with a minimum noise margin of 50mV can be realized depending on the receiver thresholds. The -10mV to -200mV threshold voltage is in accordance with the EIA/TIA-485 of $\pm 200\text{mV}$.

256 transceivers on the bus

The input impedance of the standard RS485 receiver is $12\text{k}\Omega$ (1 unit load), and the standard driver can drive to 32 unit loads. The receiver of the 490/491 transceiver has an input impedance of 1/8 unit load ($96\text{k}\Omega$), allowing up to 256 transceivers to be connected in parallel on the same communication bus. These devices can be combined arbitrarily, or combined with other 485 transceivers, as long as the total load does not exceed 256 unit loads, they can be connected to the same bus.

Drive output protection

Protection against excessive output current and dissipation by fault or bus contention is provided by overcurrent and overvoltage protection mechanisms, with fast short-circuit throughout the common-mode voltage range (see Typical Operating Characteristics).



SP491 Test circuit

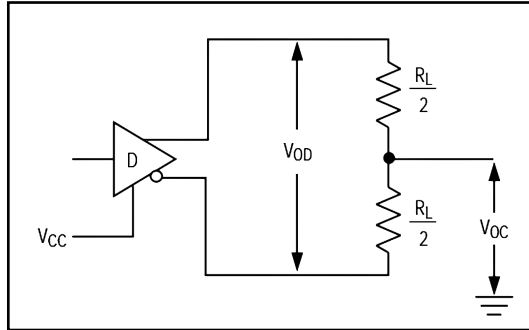


Figure 2: DC test load for the drive

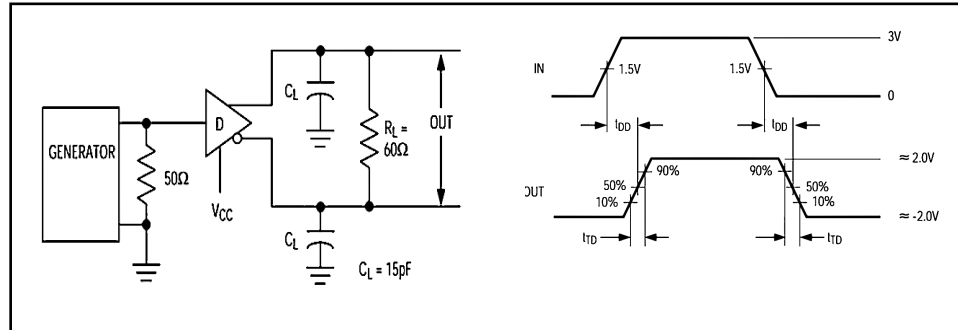


Figure 3 Drive-line Differential Delay and Transit Time

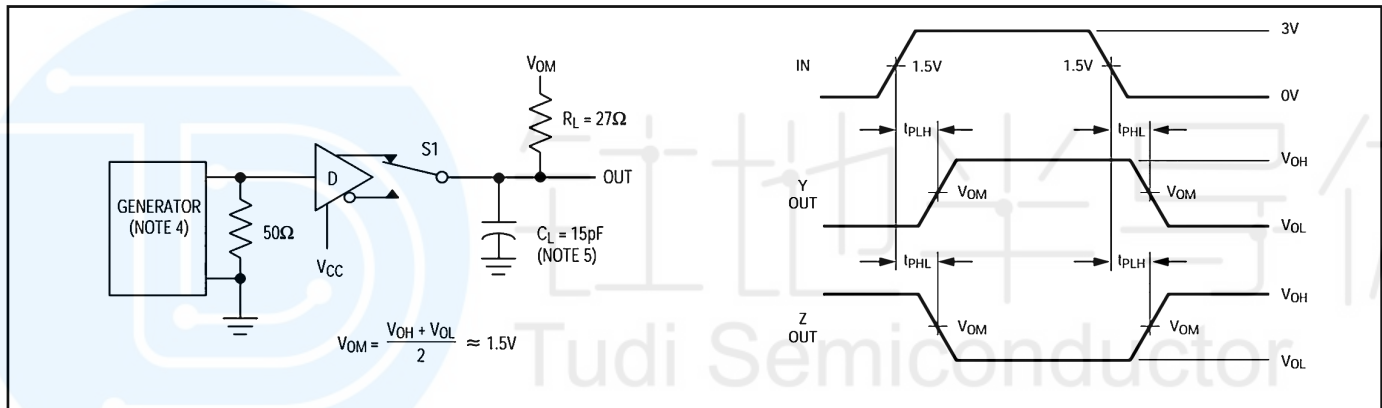


Figure 4 Drive propagation delay

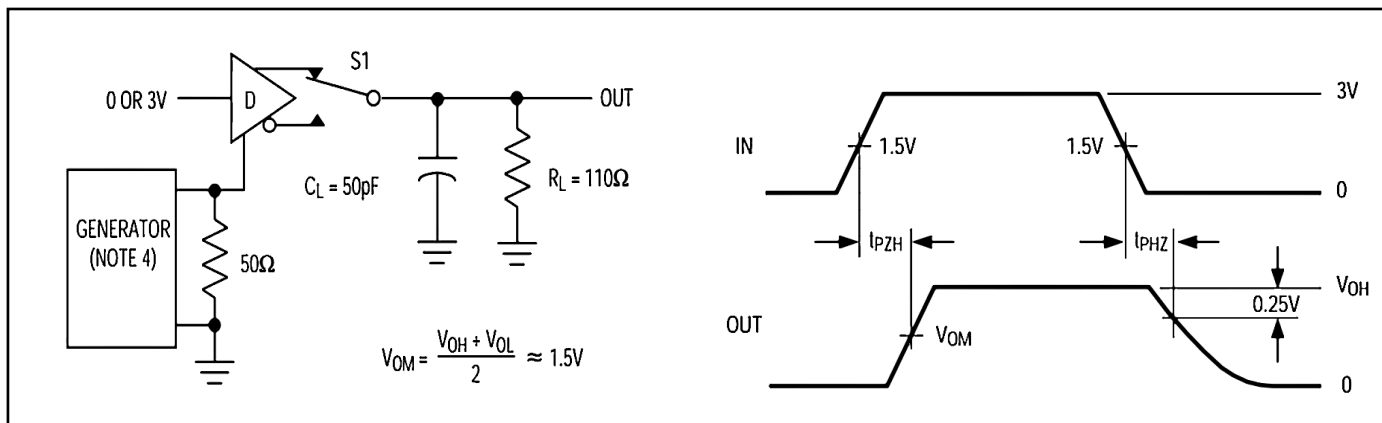


Figure 5 Drive enable and disable time

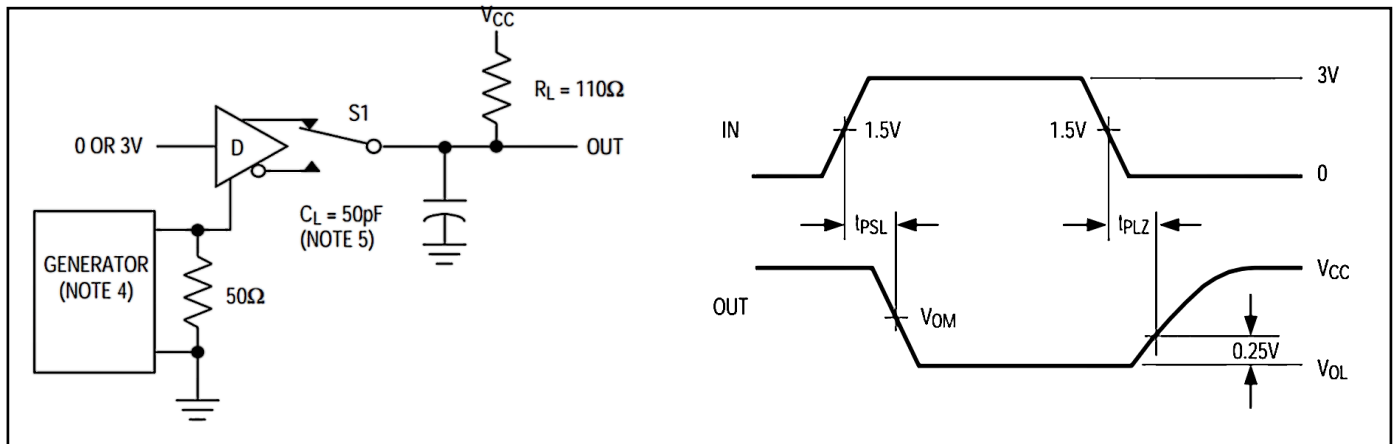


Figure 6 Drive enable and disable time

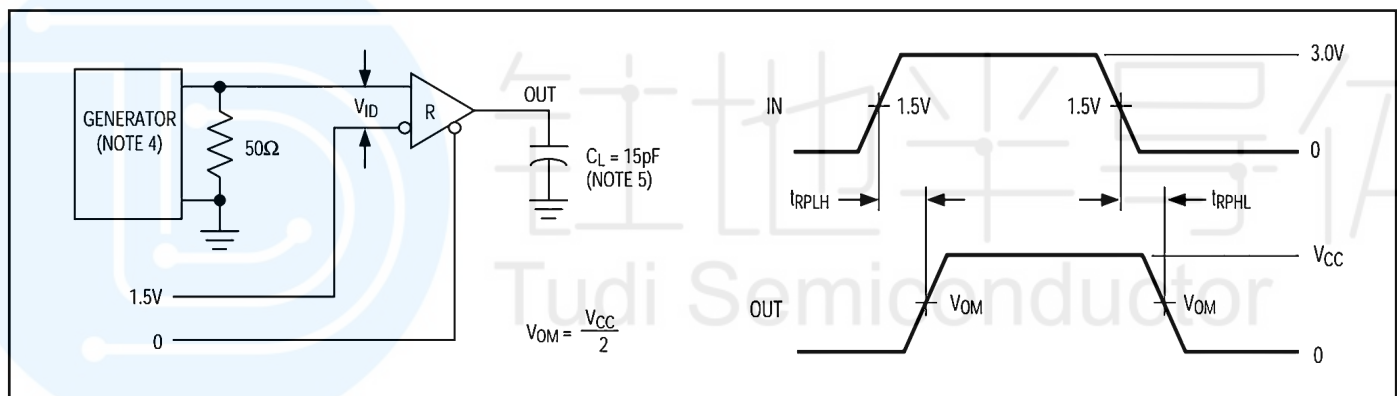
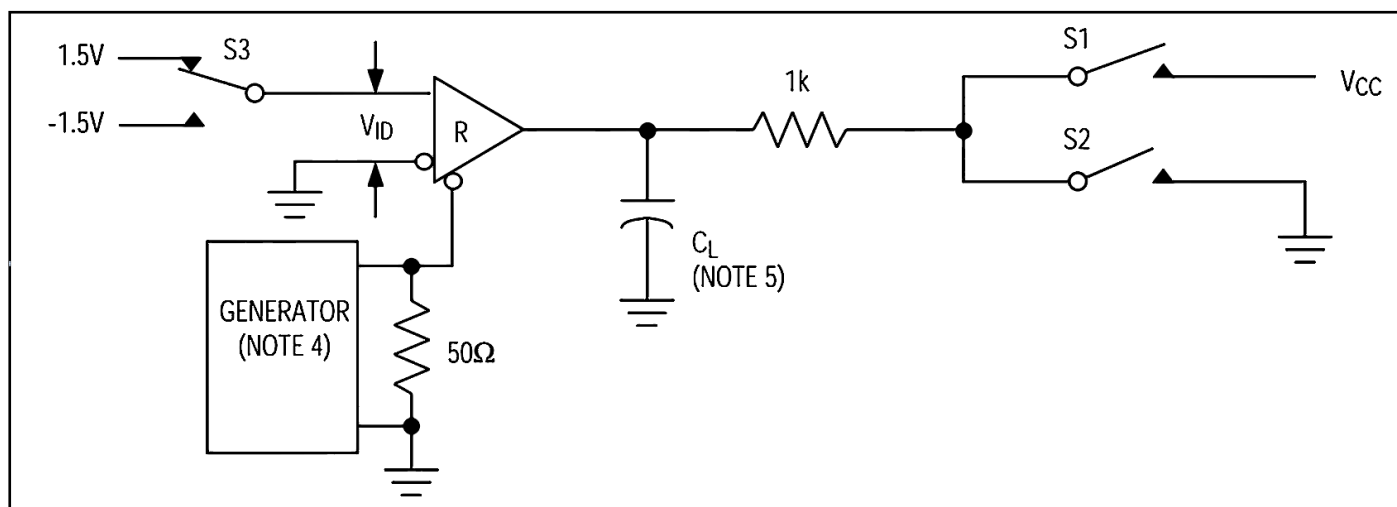


Figure 7: Receiver Propagation Delay Test Circuit



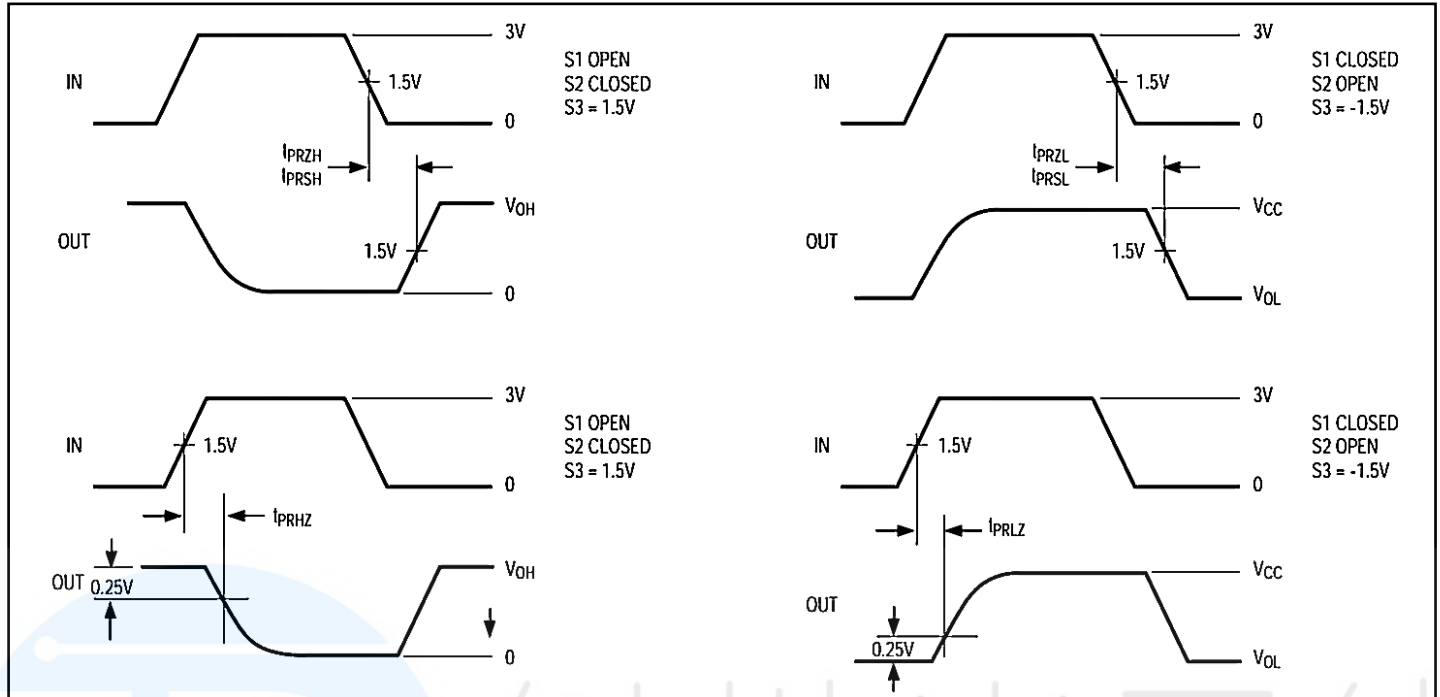


Figure 8 Receive enable and disable time

Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
SP490ECN-L/TR-TUDI	SOP8	Tape,Reel,2500	SP490EC	0°C to 70°C
SP490ECP-TUDI	DIP8	Tube,50,A box of 2000	SP490EC	
SP490EEN-L/TR-TUDI	SOP8	Tape,Reel,2500	SP490EE	- 40°C to 85°C
SP490EEP-TUDI	DIP8	Tube,50,A box of 2000	SP490EE	
SP491ECP-TUDI	DIP14	Tube,25,A box of 1000	SP491ECP	0°C to 70°C
SP491ECN-L/TR-TUDI	SOP14	Tape,Reel,2500	SP491ECN	
SP491EEN-L/TR-TUDI	SOP14	Tape,Reel,2500	SP491EEN	- 40°C to 85°C
SP491EEP-TUDI	DIP14	Tape,Reel,2500	SP491EEP	

SP490 Test circuit

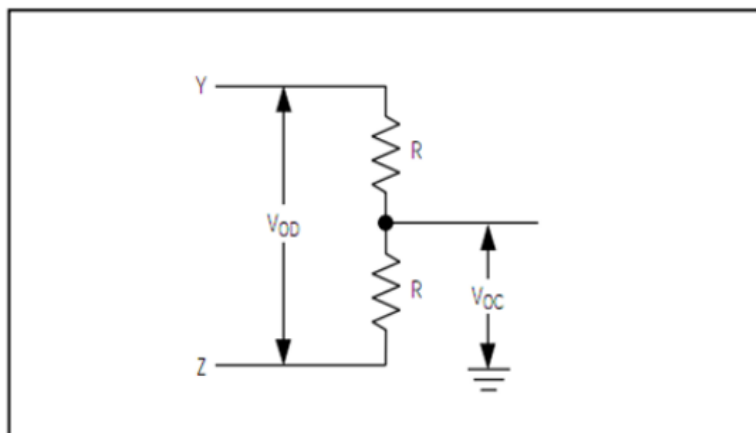


Figure9 DCTestLoadoftheDriver

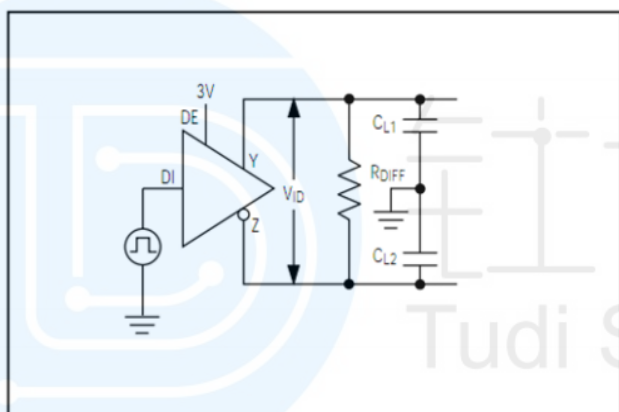


Figure10 DriverTimingTestCircuit

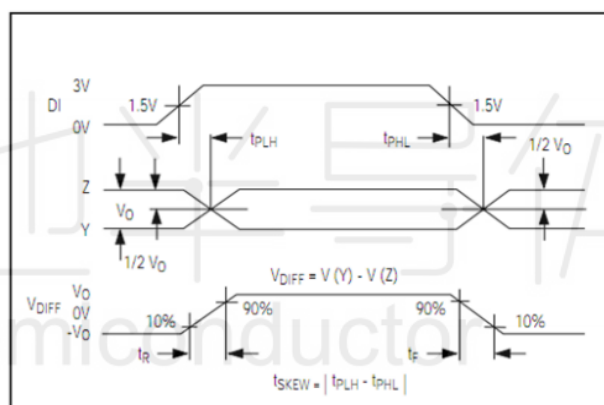


Figure11 PropagationDelayofDriver

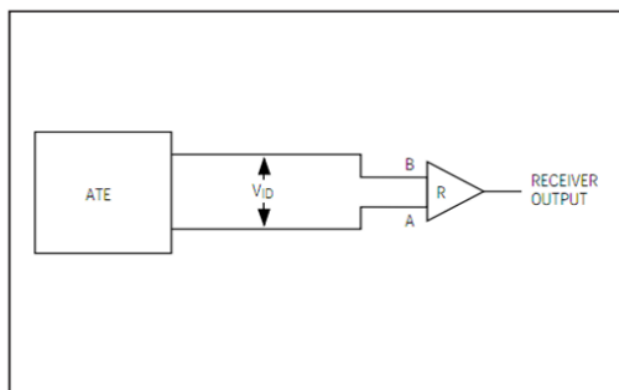


Figure12 ReceiverPropagationDelayTestCircuit

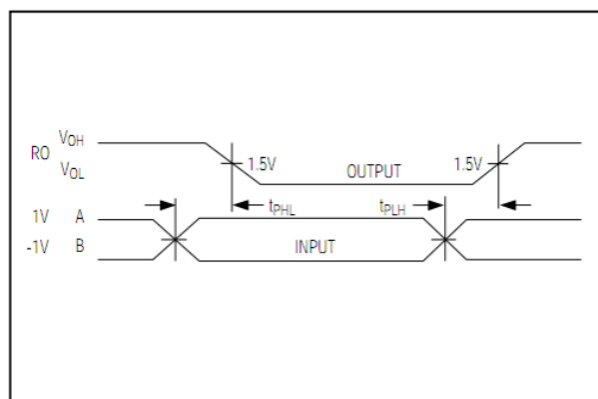
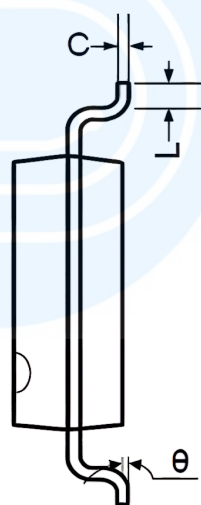
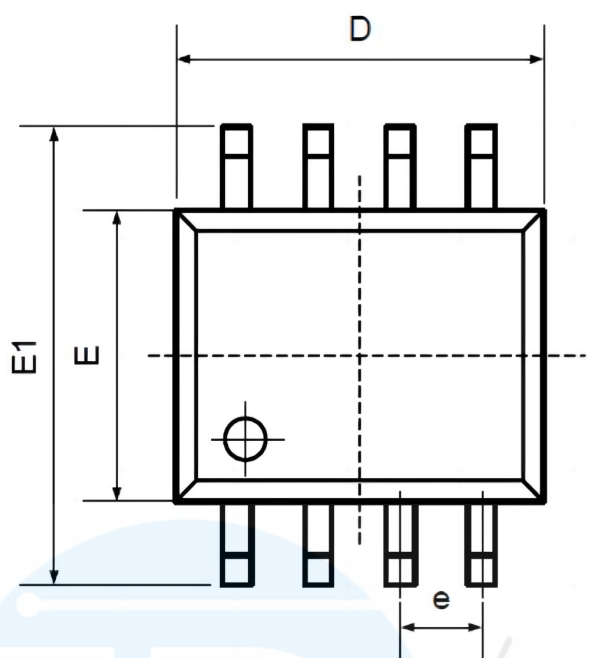
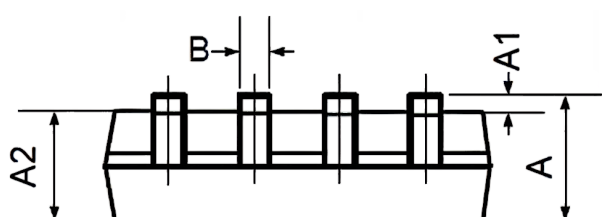


Figure13 ReceiverPropagationDelaySequence

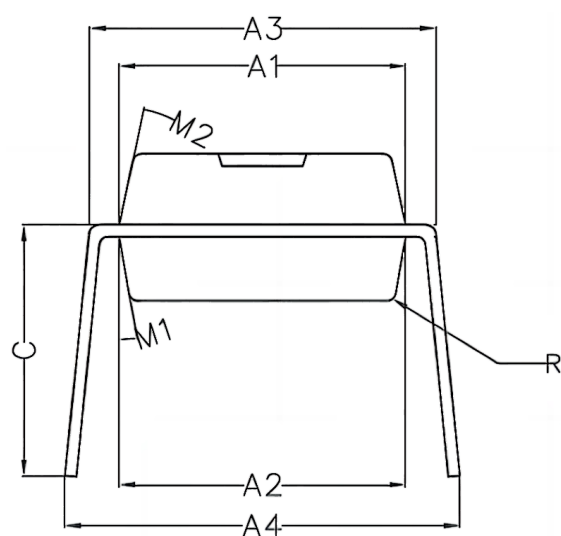
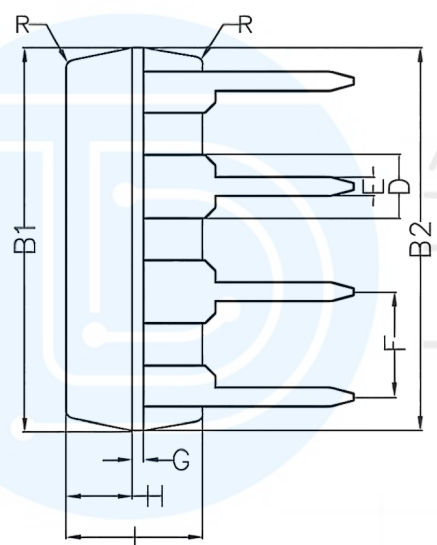
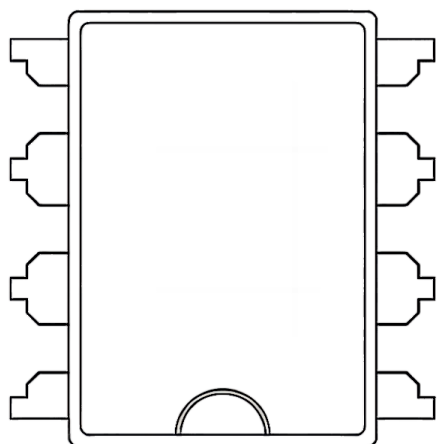
Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



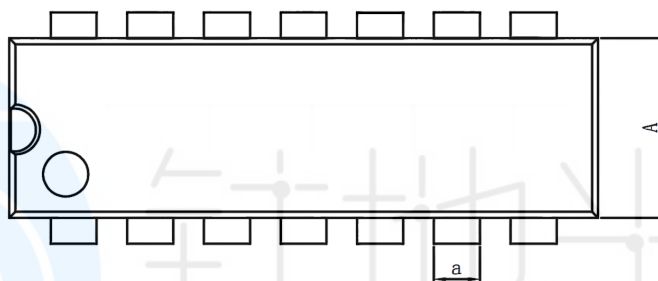
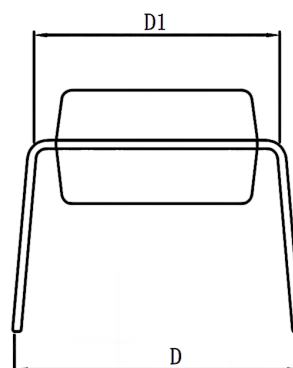
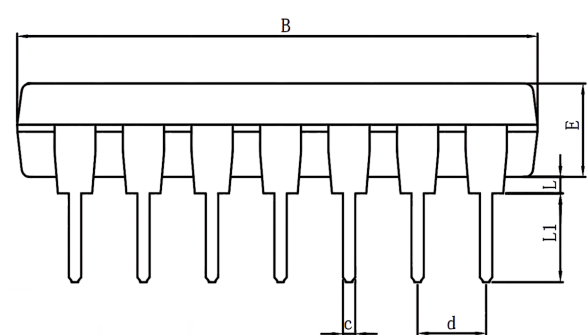
Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°



Package DIP14



DIM.	MIN	TYP	MAX	DIM.	MIN	TYP	MAX
A	6.100	6.300	6.680	a	1.504	1.524	1.544
B	18.940	19.200	19.560	C	0.437	0.457	0.477
D	8.200	8.700	9.200	d	2.530	2.540	2.550
D1	7.42	7.62	7.82	L	0.500	—	0.800
E	3.100	3.300	3.550	L1	3.000	3.200	3.600



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