

1.Description

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications

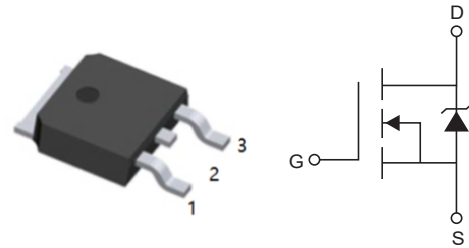
2.Features

- $V_{DS(V)} = 100V$
- $I_D = 17A$
- $R_{DS(ON)} = 105m\Omega (V_{GS} = 10V)$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view



4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, $V_{GS} = 10V$	$T_C = 25^\circ C$	I_D	17	A
Continuous Drain Current, $V_{GS} = 10V$	$T_C = 100^\circ C$		12	A
Pulsed Drain Current ① ⑤		I_{DM}	60	A
Power Dissipation	$T_C = 25^\circ C$	P_D	79	W
Linear Derating Factor			0.53	W/ $^\circ C$
Gate-to-Source Voltage		V_{GS}	± 16	V
Single Pulse Avalanche Energy ② ⑤		E_{AS}	150	mJ
Avalanche Current ① ⑤		I_{AR}	9	A
Repetitive Avalanche Energy ① ⑤		E_{AR}	7.9	mJ
Peak Diode Recovery dv/dt ③		dv/dt	5	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	$^\circ C$
Soldering Temperature, for 10 seconds			300 (1.6mm from case)	$^\circ C$



5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case	$R_{\theta JC}$		1.9	°C/W
Junction-to-Ambient (PCB Mount) **	$R_{\theta JA}$		50	°C/W
Junction-to-Ambient	$R_{\theta JA}$		110	°C/W



6. Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	$I_D=1\text{mA}$, Reference to 25°C		0.122		V/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=10\text{A}$ ④			105	m Ω
		$V_{GS}=5\text{V}$, $I_D=10\text{A}$ ④			125	
		$V_{GS}=4\text{V}$, $I_D=9\text{A}$ ④			155	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1		2	V
Forward Transconductance	g_{FS}	$V_{DS}=25\text{V}$, $I_D=9\text{A}$ ⑤	7.7			S
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$			25	μA
		$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=150^\circ\text{C}$			250	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=16\text{V}$			100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-16\text{V}$			-100	
Total Gate Charge	Q_g	$I_D=9\text{A}$			34	nC
Gate-to-Source Charge	Q_{gs}	$V_{DS}=80\text{V}$, $V_{GS}=5\text{V}$			4.8	
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig. 6 and 13 ④⑤			20	
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=50\text{V}$, $I_D=9\text{A}$ $R_G=6\Omega$, $V_{GS}=5\text{V}$ $R_D=5.5\Omega$, See Fig. 10 ④⑤		7.2		ns
Rise Time	t_r			53		ns
Turn-Off Delay Time	$t_{D(off)}$			30		ns
Fall Time	t_f			26		ns
Internal Drain inductance	L_D	Between lead, 6mm (0.25in.) from package and center of die contact		4.5		nH
Internal Source inductance	L_S			7.5		
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$ $f = 1.0\text{MHz}$, See Fig. 5 ⑤		800		pF
Output Capacitance	C_{oss}			160		pF
Reverse Transfer Capacitance	C_{rss}			90		pF



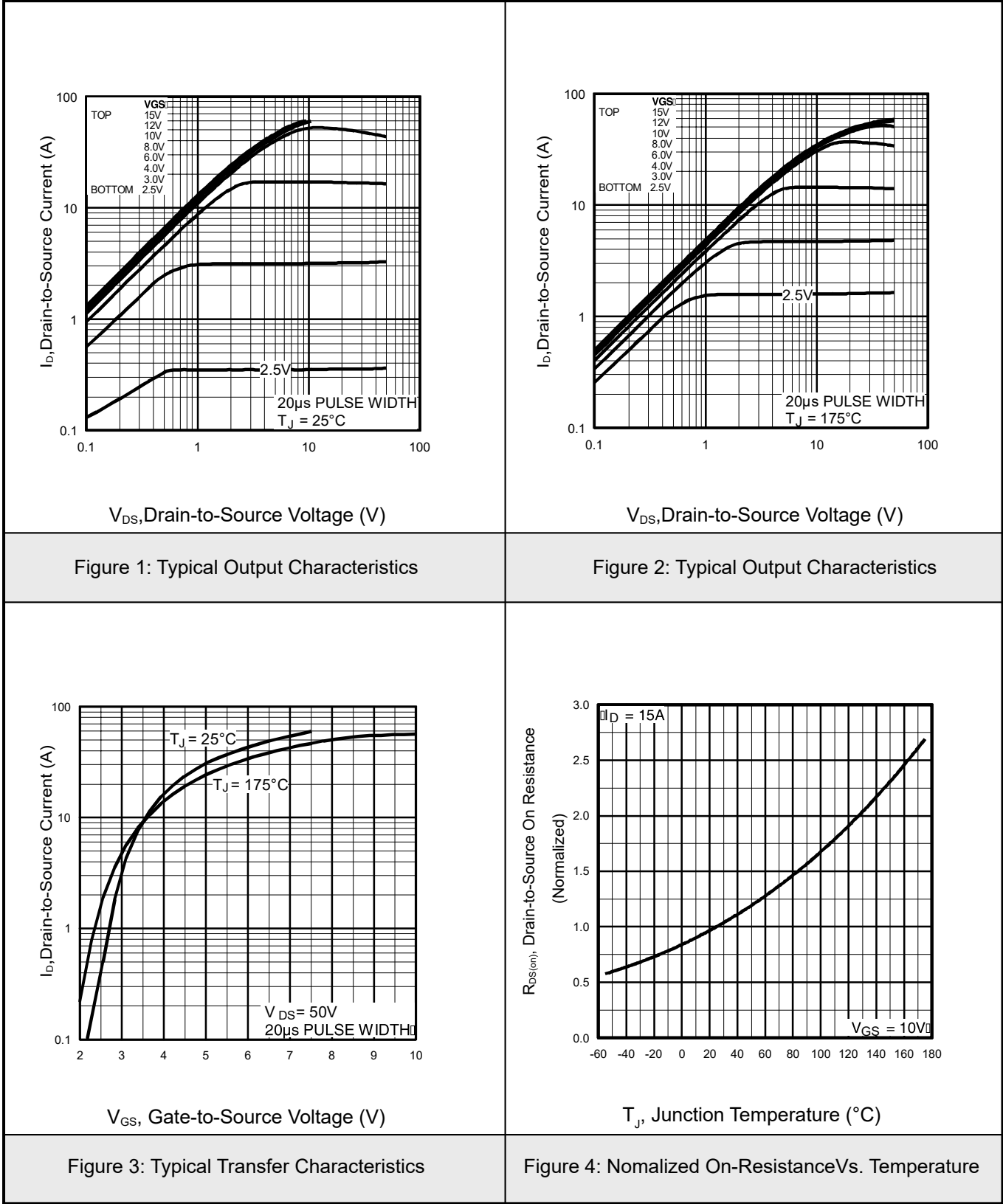
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			17	A
Pulsed Source Current (Body Diode) ① ⑤	I_{SM}				60	
Diode Forward Voltage	V_{SD}	$T_J=25^\circ\text{C}$, $I_S=9\text{A}$, $V_{GS}=0\text{V}$ ④			1.3	V
Reverse Recovery Time	t_{rr}	$T_J=25^\circ\text{C}$, $I_F=9\text{A}$ $di/dt=100\text{A}/\mu\text{s}$ ④ ⑤		140	210	ns
Reverse Recovery Charge	Q_{rr}			740	1100	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD}=25\text{V}$, starting $T_J=25^\circ\text{C}$, $L=3.1\text{mH}$
 $R_G=25\Omega$, $I_{AS}=9\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 9.0\text{A}$, $di/dt \leq 540\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$
- ⑤ Uses IRL530N data and test conditions.
- ⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.

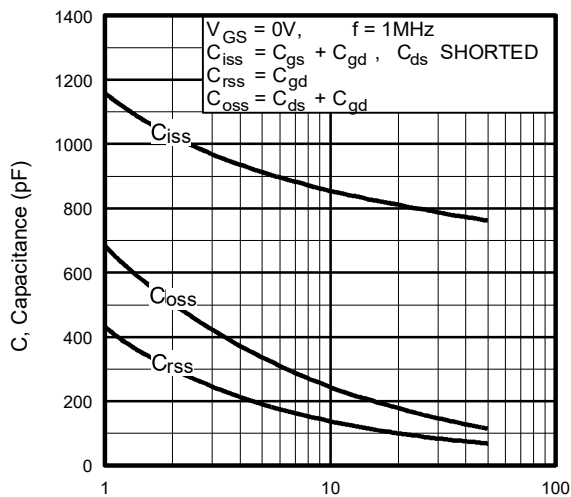


7.1 Typical Characteristics



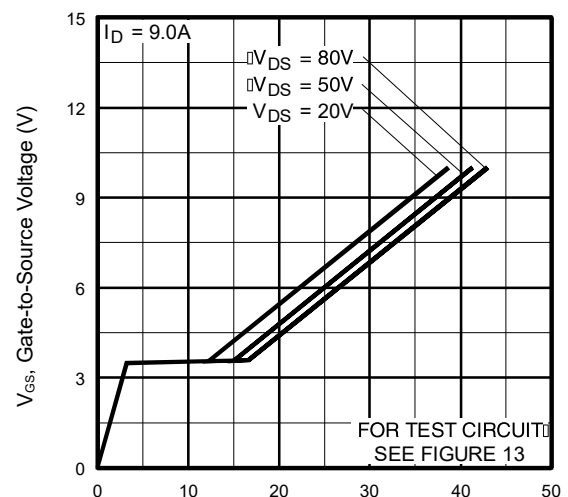


7.2 Typical Characteristics



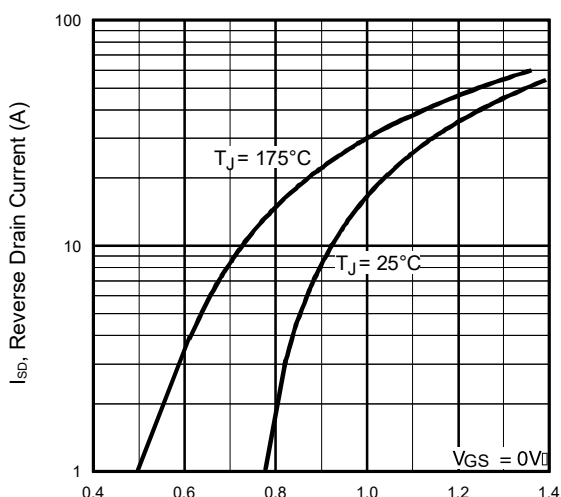
V_{DS} , Drain-to-Source Voltage (V)

Figure 5: Typical Capacitance Vs. Drain-to-Source Voltage



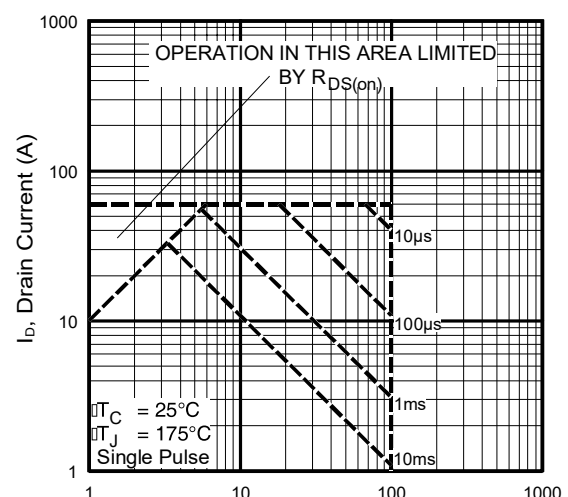
Q_G , Total Gate Charge (nC)

Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD} , Source-to-Drain Voltage (V)

Figure 7: Typical Source-Drain Diode Forward Voltage

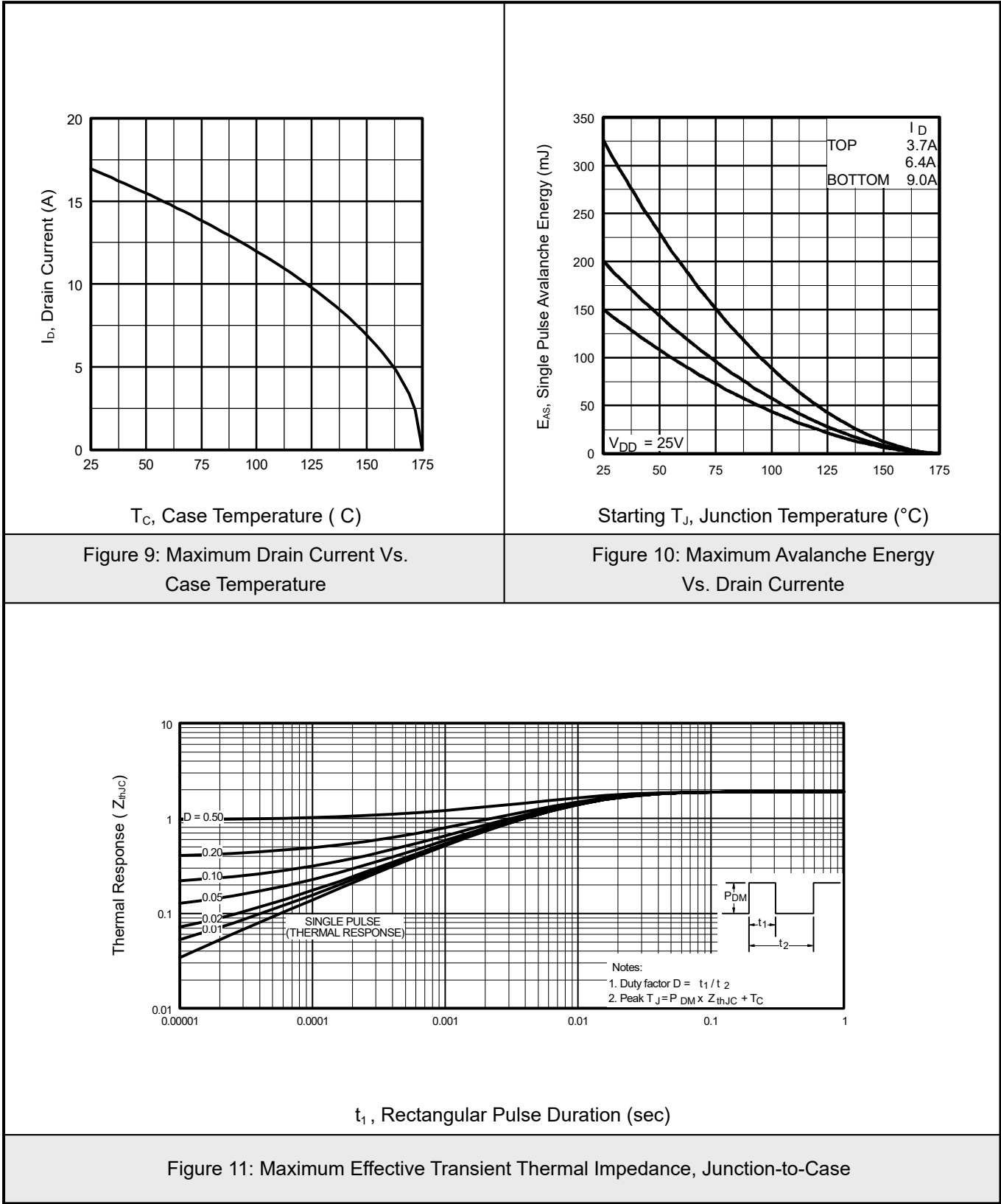


V_{DS} , Drain-to-Source Voltage (V)

Figure 8: Maximum Safe Operating Area



7.3 Typical Characteristics





7.4Typical Characteristics

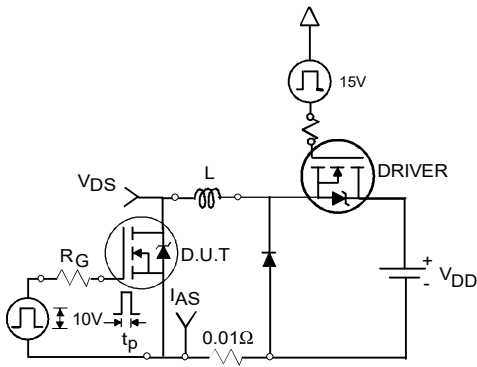


Figure 12a: Unclamped Inductive Test Circuit

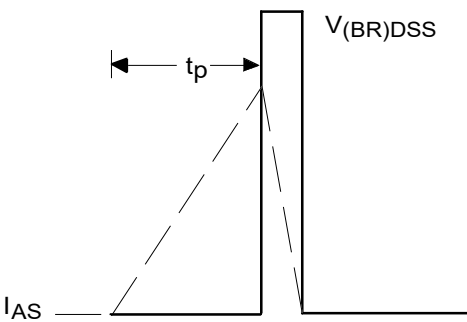


Figure 12b: Unclamped Inductive Waveforms

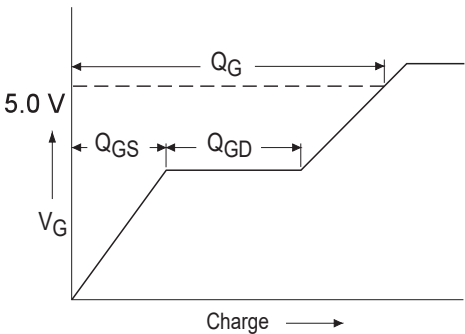


Figure 13a: Basic Gate Charge Waveform

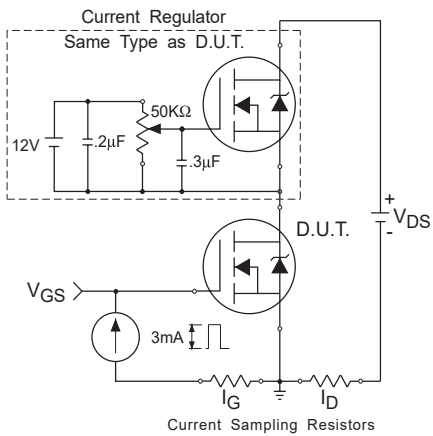
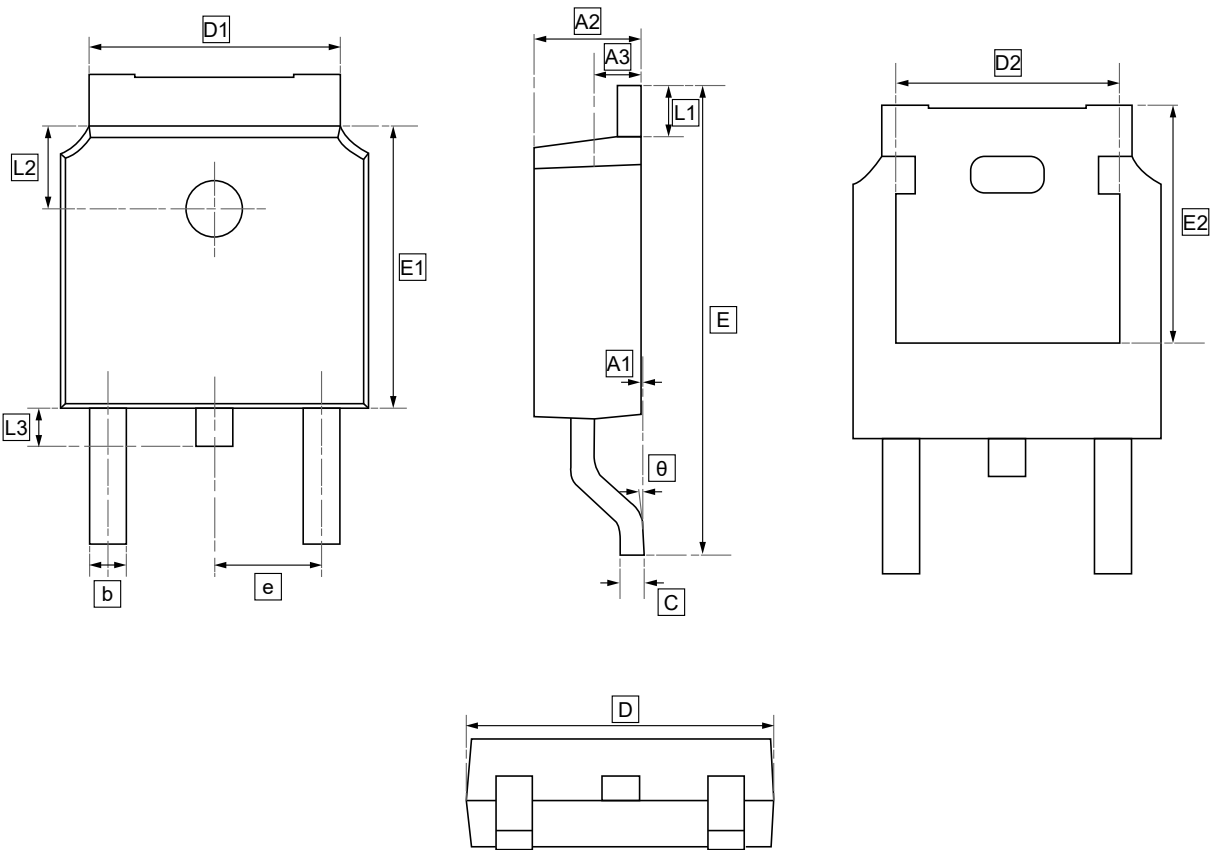


Figure 13b: Gate Charge Test Circuit



8.TO-252 Package Outline Dimensions

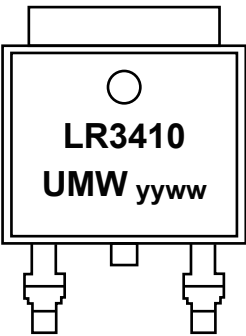


DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286 BSC	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRLR3410TR	TO-252	2500	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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