UMW FDD86113LZ

100V N-Channel MOSFET

1.Description

This N-Channel logic Level MOSFETs are produced using advanced process that incorporates Shielded Gate technology. This process has been optimized for the onstate resistance and yet maintain superior switching performance.

2.1Features

- $V_{DS\,(V)}$=100V
- I_D=5.5A
- $R_{DS(ON)}$<104mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<156mΩ(V_{GS}=4.5V)

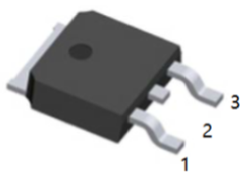
2.2Features

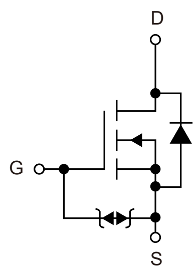
- HBM ESD protection level > 6 kV typical (Note 4)
- High perf ormance trench technology for extremely low $R_{DS(ON)}$
- Shielded Gate MOSFET Technology
- High power and current handling capability in a widely usedsurface mount package

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_C= 25°C

Parameter			Symbol	Rating	Units
Drain to Source Voltage			V_{DS}	100	V
Gate to Source Voltage			V_{GS}	±20	V
Drain Current - Continuous	T_C=25°C		I_D	5.5	A
- Continuous	T_A=25°C	(Note 1a)		4.2	A
- Pulsed				15	A
Single Pulse Avalanche Energy		(Note 3)	E_{AS}	12	mJ
Power Dissipation	T_C=25°C		P_D	29	W
Power Dissipation	T_A=25°C	(Note 1a)		3.1	W
Storage Temperature Range			T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Case (Note 1)	$R_{\theta JC}$	4.3	°C/W
Thermal Resistance, Junction to Ambient (Note 1a)	$R_{\theta JA}$	96	°C/W

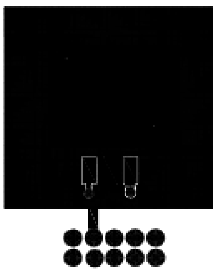
6.Electrical Characteristic (T$_J$=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	100			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		72		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{DS}=0V			1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
On Characteristics						
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.6	3	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-5		mV/°C
Static Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.2A		80	100	mΩ
		V_{GS}=4.5V, I_D=3.4A		110	140	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=4.2A		9		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz		213	285	pF
Output Capacitance	C_{oss}			55	75	pF
Reverse Transfer Capacitance	C_{rss}			2.4	5	pF
Gate Resistance	R_g			1.4		Ω
Switching Characteristics						
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=50V, I_D=4.2A V_{GS}=10V, R_{GEN}=6Ω		3.6	10	ns
Rise Time	t_r			1.3	10	ns
Turn-Off DelayTime	$t_{D(off)}$			9.7	20	ns
Fall Time	t_f			1.6	10	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS}=0V to 10V; V_{DD}=50V, I_D=4.2A		3.7	6	nC
Total Gate Charge	$Q_{g(TOT)}$	V_{GS}=0V to 4.5V		1.9	3	nC
Gate to Source Charge	Q_{gs}			0.6		nC
Gate to Drain "Miller" Charge	Q_{gd}			0.7		nC

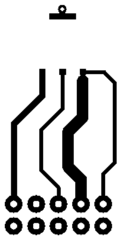
Drain–Source Diode Characteristics						
Source to Drain Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=4.2A (Note 2)		0.88	1.3	V
		V_{GS}=0V, I_S=1.7A (Note 2)		0.8	1.2	V
Reverse Recovery Time	t_{rr}	I_F=4.2A, di/dt=100A/μs		31	49	ns
Reverse Recovery Charge	Q_{rr}			20	33	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 96°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Starting T_J=25°C, L=1mH, I_{AS}=5 A, V_{DD}=90 V, V_{GS}=10 V.
4. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

7.1Typical characteristic

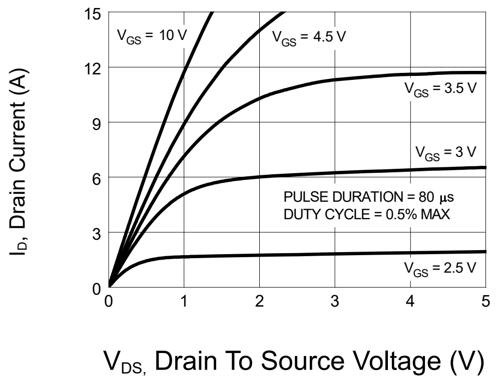


Figure 1: On-Region Characteristics

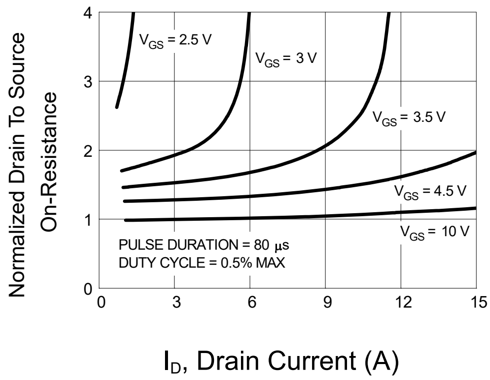


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

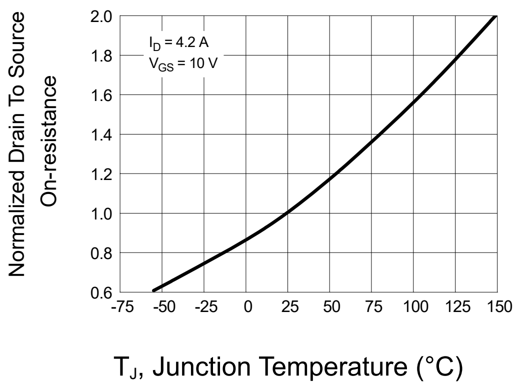


Figure 3: Normalized On Resistance vs Junction Temperature

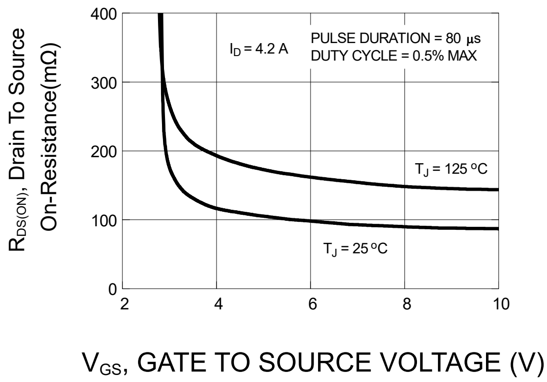


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

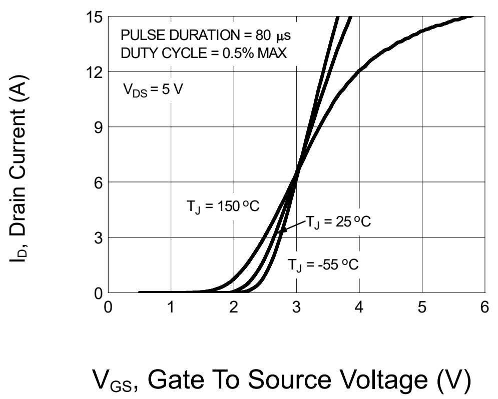


Figure 5: Transfer Characteristics

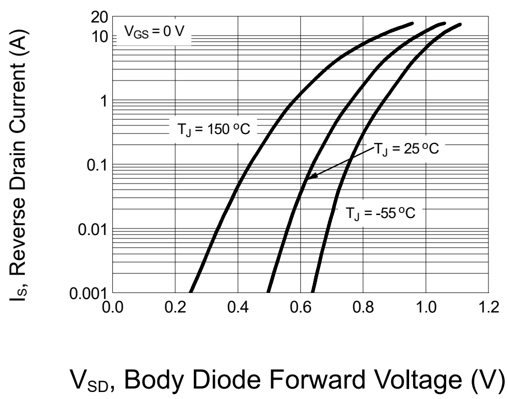


Figure 6: Source to Drain Diode Forward Voltage vs Source Current

7.2Typical characteristic

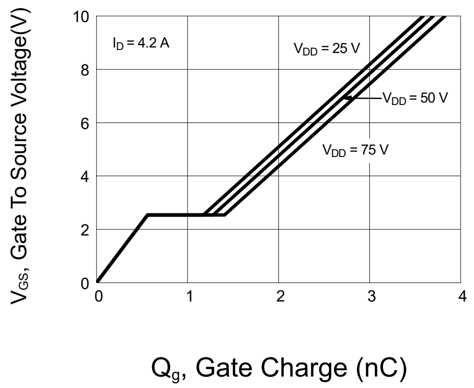


Figure 7: Gate Charge Characteristics

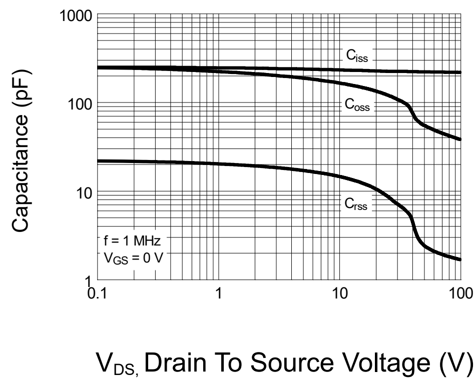


Figure 8: Capacitance vs Drain to Source Voltage

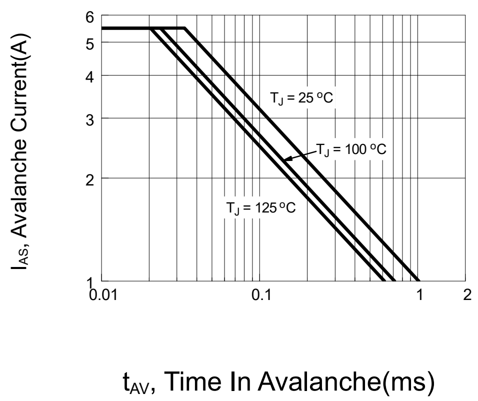


Figure 9: Unclamped Inductive Switching Capability

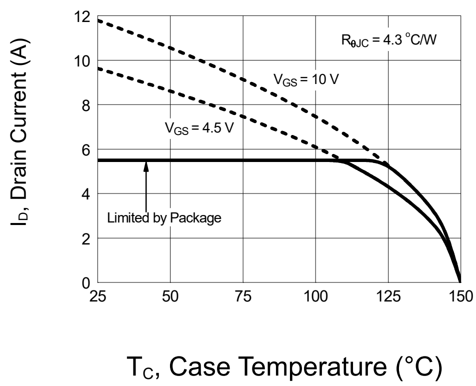


Figure 10: Maximum Continuous Drain Current vs Case Temperature

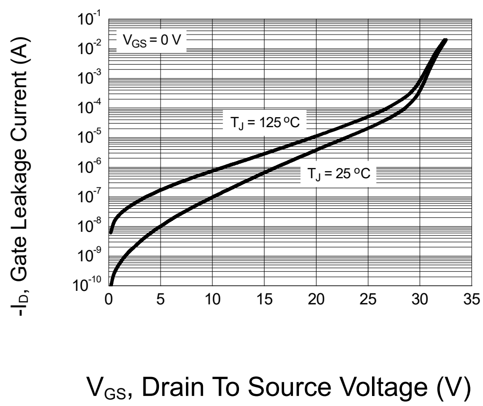


Figure 11: Gate Leakage Current vs Gate to Source Voltage

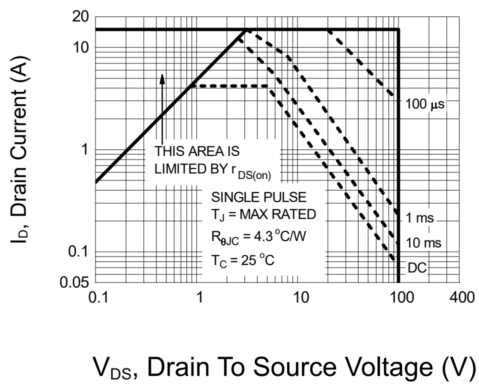


Figure 12: Forward Bias Safe Operating Area

7.3Typical characteristic

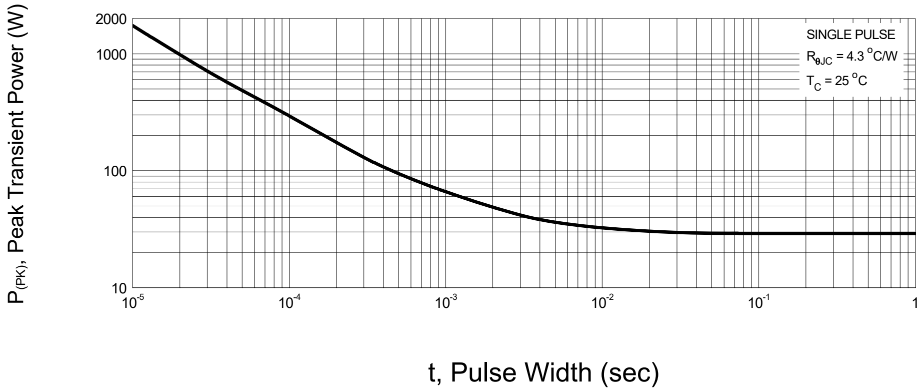


Figure 13: Single Pulse Maximum Power Dissipation

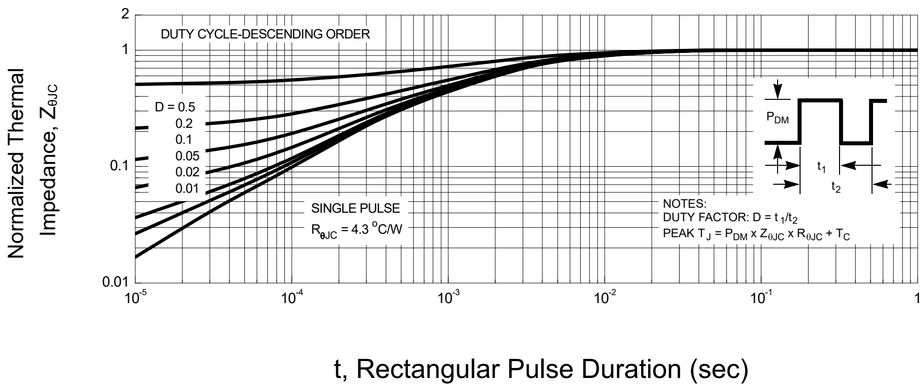
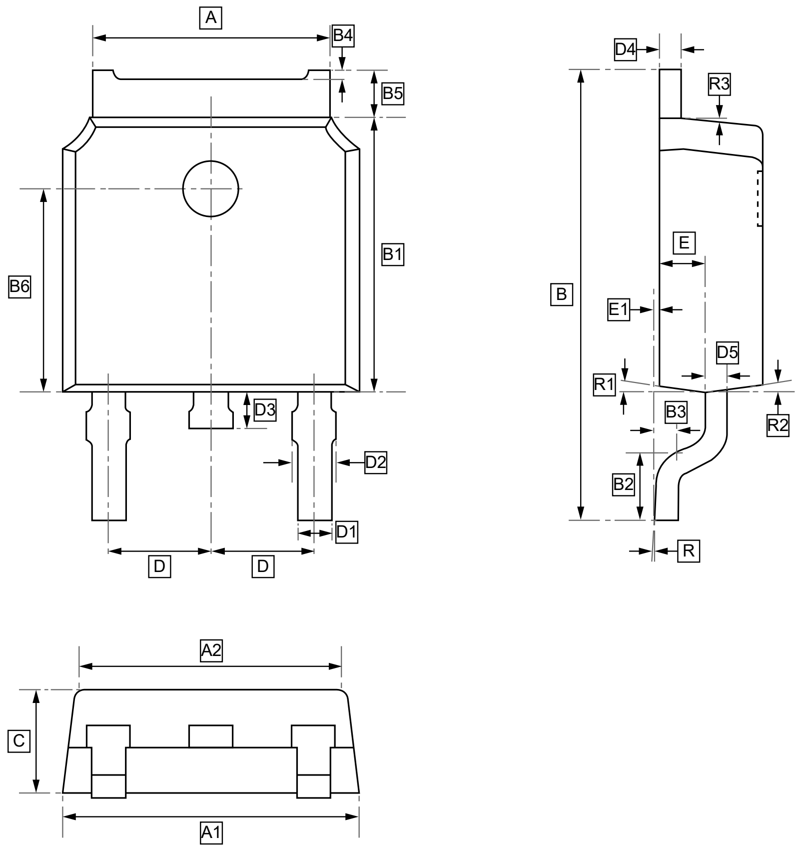


Figure 14: Junction-to-Case Transient Thermal Response Curve

8.TO-252 Package Outline Dimensions

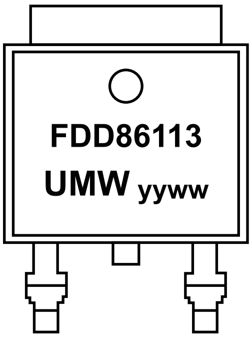


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	B3	B4	B5	B6	C	D
Min	5.1	6.4	5.6	9.5	5.9	1.35	0.4	0.1	0.85	4.35	2.15	2.286
Max	5.5	6.8	6.0	10.3	6.3	1.65	0.6	(typ.)	1.05	4.65	2.45	(typ.)

Symbol	D1	D2	D3	D4	D5	E	E1	R	R1	R2	R3
Min	0.66	0.81	0.65	0.42	0.42	0.86	0.05	0°	7°	7°	7°
Max	0.86	1.01	0.95	0.58	0.58	1.16	0.05	6°	(typ.)	(typ.)	(typ.)

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD86113LZ	TO-252	2500	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.