

1.Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically.

2.2Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Surface Mount

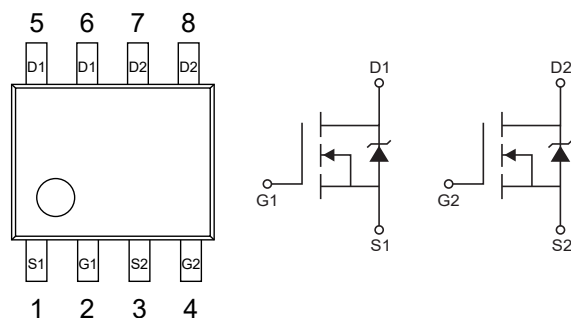
2.1Features

- $V_{DS(V)}=50V$
- $I_D=3A$
- $R_{DS(ON)}<0.09\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<0.14\Omega(V_{GS}=4.5V)$

3.Pinning information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter		Symbol	Rating	Units
Continuous Drain Current, $V_{GS}=10V$	$T_A=25^{\circ}C$	I_D	3	A
Continuous Drain Current, $V_{GS}=10V$	$T_A=100^{\circ}C$		2.3	A
Pulsed Drain Current ①		I_{DM}	10	A
Power Dissipation	$T_A=25^{\circ}C$	P_D	2	W
Linear Derating Factor			0.016	W/ $^{\circ}C$
Gate-to-Source Voltage		V_{GS}	± 20	V
Peak Diode Recovery dv/dt ②		dv/dt	4.5	V/nS
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}C$



5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		62.5	°C/W



6. Electrical Characteristics $T_J=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	50			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	$I_D=1\text{mA}$, Reference to 25°C		0.049		V/ $^{\circ}\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3\text{A}$ ③		0.07	0.09	Ω
		$V_{GS}=4.5\text{V}$, $I_D=1.5\text{A}$ ③		0.11	0.14	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1		3	V
Forward Transconductance	g_{FS}	$V_{DS}=15\text{V}$, $I_D=3\text{A}$ ③		3.8		S
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$			2	μA
		$V_{DS}=40\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$			25	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=20\text{V}$			100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-20\text{V}$			-100	
Total Gate Charge	Q_g	$I_D=2\text{A}$		12	30	nC
Gate-to-Source Charge	Q_{gs}	$V_{DS}=25\text{V}$		1.2		
Gate-to-Drain ("Miller") Charge	Q_{gd}	$V_{GS}=10\text{V}$ ③		3.5		
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=25\text{V}$		9	20	ns
Rise Time	t_r	$I_D=1\text{A}$		8	20	ns
Turn-Off Delay Time	$t_{D(off)}$	$R_G=6\Omega$		45	70	ns
Fall Time	t_f	$R_D=25\Omega$ ③		25	50	ns
Internal Drain inductance	L_D	Between lead, 6mm (0.25in.) from package and center of die contact		4		nH
Internal Source inductance	L_S			6		
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$		290		pF
Output Capacitance	C_{oss}	$V_{DS}=25\text{V}$		140		pF
Reverse Transfer Capacitance	C_{rss}	$f=1.0\text{MHz}$		37		pF



Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			2	A
Pulsed Source Current (Body Diode) ①	I_{SM}				12	
Diode Forward Voltage	V_{SD}	$T_J=25^{\circ}\text{C}, I_S=1.5\text{A}, V_{GS}=0\text{V}$ ③			1.2	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, I_F=1.5\text{A}$		70	100	ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$ ③		110	170	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② $I_{SD} \leq 1.8\text{A}$, $di/dt \leq 90\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^{\circ}\text{C}$.
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.



7.1Typical Characterisitics

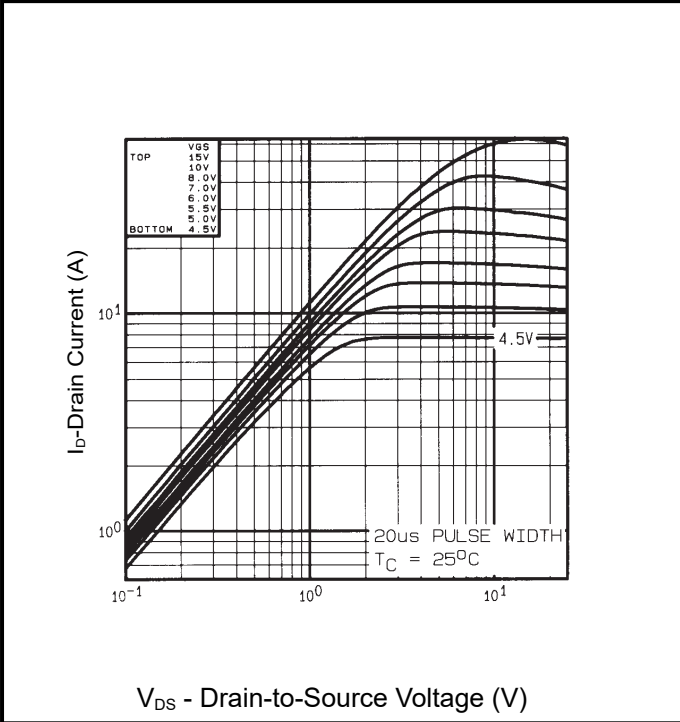


Fig 1. Typical Output Characteristics

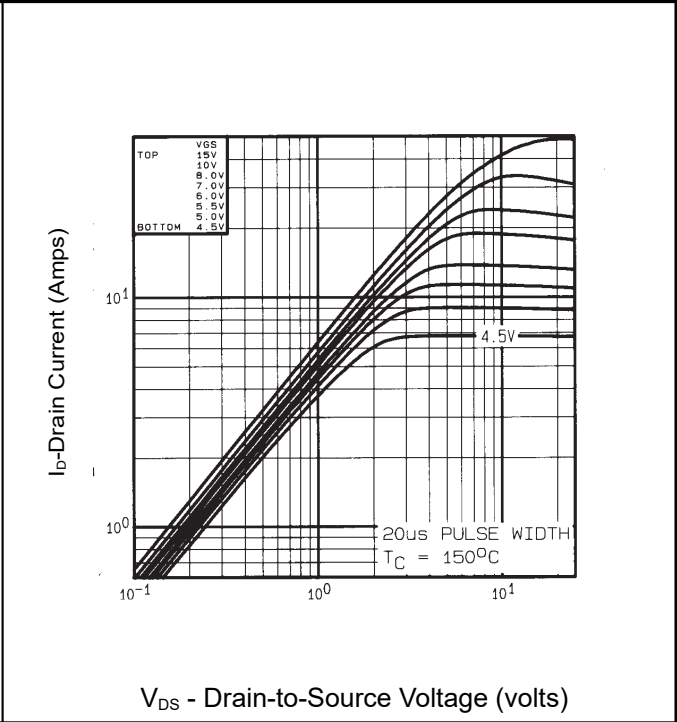


Fig 2. Typical Output Characteristics

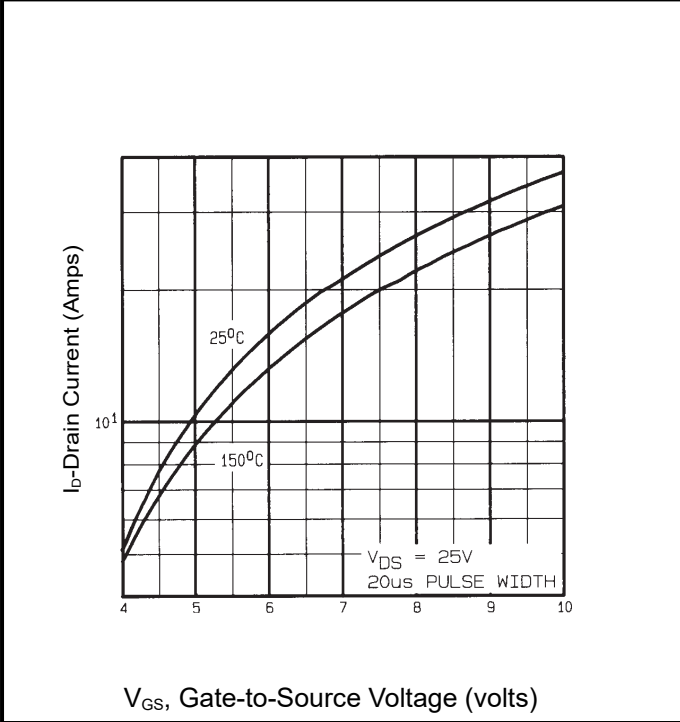


Fig 3. Typical Transfer Characteristics

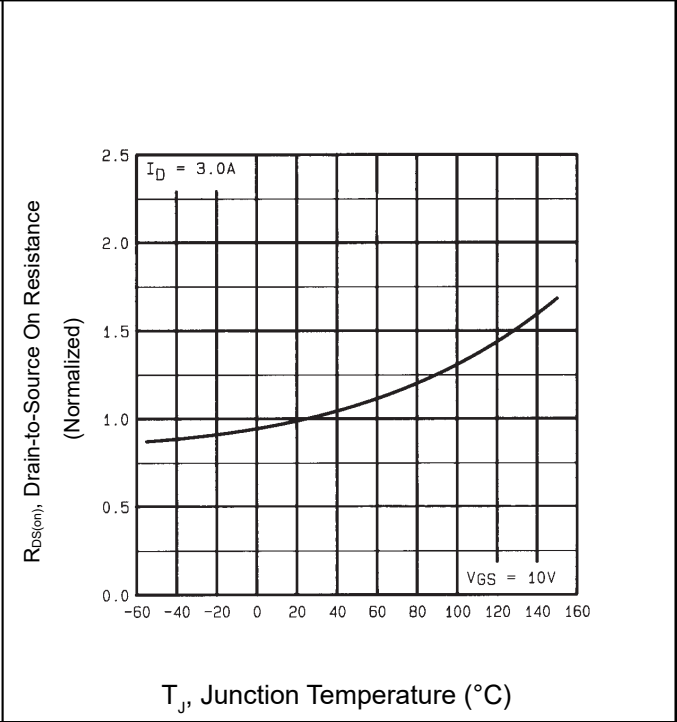
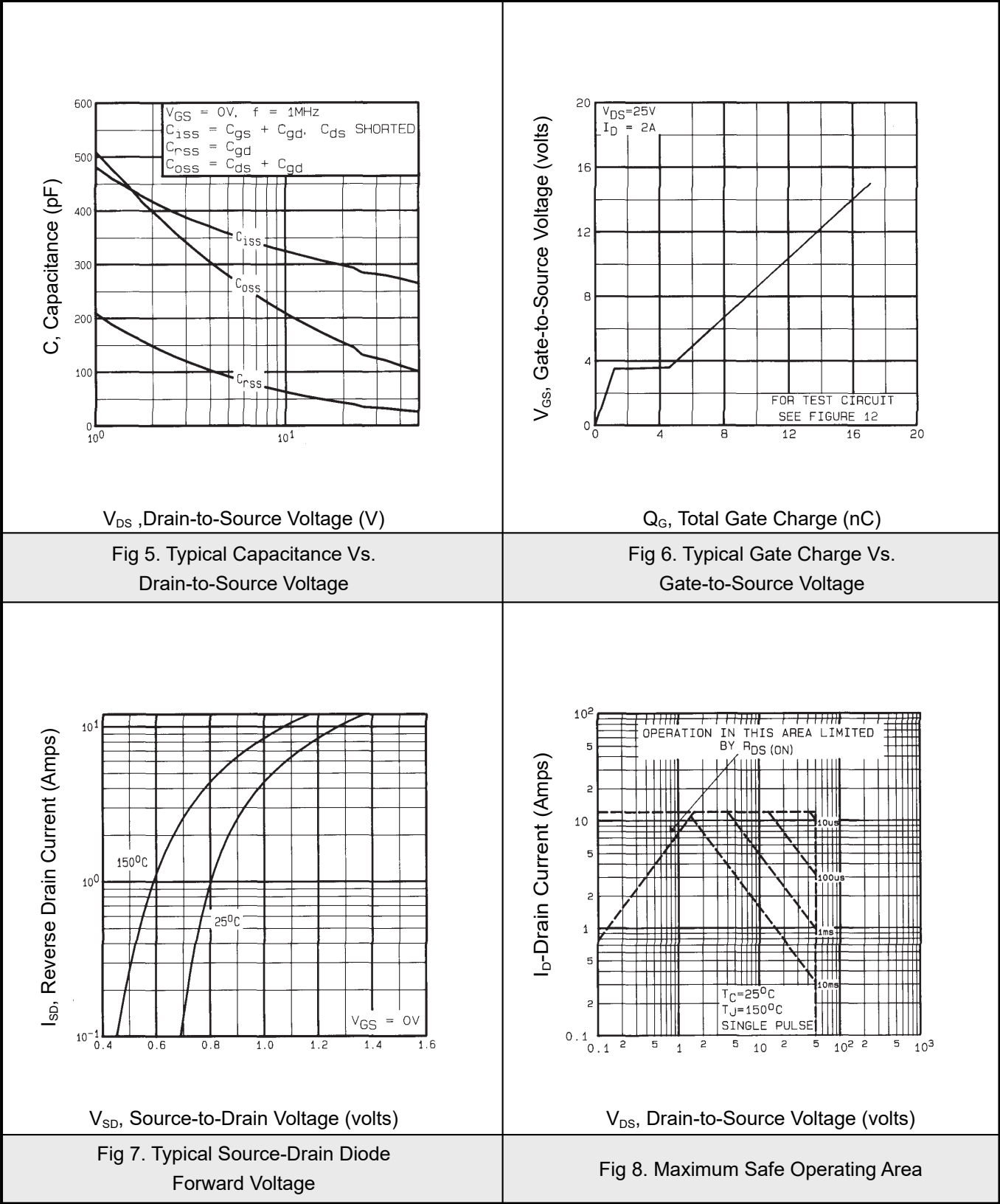


Fig 4. Nomalized On-ResistanceVs. Temperature



7.2Typical Characterisitics





7.3Typical Characterisitics

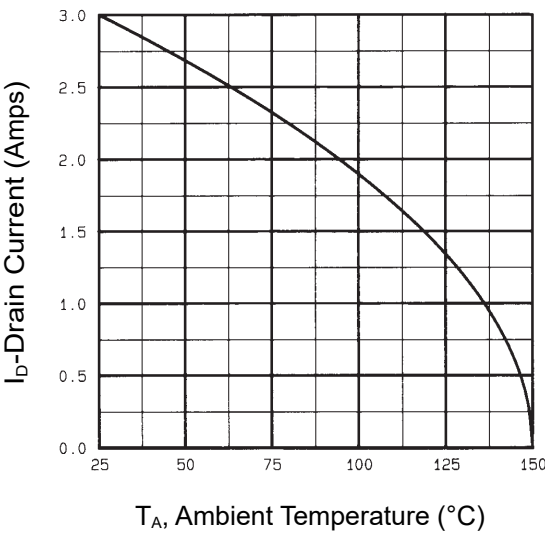


Fig 9. Maximum Drain Current Vs.AmbientTemperature

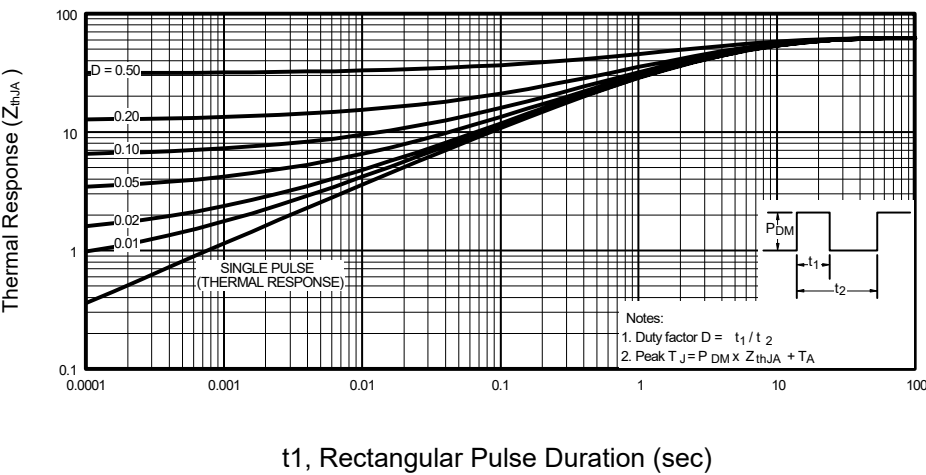


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



7.4Typical Characterisitics

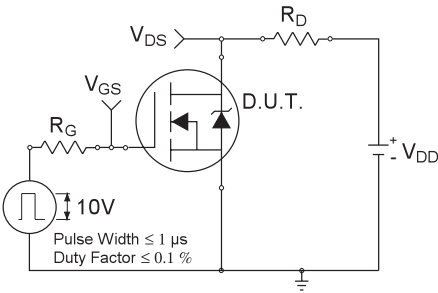


Fig 11a. Switching Time Test Circuit

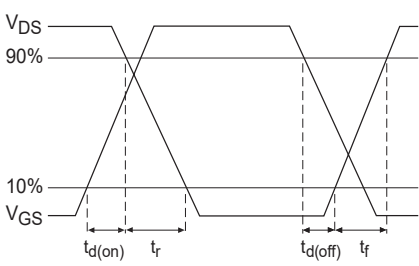


Fig 11b. Switching Time Waveforms

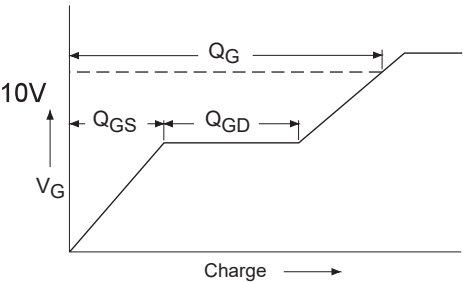


Fig 12a. Basic Gate Charge Waveform

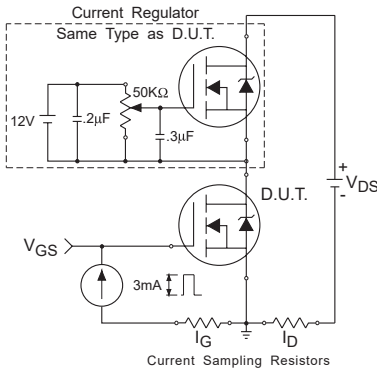
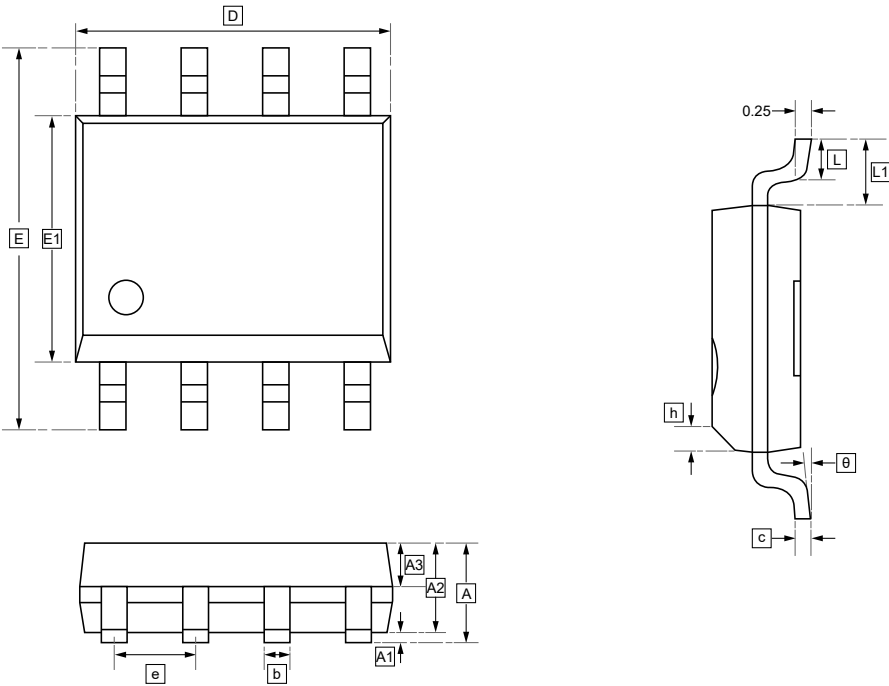


Fig 12b. Gate Charge Test Circuit



8.SOP-8 Package Outline Dimensions



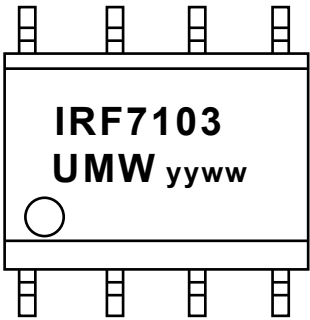
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7103TR	SOP-8	3000	Tape and reel



10.Disclaimer

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