UMW IPD135N03LG

30V N-Channel MOSFET

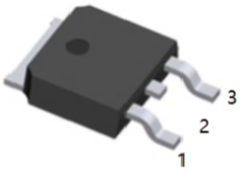
1.Features

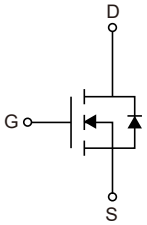
- $V_{DS\ (V)}$=30V
- I_D=30A
- $R_{DS(ON)}$<13.5mΩ(V_{GS}=10V)
- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Avalanche rated
- Very low on-resistance $R_{DS(ON)}$
- Excellent gate charge x $R_{DS(ON)}$ product (FOM)

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK) top view





3.Absolute Maximum Ratings T_J= 25°C

Parameter	Symbol	Conditions	Rating	Units
Continuous drain current	I_D	V_{GS}=10V, T_C=25°C	30	A
		V_{GS}=10V, T_C=100°C	26	A
		V_{GS}=4.5V, T_C=25°C	30	A
		V_{GS}=4.5V, T_C=100°C	21	A
Pulsed drain current [2]	$I_{D,pulse}$	T_C=25°C	210	A
Avalanche energy, single pulse [3]	I_{AS}	T_C=25°C	30	A
Avalanche energy, single pulse	E_{AS}	I_D=10A, R_{GS}=25Ω	20	mJ
Reverse diode dv/dt	dv/dt	I_D=30A, V_{DS}=24V di/dt=200 A/μs, $T_{j,max}$=175°C	6	kV/μs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25°C	31	W
storage temperature	T_J,T_{STG}		-55 to 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

4.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal resistance, junction -case	R_{thJC}				4.9	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint			75	K/W
		6 cm^2 cooling area [4])			50	K/W
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=1mA	30			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.7	2.5	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=30V, V_{GS}=0V, T_J=25°C		0.1	1	μA
		V_{DS}=30V, V_{GS}=0V, T_J=125°C		10	100	μA
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V		10	100	nA
Drain-source on-state resistance [5])	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=20A		10	20.5	mΩ
		V_{GS}=10V, I_D=30A		8	13.5	mΩ
Gate resistance	R_G			1.2		Ω
Transconductance	g_{FS}	$\|V_{DS}\|>2\|I_D\|R_{DS(ON)max}$,$I_D$=30A	22	43		S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz		770	1000	pF
Output capacitance	C_{oss}			350	470	pF
Reverse transfer capacitance	C_{rss}			16		pF
Turn-on delay time	$t_{D(on)}$	V_{DD}=15V, V_{GS}=10V I_D=30A, R_G=1.6Ω		3		ns
Rise time	t_r			3		ns
Turn-off delay time	$t_{D(off)}$			12		ns
Fall time	t_f			2.2		ns
Gate Charge Characteristics [6])						
Gate to source charge	Q_{gs}	V_{DD}=15V, I_D=30A V_{GS}=0 to 4.5V		2.7		nC
Gate charge at threshold	$Q_{g(th)}$			1.2		nC
Gate to drain charge	Q_{gd}			1.2		nC
Switching charge	Q_{SW}			2.6		nC
Gate charge total	Q_g			4.8	6.4	nC
Gate plateau voltage	$V_{plateau}$			3.5		V

Gate charge total	Q_g	V_{DD}=15V, I_D=30A, V_{GS}=0 to 10V		10		nC
Gate charge total, sync.FET	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to 4.5V		4.2	5.5	nC
Output charge	Q_{oss}	V_{DD}=15V, V_{GS}=0V		9		nC
Diode continuous forward current	I_S	T_C=25°C			25	A
Diode pulse current	$I_{S,pulse}$				210	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=30A, T_J=25°C		0.98	1.2	V
Reverse recovery charge	Q_{rr}	V_R=15V, I_F=I_S, di_F/dt=400A/µs			10	nC

Notes:

[1] J-STD20 and JESD22

[2] See figure 3 for more detailed information.

[3] See figure 13 for more detailed information.

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[5] Measured from drain tab to source pin.

[6] See figure 16 for gate charge parameter definition.

5.1Typical characteristic

$P_{tot}=f(T_C)$

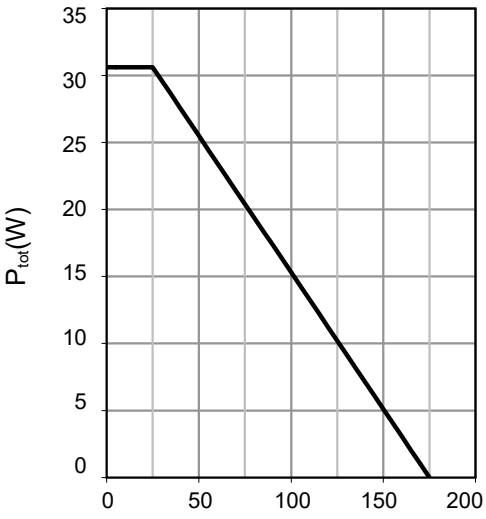


Fig 1. Power dissipation

$I_D=f(T_C)$; $V_{GS}\geq 10V$

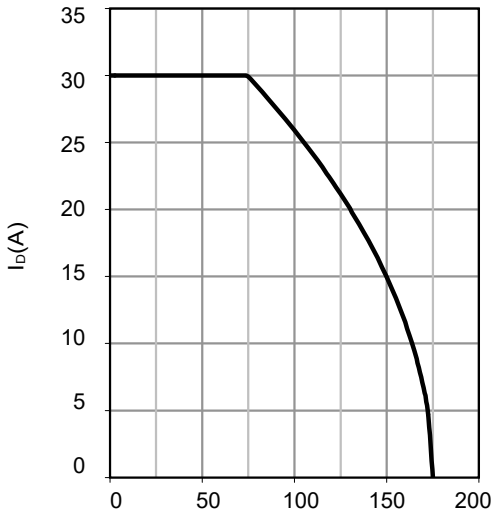


Fig 2. Drain current

ID=f(V_{DS}); T_C=25°C; D=0; parameter: t_p

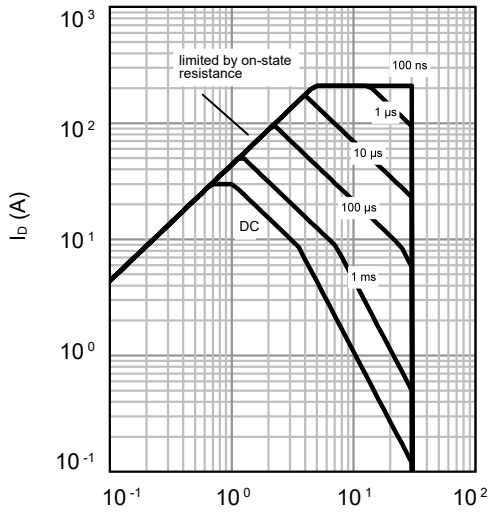


Fig 3. Safe operating area

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

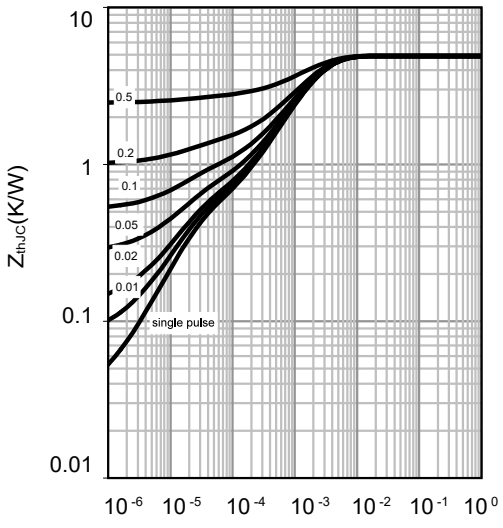


Fig 4. Max transient thermal impedance

5.2Typical characteristic

$I_D=f(V_{DS})$; T_J=25°C; parameter: V_{GS}

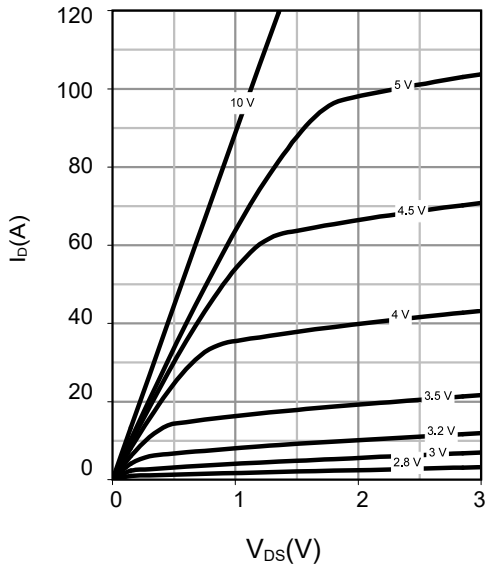


Fig 5. output characteristics

$R_{DS(ON)}=f(I_D)$; T_J=25°C; parameter: V_{GS}

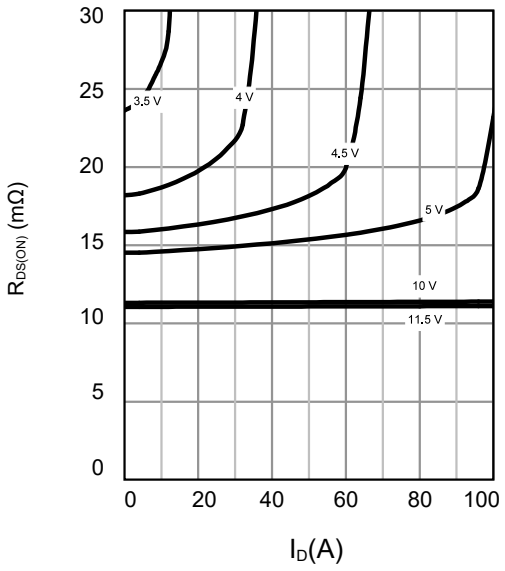


Fig 6. drain-source on resistance

ID=f(V_{GS}); |V_{DS}|>2| I_D |$R_{DS(ON)max}$; parameter: T_J

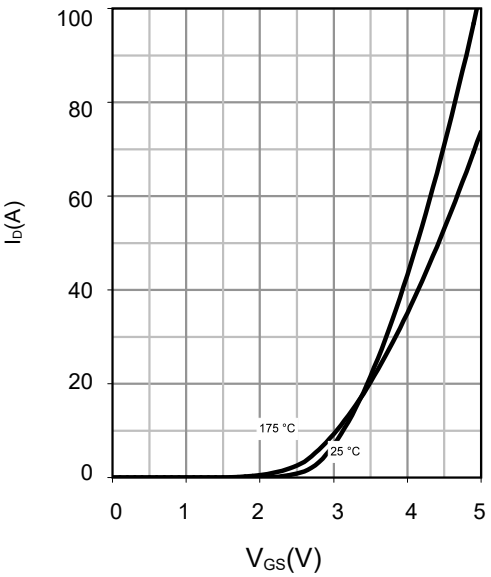


Fig 7. transfer characteristics

$g_{fs}=f(I_D)$; T_J=25°C

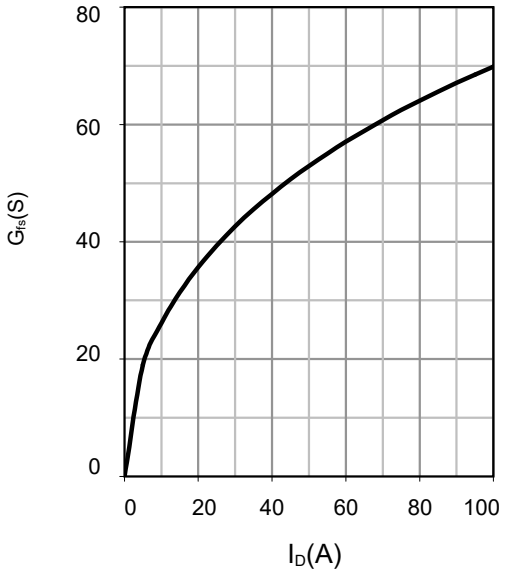


Fig 8. forward transconductance

5.3Typical characteristic

$R_{DS(ON)}=f(T_J)$; I_D=30A; V_{GS}=10V

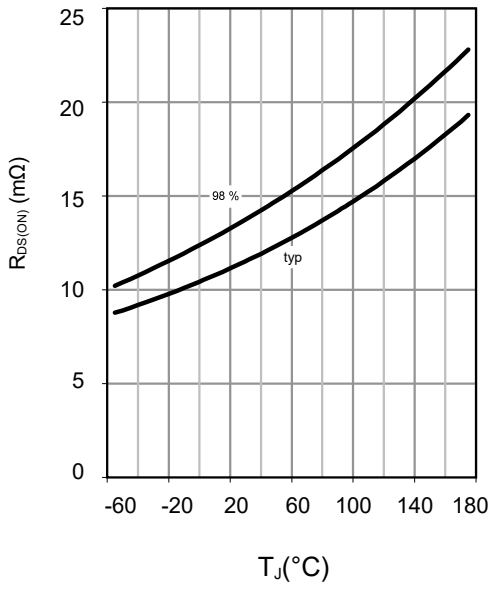


Fig 9. Drain-source on-state resistance

$V_{GS(th)}=f(T_J)$;$V_{GS}=V_{DS}$; I_D=250μA

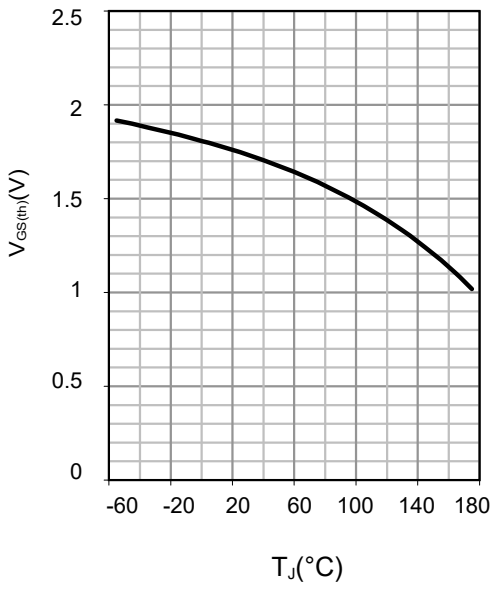


Fig 10. Gate threshold voltage

C=f(V_{DS}); V_{GS}=0V; f=1MHZ

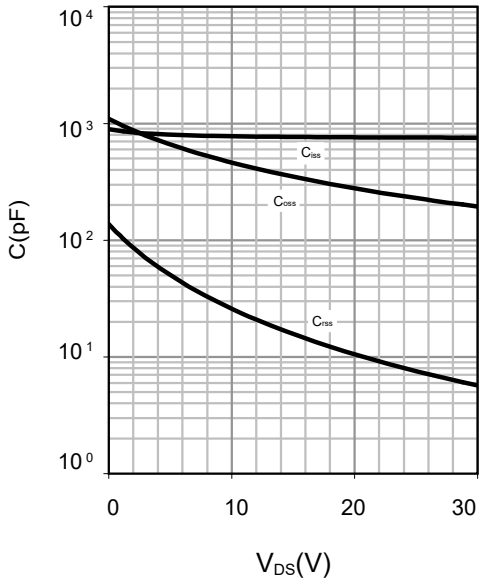


Fig 11. capacitances

I_F=f(V_{SD}); parameter: T_J

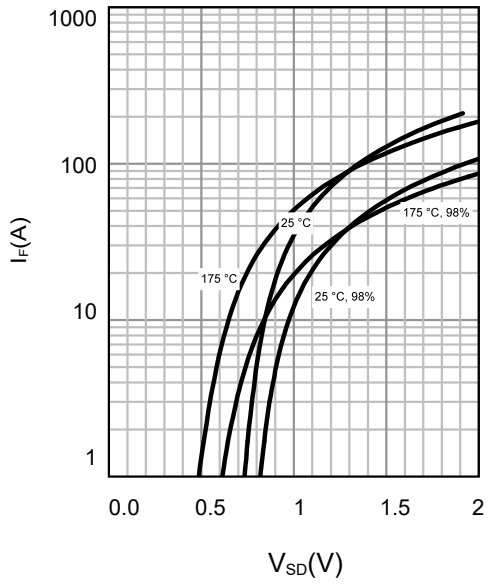


Fig 12. Forward characteristics of reverse diode

5.4Typical characteristic

$I_{AS}=f(t_{AV})$; $R_{GS}=25\Omega$; parameter: $T_{j(start)}$

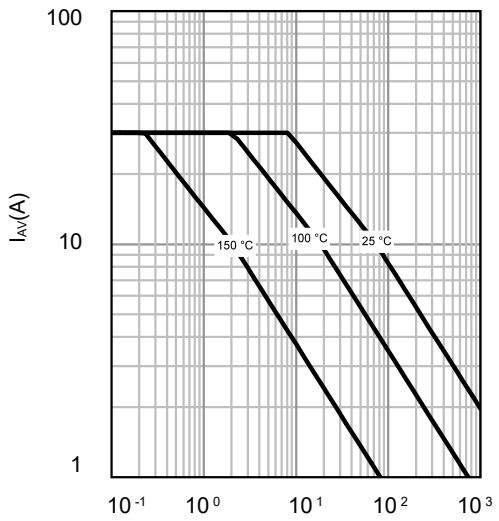


Fig 13. Avalanche characteristics

$V_{GS}=f(Q_{gate})$; $I_D=30A$pulsed; parameter: V_{DD}

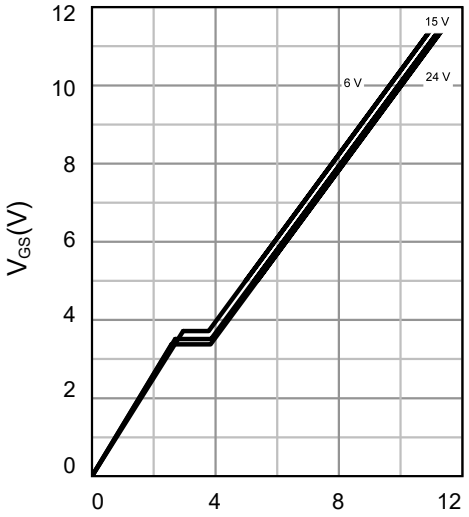


Fig 14. gate charge

$V_{BR(DSS)}=f(T_J)$; $I_D=1m$ A

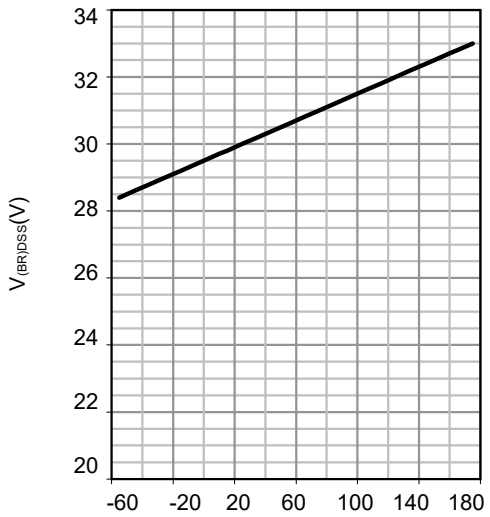


Fig 15. drain source breakdown voltage

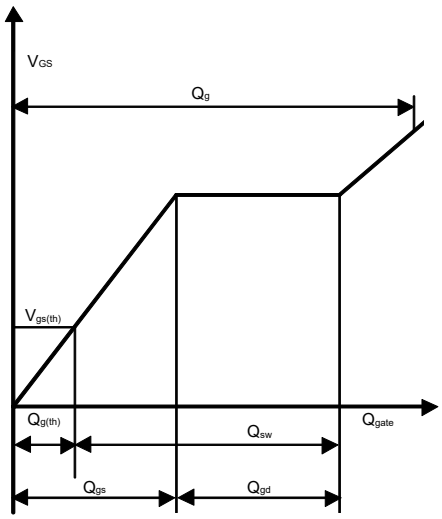
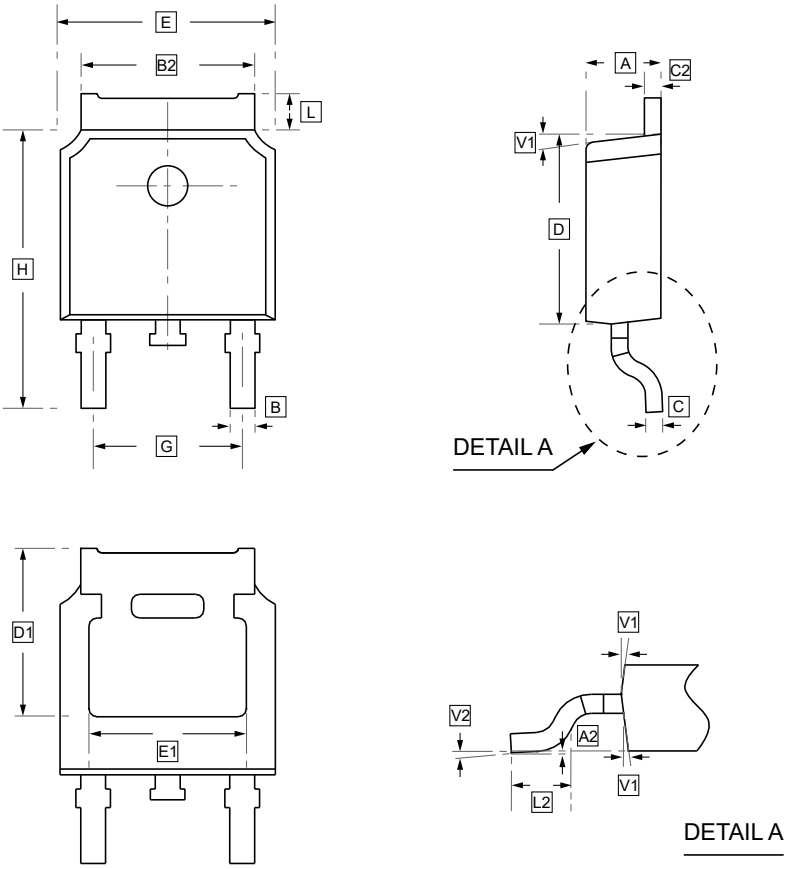


Fig 16. Gate charge waveforms

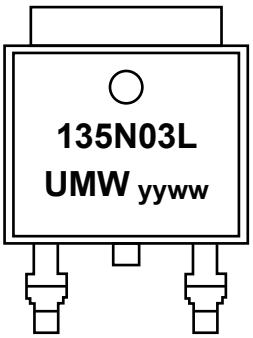
6.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A2	B	B2	C	C2	D	D1	E	E1	G	H	L	L2	V1	V2
Min	2.10	0	0.66	5.18	0.40	0.44	5.90	5.30	6.40	4.63	4.47	9.50	1.09	1.35		0°
Max	2.50	0.10	0.86	5.48	0.60	0.58	6.30	REF	6.80		4.67	10.70	1.21	1.65		6°

7.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IPD135N03LG	TO-252	2500	Tape and reel

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