UMW TSV911/912/914

TSV91x Rail-to-Rail Input/Output, 8MHz Operational Amplifiers

1.Description

The TSV91x family of single, dual, and quad operational amplifiers is designed for general-purpose applications. This family of devices features rail-to-rail input and output (RRIO) swings,wide bandwidth (8MHz), and low offset voltage (0.3mV typical)

The opamps are unity-gain stable and have very low input bias current, making them suitable for applications with high source impedance. The devices also feature low input bias current, making them suitable for sensor interfaces, battery-powered and portable applications, and active filtering .

The TSV91x features a robust design that is easy for circuit designers to use. Features include an integrated RFI-EMI suppression filter that is unity-gain stable, does not exhibit phase reversal under overdrive conditions, and has high electrostatic discharge (ESD) protection (4kV HBM)

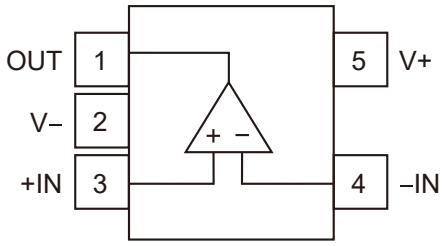
2.Features

- Rail-to-Rail Input and Output
- Low noise: 18nV/√Hz at 1kHz
- Low Power Consumption: 550μA (Typical)
- High gain bandwidth: 8MHz
- Operating Supply Voltage Range: 2.5V to 5.5V
- Low input bias current: 1pA (typ)
- Low input offset voltage: 1.9mV (max)
- Low Offset Voltage Drift: ±0.5μV/°C (Typical)
- ESD in model (HBM)
- Extended temperature range: –40°C to +125°C

3.Applications

- Battery-Powered Applications
- Motor Control
- Power Modules
- HVAC: Heating, ventilation, and air conditioning
- Washing Machines
- Refrigerators
- Medical Instruments
- Active Filters
- Sensor Signal Conditioning
- Audio Receivers
- Automotive Infotainment

4.1 Pinning Information

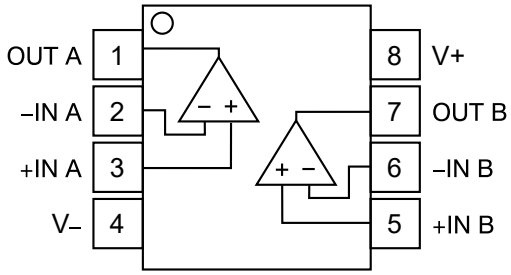


TSV911
PIN SOT-23

Pin Functions

Pin		I/O	Description
Number	Name		
4	-IN	I	Inverting Input
3	+IN	I	Non-Inverting Input
1	OUT	O	Output
2	V-	-	Negative (Lowest) Supply or Ground (For Single Supply Operation)
5	V+	-	Positive (Highest) Supply

4.2 Pinning Information

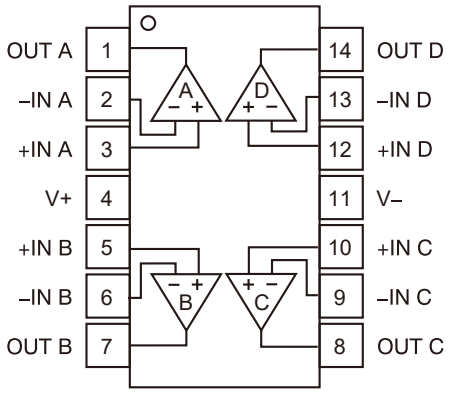


TSV912
PIN SOP-8

Pin Functions

Pin		I/O	Description
Number	Name		
2	-INA	I	Inverting input, channel A
3	+INA	I	Non-inverting input, channel A
6	-INB	I	Inverting input, channel B
5	+INB	I	Non-inverting input, channel B
1	OUTA	O	Output, channel A
7	OUTB	O	Output, channel B
4	V-	-	Negative (Lowest) Supply or Ground (For Single Supply Operation)
8	V+	-	Positive (Highest) Supply

4.3 Pinning Information



TSV914
PIN SOP-14

Pin Functions

Pin		I/O	Description
Number	Name		
2	-INA	I	Inverting Input, Channel A
3	+INA	I	Noninverting Input, Channel A
6	-INB	I	Inverting Input, Channel B
5	+INB	I	Non-Inverting Input, Channel B
9	-INC	I	Inverting Input, Channel C
10	+INC	I	Non-Inverting Input, Channel C
13	-IND	I	Inverting Input, Channel D
12	+IND	I	Non-Inverting Input, Channel D
1	OUTA	O	Output, Channel A
7	OUTB	O	Output, Channel B
8	OUTC	O	Output, Channel C
14	OUTD	O	Output, Channel D
11	V-	-	Negative (lowest) supply or ground (for single supply operation)
4	V+	-	Positive (highest) supply

5.Absolute Maximum Ratings (Measured at Free-Air Temperature)

Parameter			Min	Max	Unit
Supply Voltage				6	V
Signal input pins	Voltage (2)	Common mode		(V+) + 0.5	V
		Differential mode		$\pm V_{CC}$	V
	Current (2)			10	mA
Rated temperature, T_A			-40	125	°C
Junction Temperature, T_J				150	°C
Storage temperature, T_{STG}			-65	150	°C

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These listed values are stress ratings only under extreme conditions and do not imply that the device will operate normally under these conditions and at any other conditions beyond the “Recommended Operating Conditions”. Exposure to absolute maximum ratings for extended periods may affect device reliability.

(2) Input pins are diode clamped to the supply rails. Input signals that can swing 0.5V beyond the rails should be current limited to 10mA or less.

6.Recommended Operating Conditions

Measured Over Free-Air Temperature Range

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_S	2.5	5.5	V
Rated Temperature Range		-40	125	°C

7.1 Thermal Performance Information: TSV912

Thermal Specifications	Symbol	D(SOP) 8 Pin	DGK(VSSOP) 8 Pin	DSG(WSON) 8 Pin	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	157.6	201.2	94.4	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	104.6	85.7	116.5	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	99.7	122.9	61.3	°C/W
Junction-to-top characterization parameter	ψ_{JT}	55.6	21.2	13	°C/W
Junction-to-board characterization parameter	ψ_{JB}	99.2	121.4	61.7	°C/W
Junction-to-case (bottom) thermal resistance	$R_{\theta JC(bot)}$	Not applicable	Not applicable	34.4	°C/W

7.2 Thermal Performance Information: TSV914

Thermal Specifications	Symbol	D(SOP) 14 Pin	PW(TSSOP) 14 Pin	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$	106.9	205.8	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	69	106.7	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	63	133.9	°C/W
Junction-to-top characterization parameter	ψ_{JT}	25.9	34.4	°C/W
Junction-to-board characterization parameter	ψ_{JB}	62.7	132.6	°C/W

8.Electrical Characteristics

V_S (Total Supply Voltage)=(V+)-(V-)=2.5V to 5.5V, T_A=25°C, R_L=10kΩ(connected to V_S, V_{CM}=V_S2, and V_{OUT}=V_S2.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	V_S=5V		±0.3	±1.5	mV
		V_S=5V, T_A=-40°C to +125°C			±3	mV
Drift	dV_{OS}/dT	V_S=5V, T_A=-40°C to +125°C		±0.5		μV/°C
Power Supply Rejection Ratio	PSRR	V_S=2.5V-5.5V, V_{CM}=(V-)		±7		μV/V
Channel Separation, DC		At DC		100		dB
Common-Mode Voltage Range	V_{CM}	V_S=2.5V to 5.5V	(V-)-0.1		(V+)+0.1	V
Common-Mode Rejection Ratio	CMRR	V_S=5.5V, (V-)-0.1V<V_{CM}<(V+)-1.4V T_A=-40°C to +125°C	80	103		dB
		V_S=5.5V, V_{CM}=-0.1V to 5.6V T_A=-40°C to +125°C	57	87		dB
		V_S=2.5V, (V-)-0.1V<V_{CM}<(V+)-1.4V T_A=-40°C to +125°C		88		dB
		V_S=2.5V, V_{CM}=-0.1V to 1.9V T_A=-40°C to +125°C		81		dB
Input Bias Current	I_B			±1		pA
Input Offset Current	I_{OS}			±0.05		pA
Input Voltage Noise (Peak-to-Peak)	E_n	V_S=5V, f=0.1Hz to 10Hz		4.77		$μV_{PP}$
Input Voltage Noise Density	e_n	V_S=5V, f=10kHz		12		nV/√Hz
		V_S=5V, f=1kHz		18		nV/√Hz
Input Current Noise Density	i_n	f=1kHz		10		fA/√Hz
Differential	C_{ID}			2		pF
Common Mode	C_{IC}			4		pF

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Open-Loop Voltage Gain	A_{OL}	V_S=2.5V, (V-)+0.04V<V_O<(V+)-0.04V R_L=10kΩ		100		dB
		V_S=5.5V, (V-)+0.05V<V_O<(V+)-0.05V R_L=10kΩ		130		dB
		V_S=2.5V, (V-)+0.06V<V_O<(V+)-0.06V R_L=2kΩ	104	100		dB
		V_S=5.5V, (V-)+0.15V<V_O<(V+)-0.15V R_L=2kΩ		130		dB
Gain Bandwidth Product	GBP	V_S=5V, G=1		8		MHz
Phase Margin	φ_m	V_S=5V, G=1		55		Degrees
Slew Rate	SR	V_S=5V, G=1, R_L=2kΩ, C_L=100pF		4.5		V/μs
Settling Time	t_s	Accuracy to 0.1%, V_S=5V, 2V step G=1, C_L=100pF		0.5		μs
		Accuracy to 0.01%, V_S=5V, 2V step G=1, C_L=100pF		1		μs
Overload Recovery Time	t_{OR}	V_S=5V, V_{IN} × GAIN>V_S		0.2		μs
Total Harmonic Distortion+Noise (1)	THD+N	V_S=5V, V_O=1V_{RMS}, G=1, f=1kHz		0.0008		%
Voltage output swing relative to the supply rail	V_O	V_S=5.5V, R_L=10kΩ			15	mV
		V_S=5.5V, R_L=2kΩ			50	mV
Short Circuit Current	I_{SC}	V_S=5V		±50		mA
Open Loop Output Impedance	Z_O	V_S=5V, f=10MHz		100		Ω
Quiescent Current per Amplifier	I_Q	V_S=5.5V, I_O=0mA		550	750	μA
		V_S=5.5V, I_O=0mA T_A=-40°C to +125°C			1100	μA

(1) Third order filter; bandwidth at –3dB = 80kHz

9.1 Typical Characteristic

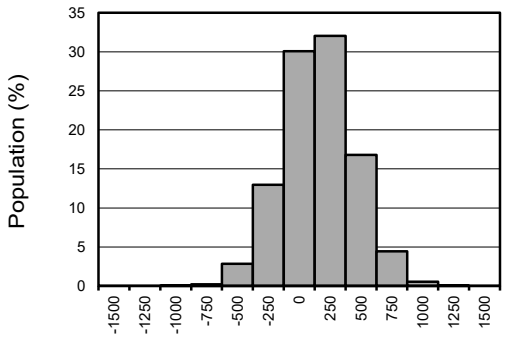


Figure 1: Offset Voltage Generation Distribution

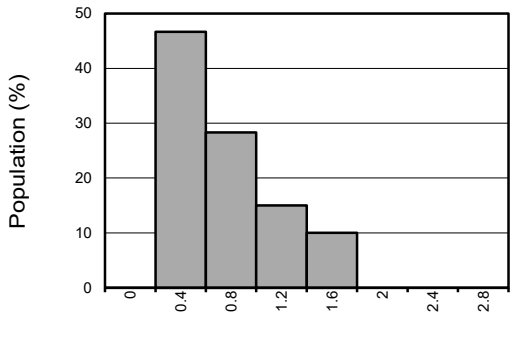


Figure 2: Offset Voltage Drift Distribution

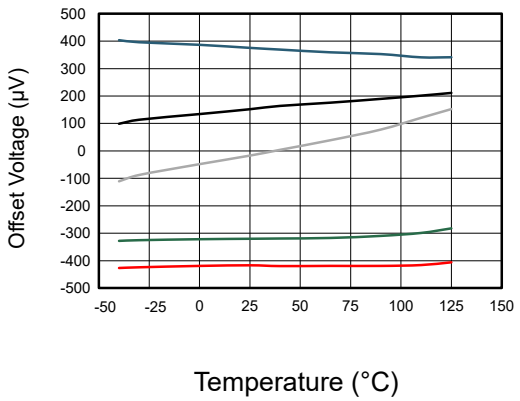


Figure 3: Offset Voltage vs. Temperature

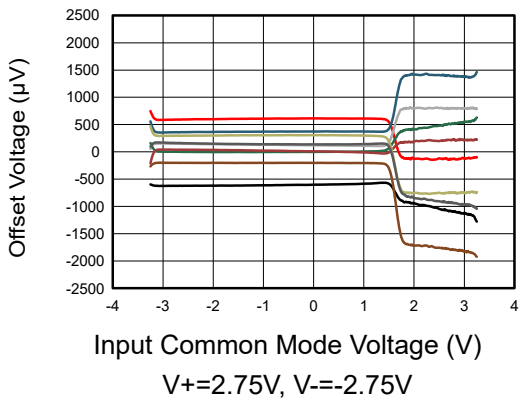


Figure 4: Offset Voltage vs. Common Mode Voltage

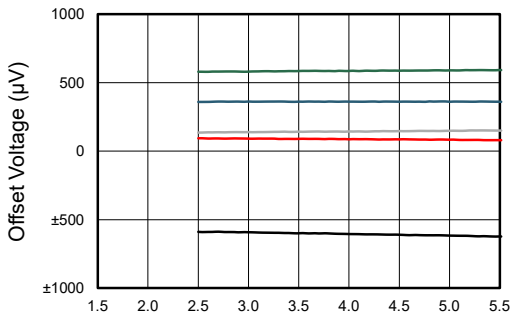


Figure 5: Offset Voltage vs. Power Supply

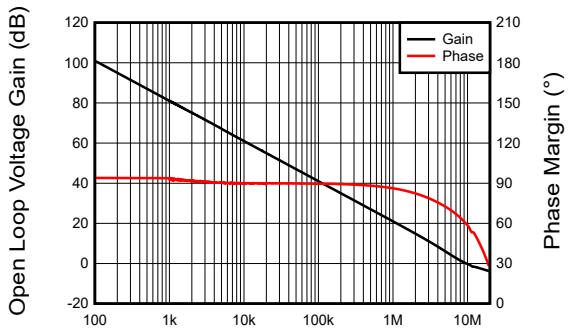


Figure 6: Open-Loop Gain and Phase vs. Frequency

9.2 Typical Characteristic

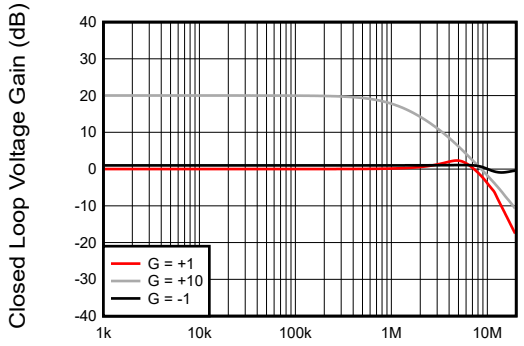


Figure 7: Closed-Loop Gain vs. Frequency

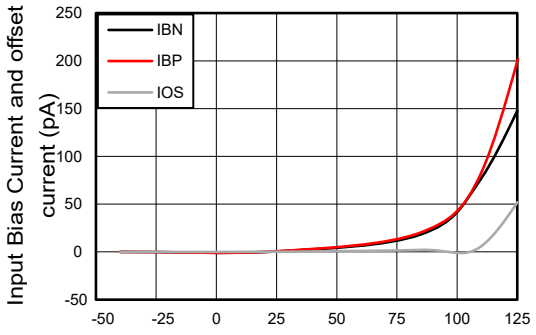


Figure 8: Input Bias Current vs. Temperature

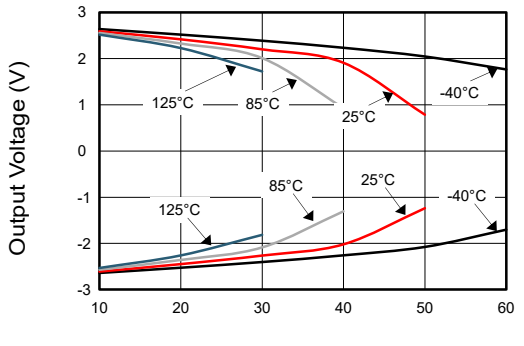


Figure 9: Output Voltage Swing vs. Output Current

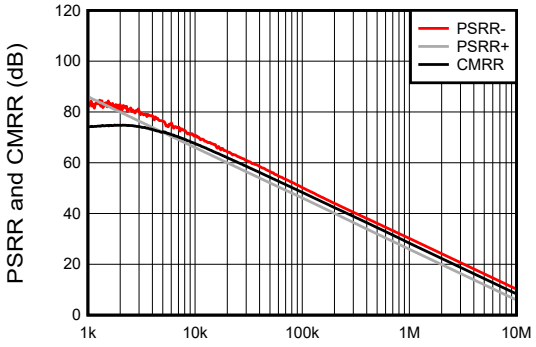


Figure 10: cmrr and psrr vs. frequency (Referred to Input)

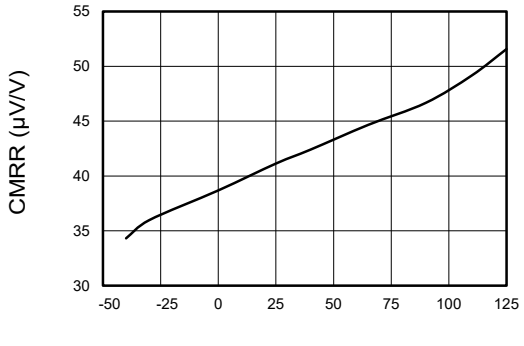


Figure 11: cmrr vs. temperature

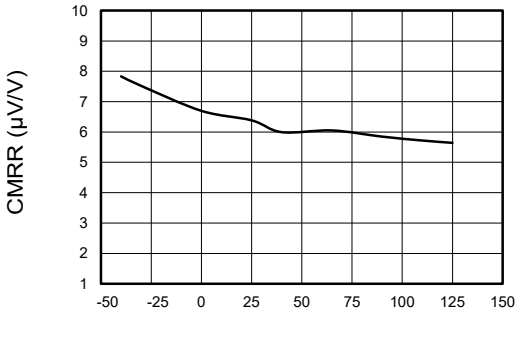
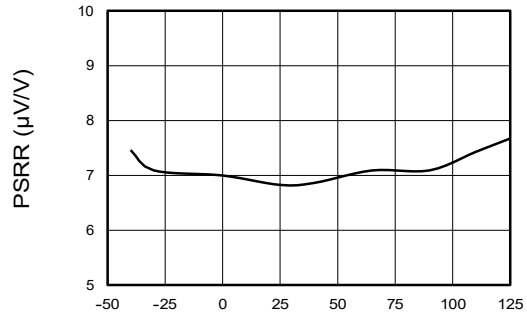


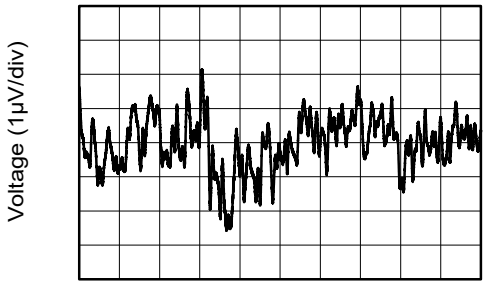
Figure 12: cmrr vs. temperature

9.3 Typical Characteristic



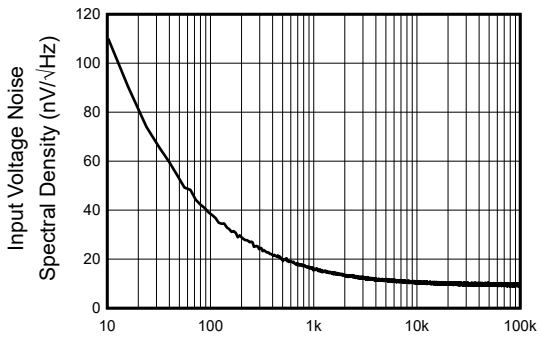
Temperature (°C), V_S=2.5V to 5.5V

Figure 13: psrr vs. temperature



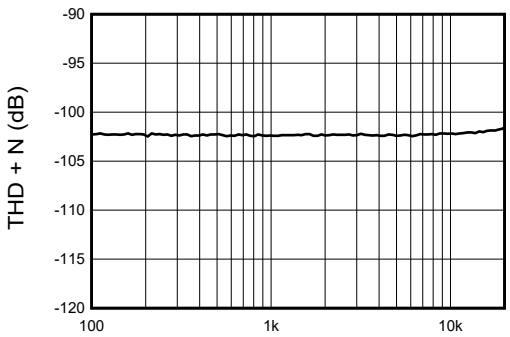
Time (1s/div), V_S=2.5V to 5.5V

Figure 14: 0.1Hz to 10Hz input voltage noise



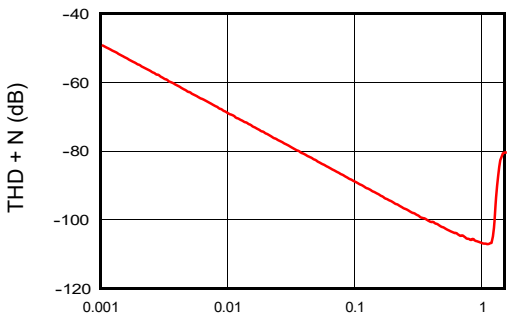
Frequency (Hz)

Figure 15: Input Voltage Noise Spectral Density Vs. Frequency



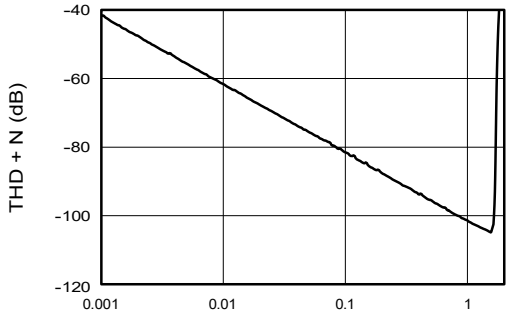
Frequency (Hz)

Figure 16: thd + n vs. frequency



Output Voltage Amplitude (V_{RMS})

Figure 17: thd + n vs. amplitude



Output Voltage Amplitude (V_{RMS})

Figure 18: thd + n vs. amplitude

9.4 Typical Characteristic

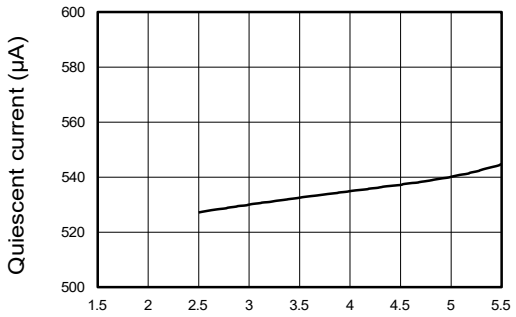


Figure 19: Quiescent Current vs Supply Voltage

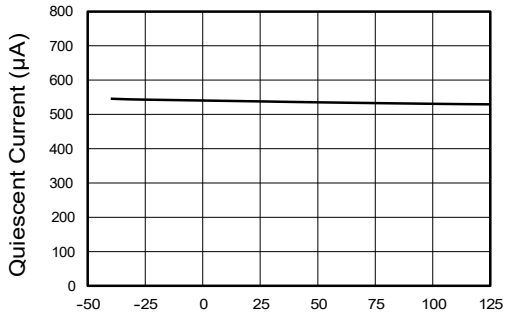


Figure 20: Quiescent Current vs Temperature

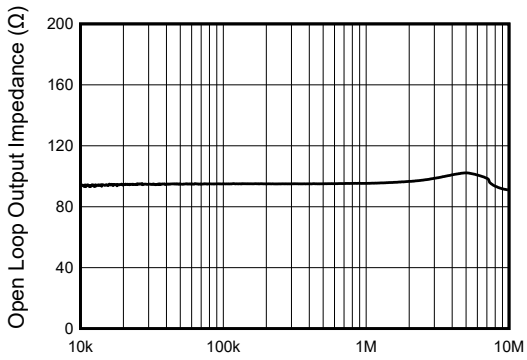


Figure 21: Open-Loop Output Impedance vs Frequency

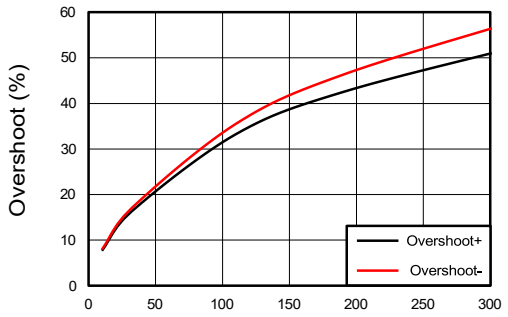


Figure 22: Small Signal Overshoot vs Load Capacitance

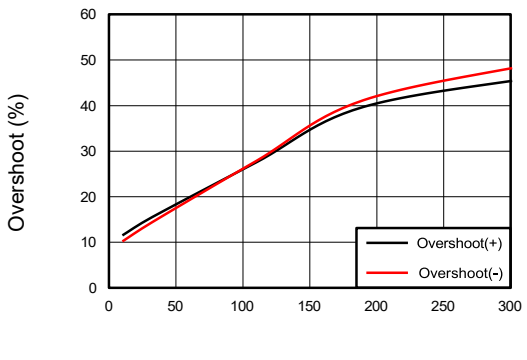


Figure 23: Small Signal Overshoot vs Load Capacitance

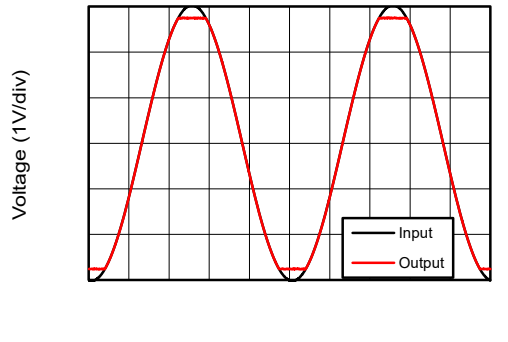
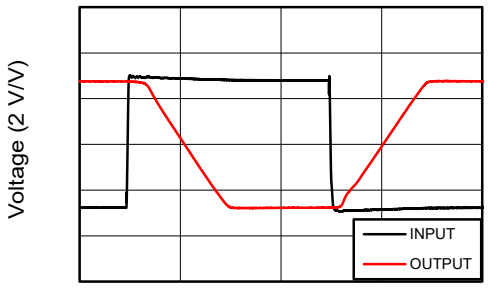


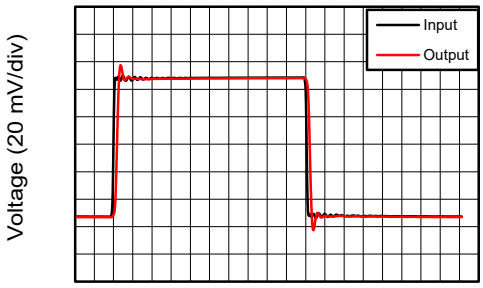
Figure 24: No Phase Reversal

9.5 Typical Characteristic



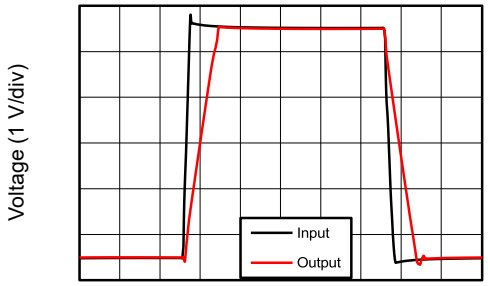
Time (1μs/div)
V+=2.75V, V-=-2.75V, G =-10V/V

Figure 25: Quiescent Current vs Supply Voltage



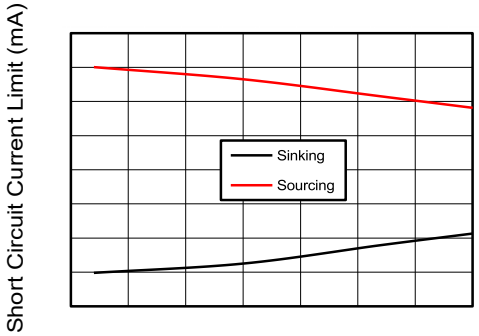
Time (0.1μs/div)
V+=2.75V, V– = –2.75V, G = 1V/V

Figure 26: Small Signal Step Response



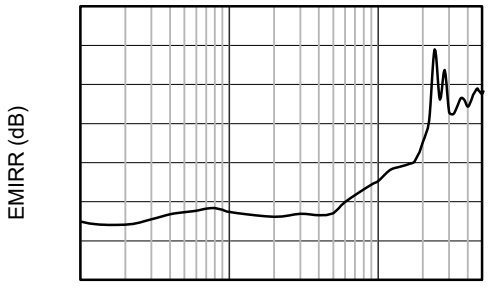
Time (1μs/div)
V+=2.75V, V-=-2.75V, C_L=100pF, G=1V/V

Figure 27: Large Signal Step Response



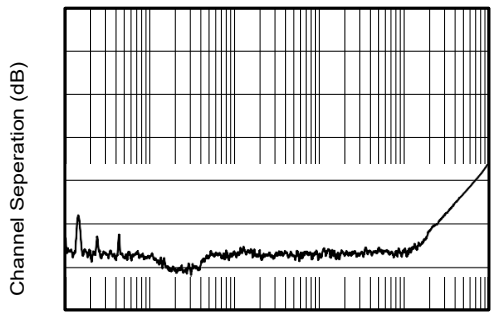
Temperature (°C)

Figure 28: Short Circuit Current vs Temperature



Frequency (Hz), P_{RF}=-10dBm

Figure 29: Electromagnetic Interference Rejection Ratio (emirr+) Referenced to the Non-Inverting Input Vs Frequency



Frequency (Hz), V+=2.75V, V-=-2.75V

Figure 30: Channel Separation vs Frequency

9.6 Typical Characteristic

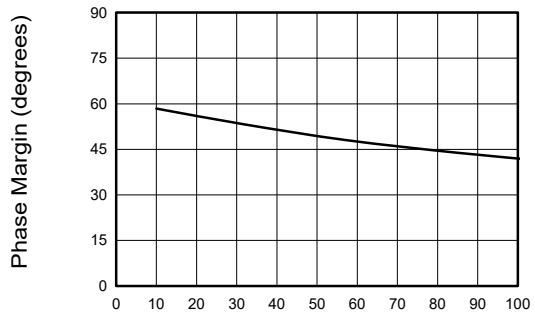


Figure 31: Phase Margin vs Capacitive Load

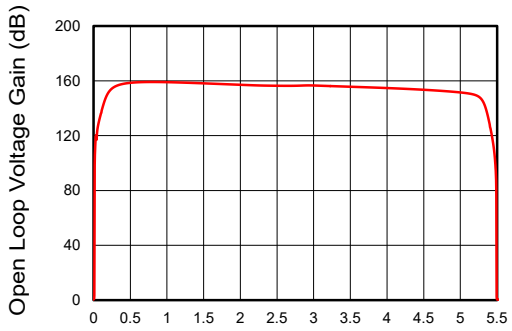


Figure 32: Open-Loop Voltage Gain Vs Output Voltage

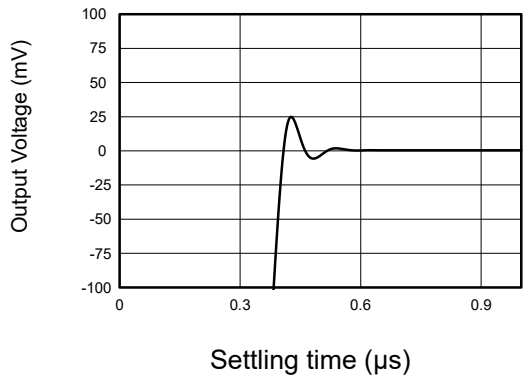


Figure 33: Large Signal Settling Time (Positive)

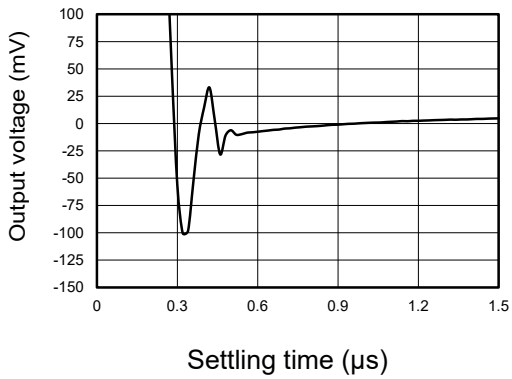
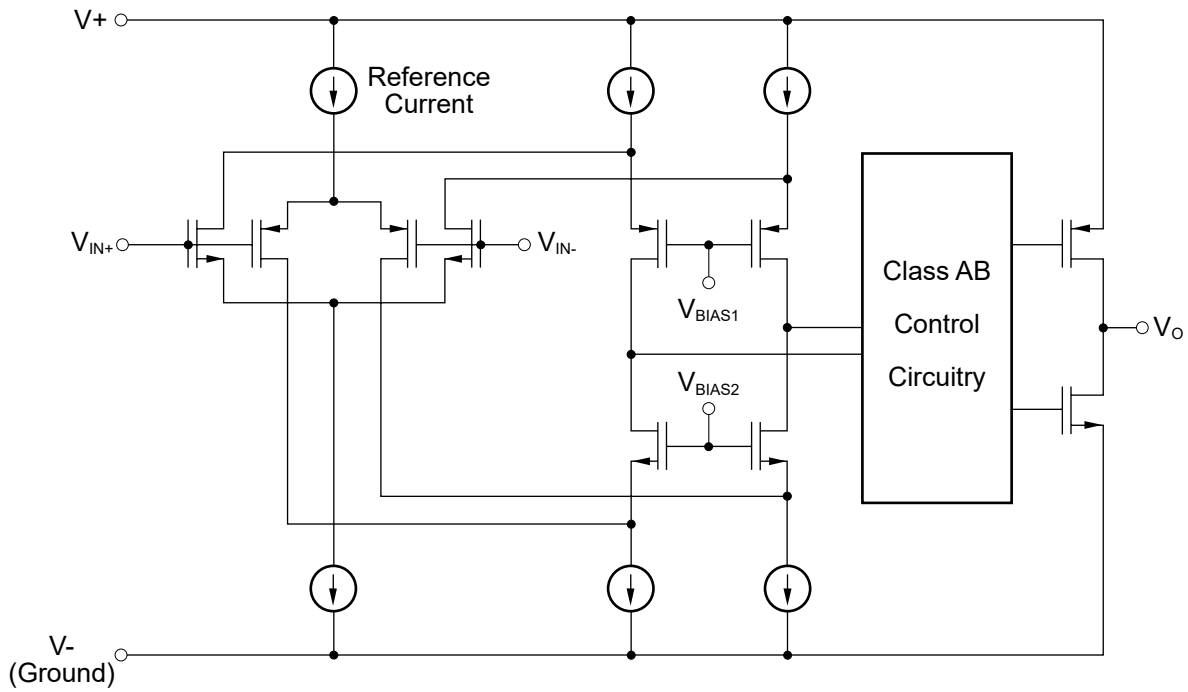


Figure 34: Large Signal Settling Time (Negative)

10.Functional Block Diagram



Rail-to-Rail Input

The TSV91x family's input common-mode voltage range extends 100mV out from the supply rails, supporting a full supply voltage range of 2.5V to 5.5V. This performance is achieved by a complementary input stage: an N-channel input differential pair and a P-channel differential pair in parallel, as shown in the functional block diagram. The N-channel pair is active when the input voltage is close to the positive rail (typically between (V+) – 1.4V and 100mV above the positive supply voltage), while the P-channel pair is active when the input is between 100mV below the negative supply voltage and approximately (V+) – 1.4V. Both channel pairs are typically turned on in a small switching region between (V+) – 1.2V and (V+) – 1V. This 200mV transition region may vary by up to 200mV from process to process. Therefore, this transition region (both stages are on) ranges from (V+) – 1.4V to (V+) – 1.2V on the low side and up to (V+) – 1V to (V+) – 0.8V on the high side. In this transition region, performance such as PSRR, CMRR, offset voltage, temperature drift, and THD may be degraded compared to when the device is operated outside this region.

Rail-to-Rail Output

The TSV91x family of devices is a low-power, low-voltage operational amplifier that provides strong output drive capability. A class AB output stage with common-source transistors enables full rail-to-rail output swing capability. For a 10kΩ resistive load, the output swing is within 15mV of both rails regardless of the applied supply voltage. Different load conditions change the amplifier's ability to swing close to the supply rails.

Overload Recovery

Overload recovery is defined as the time required for the output of an operational amplifier to recover from saturation to linearity. The output device of an operational amplifier enters the saturation region when the output voltage exceeds the rated operating voltage due to high input voltage or high gain. After the device enters the saturation region, the charge carriers in the output device take time to return to the linear state. When the charge carriers return to the linear state, the device starts switching at the specified slew rate. Therefore, the propagation delay (in an overload condition) is equal to the sum of the overload recovery time and the transition time. The overload recovery time of the TSV91x family of devices is approximately 200ns.

Device Functional Modes

The TSV91x family has a single-function mode. The devices are powered as long as the supply voltage is between 2.5V (±1.25V) and 5.5V (±2.75V).

Application Information

The TSV91x family achieves 8MHz bandwidth and 4.5V/μs slew rate with only 550μA supply current per channel, providing good AC performance at low power consumption. It also has good performance in DC applications, with low input noise voltage (18nV/√Hz at 1kHz), low input bias current, and a typical input offset voltage of 0.3mV.

11.Typical Application

Figure 35 shows the TSV91x configured in a low-side motor control application.

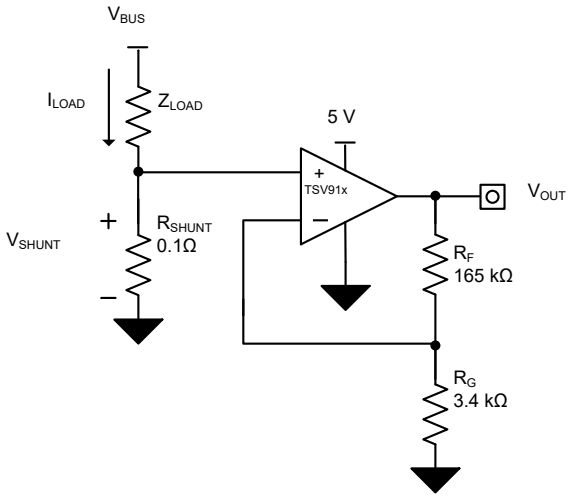


Figure 35. TSV91x in a low-side motor control application

The design requirements for this design are as follows:

• Load current: 0A to 1A

• Output voltage: 4.95V

• Maximum shunt voltage: 100mV

12.Application Curves

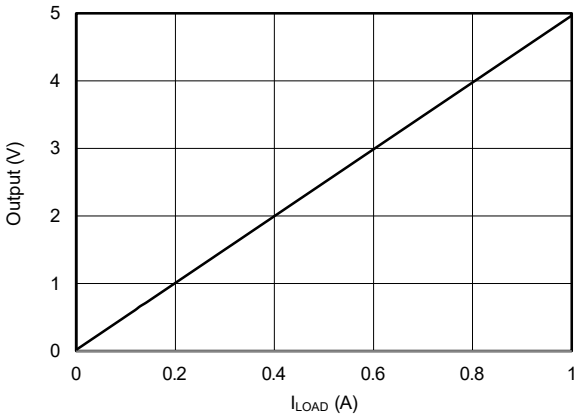
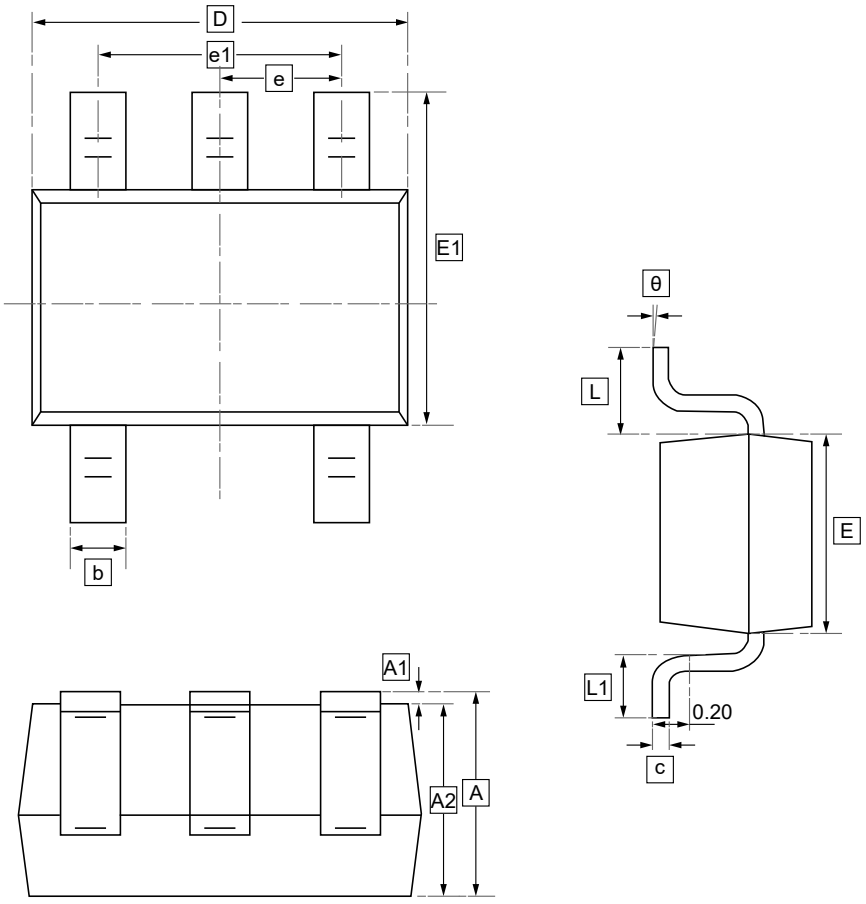


Figure 36. Low-Side Current Sense Transfer Function

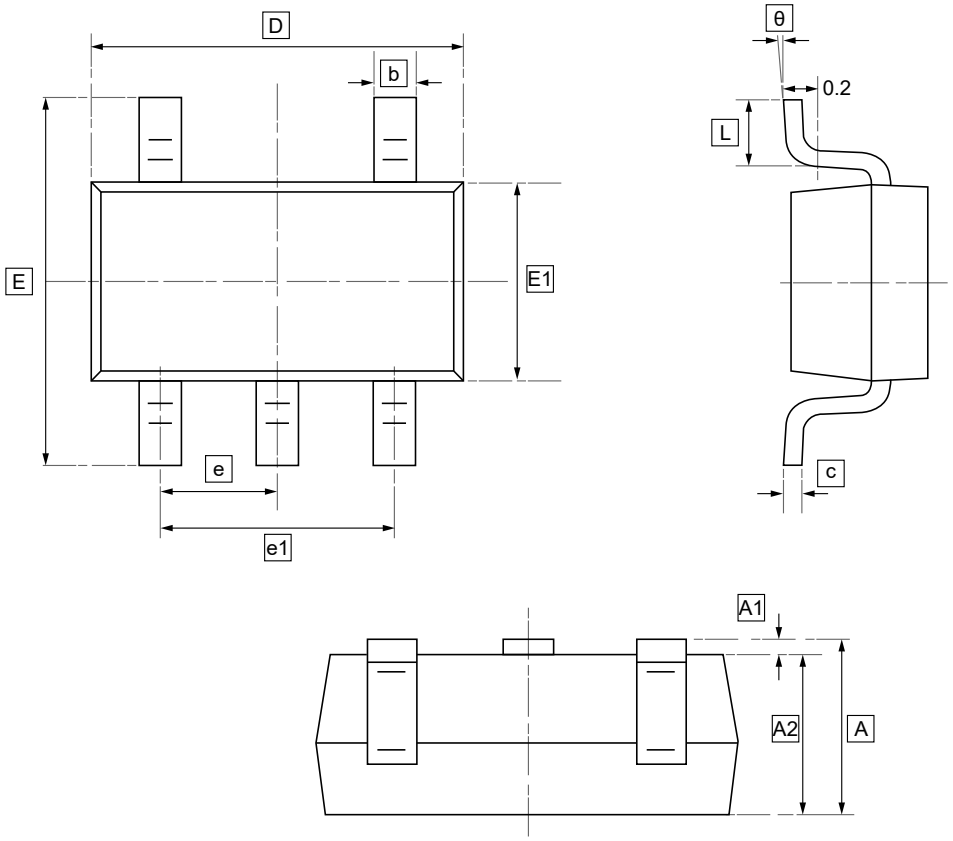
13.1 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	2.05	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

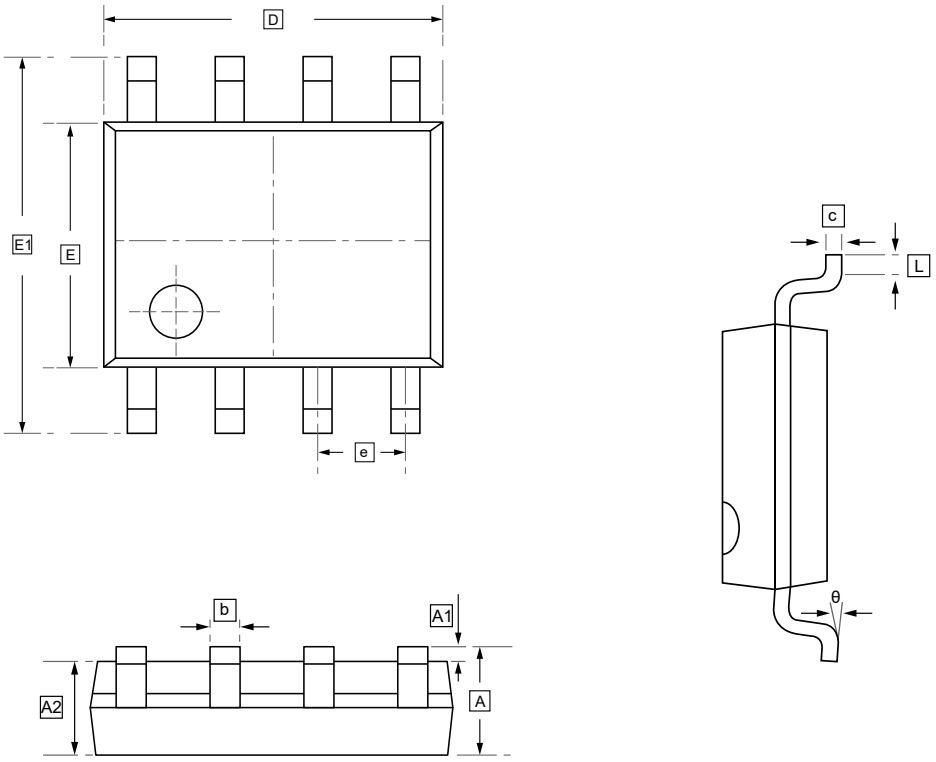
13.2 SOT-23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

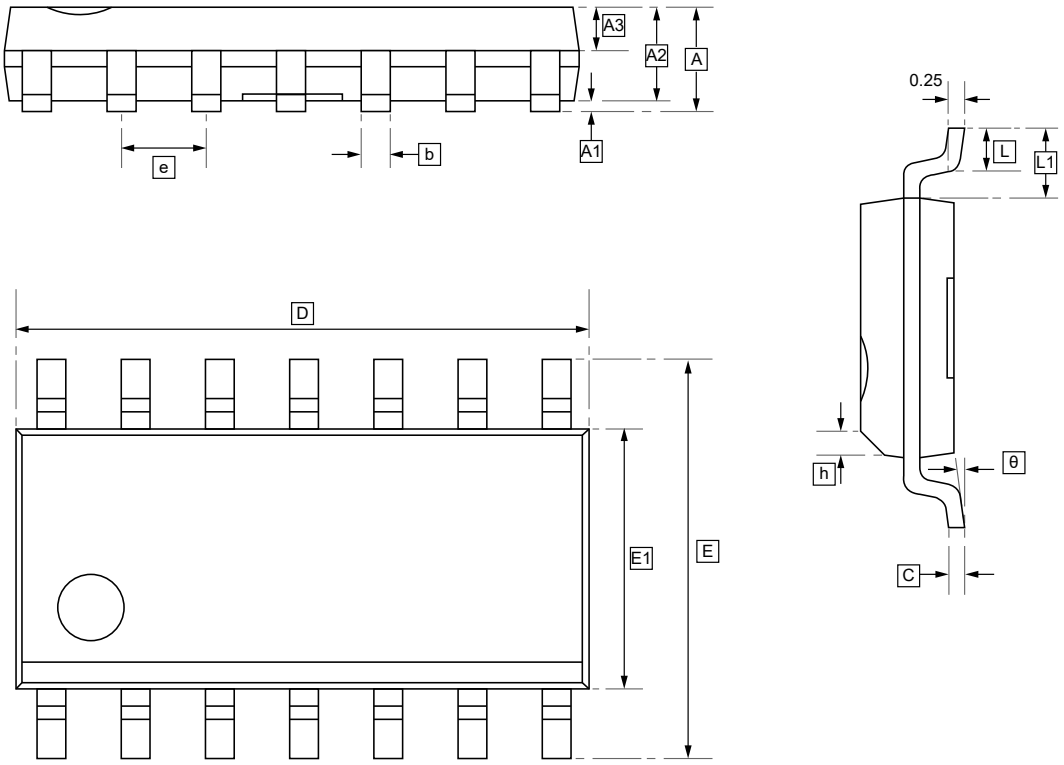
13.3 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

13.4 SOP-14 Package Outline Dimensions

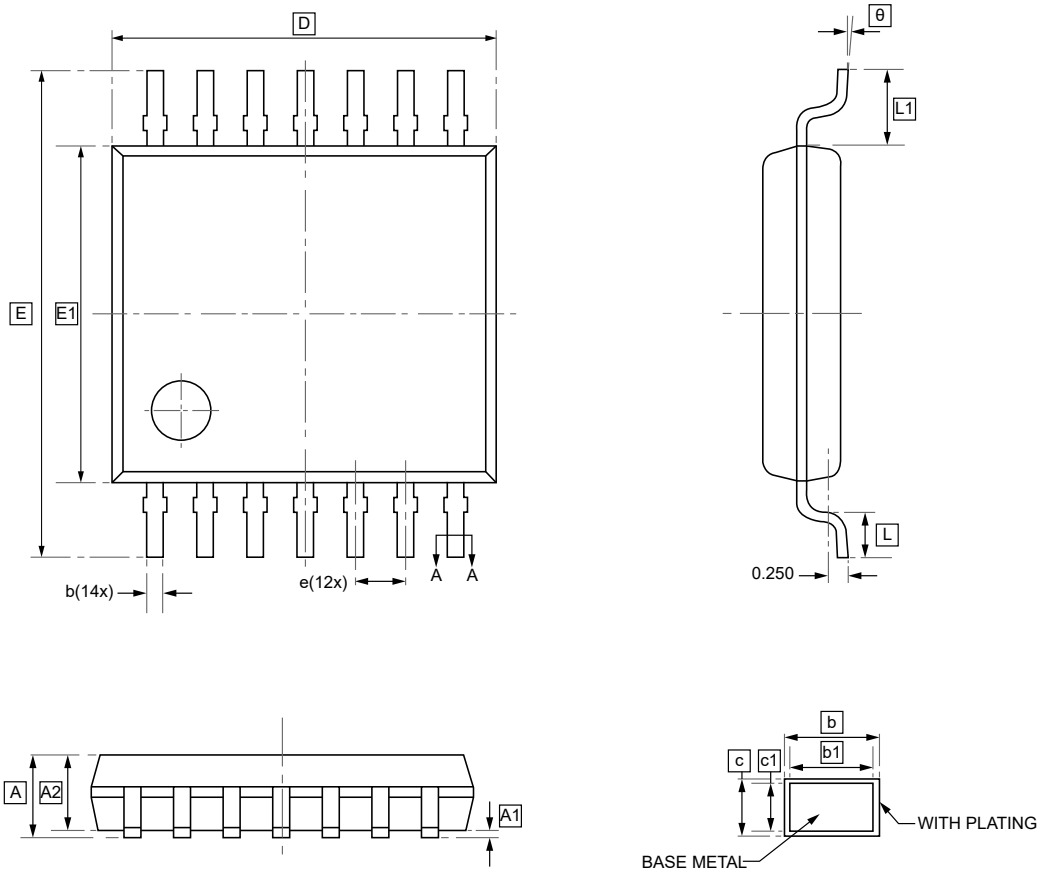


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	C	D	E	E1	e	h	L
Min	-	0.05	1.35	0.65	0.203	0.17	8.45	5.80	3.80	1.24	0.25	0.40
Max	1.75	0.25	1.55	0.75	0.305	0.25	8.85	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

13.5 TSSOP-14 Package Outline Dimensions

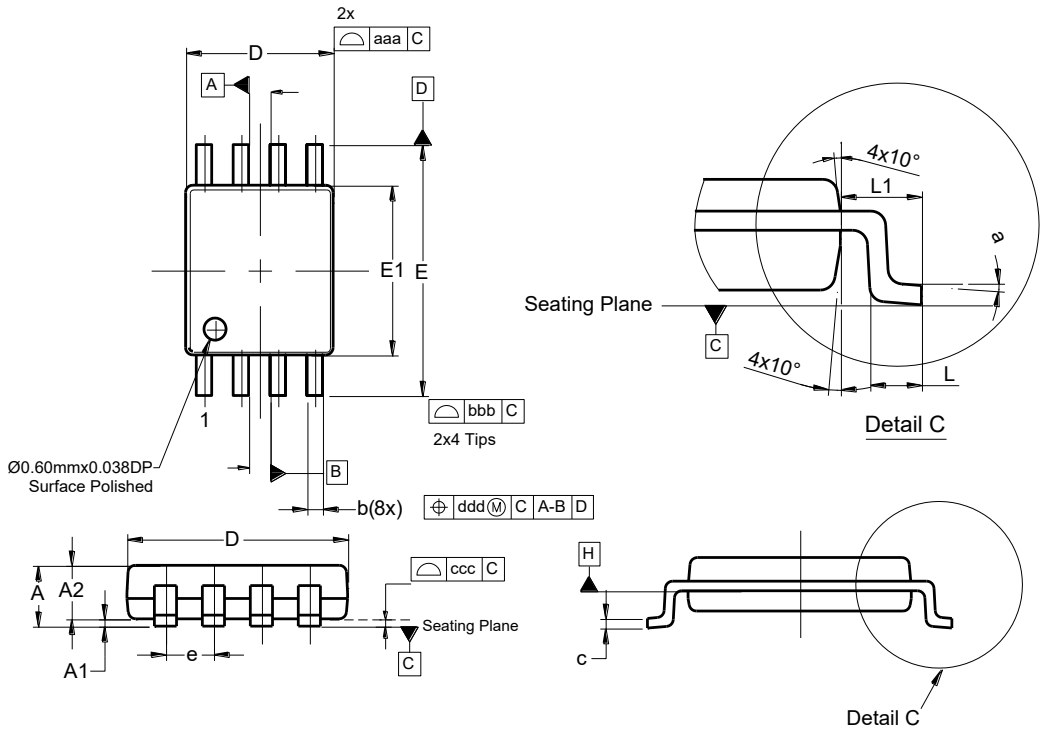


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	c1	D	E	E1	e	L1
Min	-	0.05	0.90	0.20	0.19	0.13	0.120	4.90	6.20	4.30	0.65	0.85
Max	1.20	0.15	1.05	0.28	0.25	0.17	0.14	5.10	6.60	4.50	BSC	1.15

Symbol	L	θ
Min	0.45	0°
Max	0.75	8°

13.6 VSSOP-8 Package Outline Dimensions

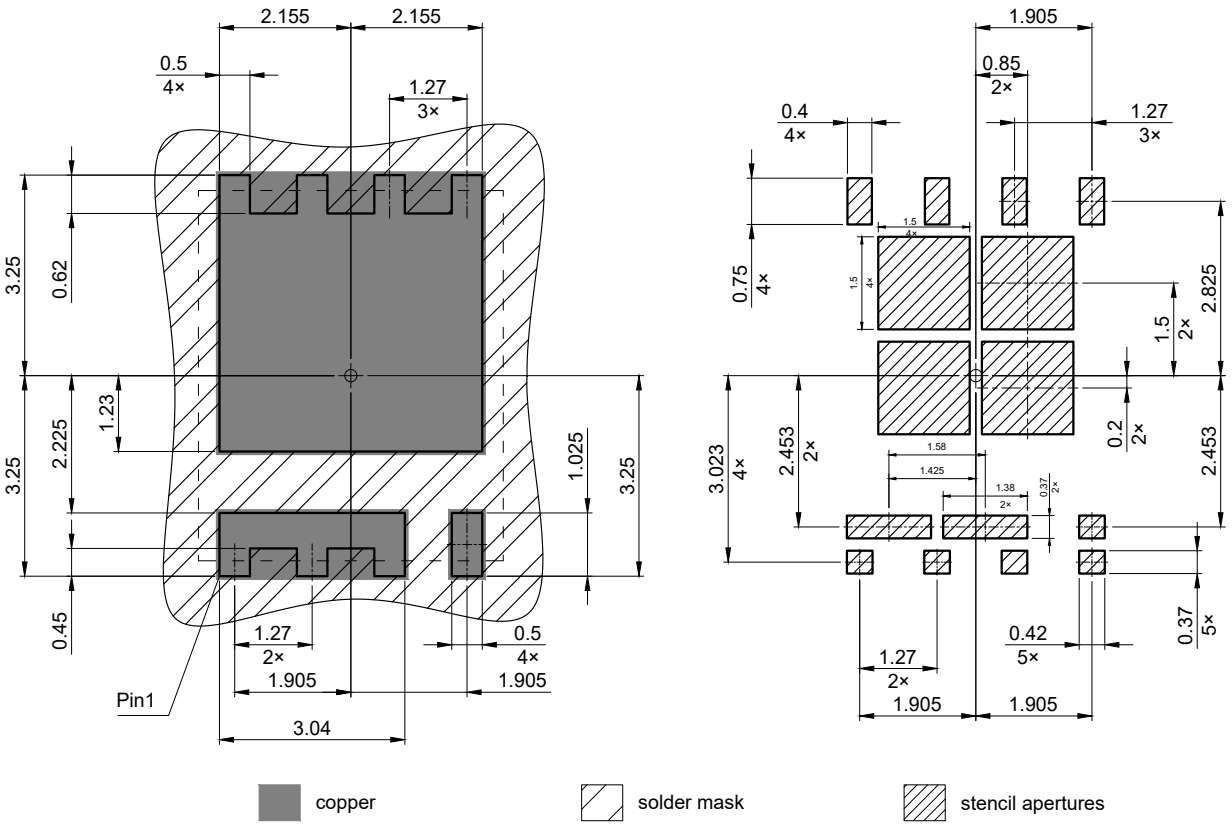


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	L1	a
Min	0.60	-	0.60	0.17	0.08	1.90	3.20	2.20	-	0.30	0.50	0°
Max	0.90	0.10	0.80	0.25	0.13	2.10	3.60	2.40	-	0.40	0.60	6°

Symbol	aaa	bbb	ccc	ddd
Min	0.20	0.25	0.10	0.13
Max				

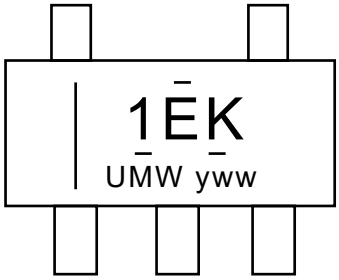
13.7 WSON-8 Package Outline Dimensions



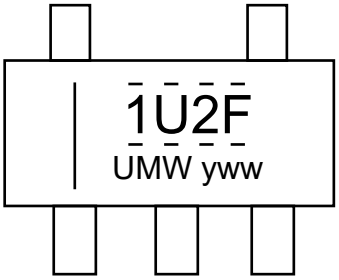
All dimensions are in units mm

14.Ordering Information

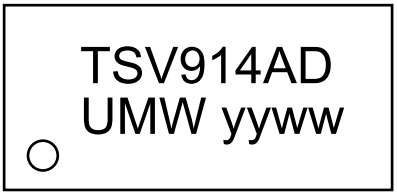
SC-70-5



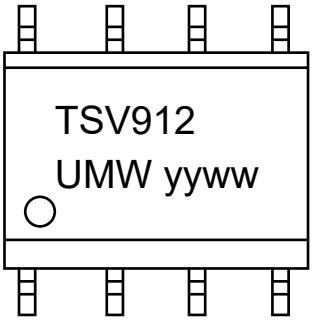
SC-70-5



SOP-14



SOP-8



y: Year Code
yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW TSV911AIDBVR	1U2F	SOT-23-5	3000	Tape and reel
UMW TSV911AIDCKR	1EK	SC-70-5	3000	Tape and reel
UMW TSV912AIDR	TSV912	SOP-8	2500	Tape and reel
UMW TSV912AIDGKR	TSV912	VSSOP-8	2500	Tape and reel
UMW TSV912AIDSGR	TSV912	WSON-8	2500	Tape and reel
UMW TSV914AIPWR	TSV914	TSSOP-14	2500	Tape and reel
UMW TSV914AIDR	TSV914AD	SOP-14	2500	Tape and reel

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