UMW 6N135,6N136

Single Channel，High Speed 1MBit/s Transistor Optocouplers

1.Description

The UMW 6N135/6N136 optocoupler consists of an 850nm AlGaAs LED optically coupled to a high speed photodetector transistor. A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor. The devices are packaged in an 8-pin DIP package and available in wide-lead spacing (M-type) and SMD option.

2.Features

- Open-Collector Output
- TTL Compatible
- High bit rate: 1 MBit/s
- Superior CMR-10 kV/μs
- CTR guaranteed: 0-70°C
- RoHS compliant

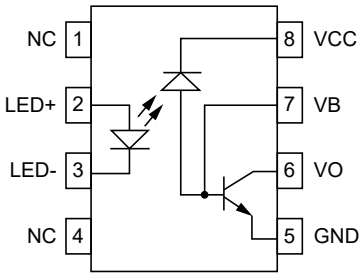
3.Applications

- Output interface to CMOS-LSTTL-TTL
- Telecommunication equipment
- Power transistor isolation in motor drives
- Replacement for low speed phototransistor photo couplers
- Home applian WXW

4.Pinning information

Truth Table (Positive Logic)

LED	V_O
ON	LOW
OFF	HIGH



DIP-8/SOP-8

5.Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Units
Storage temperature	T_{STG}	-55 to +125	°C
Operating temperature	T_{OPR}	-55 to +100	°C
Lead solder temperature	T_{SOL}	260 for 10 sec	°C
Emitter			
DC/Average forward input current (Note 1)	$I_{F(avg)}$	25	mA
Peak forward input current (50% duty cycle, 1 ms p.w.) (Note 2)	$I_{F(pk)}$	50	mA
Peak transient input current (≤1μs p.w., 300 pps)	$I_{F(trans)}$	1	A
Reverse input voltage	V_R	5	V
Input power dissipation (Note 3)	$P_{D(i)}$	100	mW
Detector			
Average output current	$I_{O(avg)}$	8	mA
Peak output current	$I_{O(pk)}$	16	mA
Emitter-base reverse voltage	V_{EBR}	5	V
Supply voltage	V_{CC}	-0.5 to 30	V
Output voltage	V_O	-0.5 to 20	V
Base current	I_B	5	mA
Output power dissipation (Note 4)	$PD_{(o)}$	100	mW

Notes:

1. Derate linearly above 70°Cfree -air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°Cfree -air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°Cfree -air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°Cfree -air temperature at a rate of 2.0mW/°C.

6.Electrical characteristics

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Emitter							
Input forward voltage		V_F	I_F=16mA, T_A=25°C		1.45	1.7	V
			I_F=16mA			1.8	V
Input reverse breakdown voltage		BV_R	I_R=10μA	5			V
Temperature coefficient of forward voltage		$(\Delta V_F/\Delta T_A)$	I_F=16mA		-1.6		mV/°C
Detector							
Logic high output current		I_{OH}	I_F=0mA, V_O=V_{CC}=5.5V T_A=25°C		0.001	0.5	μA
			I_F=0mA, V_O=V_{CC}=15V T_A=25°C		0.005	1	
			I_F=0mA, V_O=V_{CC}=15V			50	
Logic low supply current		I_{CCL}	I_F=16mA, V_O=Open V_{CC}=15V		120	200	μA
Logic high supply current		I_{CCH}	I_F=0mA, V_O=Open V_{CC}=15V, T_A=25°C			1	μA
			I_F=0mA, V_O=Open V_{CC}=15V			2	μA
Coupled							
Current transfer ratio (Note 1)	6N135	C_{TR}	I_F=16mA, V_{CC}=4.5V V_O=0.4V, T_A=25°C	7	18	50	%
			I_F=16mA, V_{CC}=4.5V V_O=0.5V	5	19		
	6N136		I_F=16mA, V_{CC}=4.5V V_O=0.4V, T_A=25°C	19	24	50	
			I_F=16mA, V_{CC}=4.5V V_O=0.5V	15	25		

Logic low output voltage output voltage	6N135	V_{OL}	I_F=16mA, V_{CC}=4.5V I_O=1.1mA, T_A=25°C		0.18	0.4	V
			I_F=16mA, V_{CC}=4.5V I_O=0.8mA			0.5	
	6N136		I_F=16mA, V_{CC}=4.5V I_O=3mA, T_A=25°C		0.1	0.4	
			I_F=16mA, V_{CC}=4.5V I_O=2.4mA		0.1	0.5	
Switching (V_{CC}=5V)							
Propagation delay time to logic low	6N135	T_{PHL}	T_A=25°C, (R_L=4.1kΩ, I_F=16mA) (Note 2)		0.45	1.5	μs
			(R_L=4.1kΩ, I_F=16mA) (Note 3)			2	
	6N136		T_A=25°C, (R_L=1.9kΩ, I_F=16mA) (Note 2)		0.2	0.8	
			(R_L=1.9kΩ, I_F=16mA) (Note 3)			1	
Propagation delay time to logic high	6N135	T_{PLH}	T_A=25°C, (R_L=4.1kΩ, I_F=16mA) (Note 2)		0.5	1.5	μs
			(R_L=4.1kΩ, I_F=16mA) (Note 3)			2	
	6N136		T_A=25°C, (R_L=4.1kΩ, I_F=16mA) (Note 2)		0.6	0.8	
			(R_L=4.1kΩ, I_F=16mA) (Note 3)			1	

Common mode transient immunity at logic high	6N135	$\|CM_H\|$	I_F=0mA, V_{CM}=10V_{P-P} R_L=4.1kΩ) (Note 4) T_A=25°C		10000		V/μs
	6N136		I_F=0mA, V_{CM}=10V_{P-P} R_L=1.9kΩ) (Note 4) T_A=25°C		10000		
Common mode transient immunity at logic low	6N135	$\|CM_L\|$	I_F=16mA, V_{CM}=10V_{P-P} R_L=4.1kΩ) (Note 4) T_A=25°C		10000		
	6N136		I_F=0mA, V_{CM}=10V_{P-P} R_L=1.9kΩ) (Note 4) T_A=25°C		10000		
Isolation							
Input-output insulation leakage current		I_{I-O}	Relative humidity=45% T_A=25°C, t=5s V_{I-O}=3000V_{DC} (Note 5)			1	μA
Withstand insulation test voltage		V_{ISO}	RH≤50%, T_A=25°C (Note5) t=1min.	5000			V_{RMS}
Resistance (input to output)		R_{I-O}	(Note 5) V_{I-O}=500V_{DC}		10^{12}		Ω
Capacitance (input to output)		C_{I-O}	(Note 5) f=1MHz		0.6		pF
DC Current gain		H_{FE}	I_O=3mA, V_O=5V		150		

Notes:

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

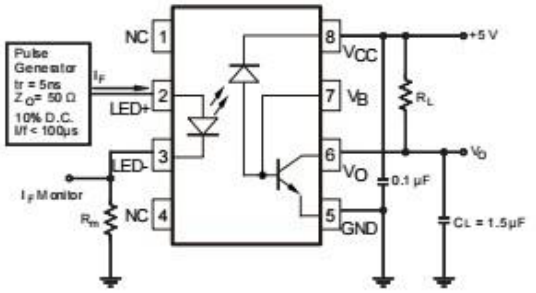
2. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1kΩ pull-upresistor.

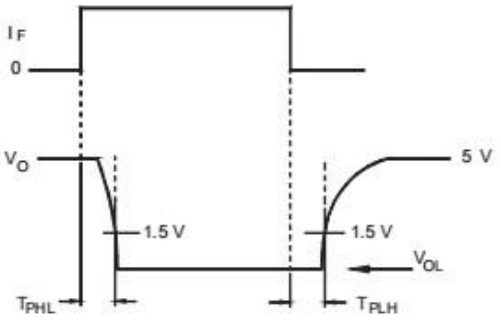
3. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull-up resistor.

4. Common mode transient immunity in logic high level is the maximum tolerable (positive) dVcm/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dVcm/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O<0.8 V).

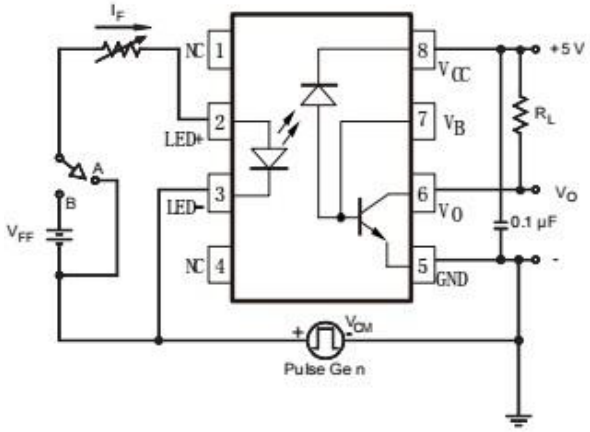
5. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 areshorted together.

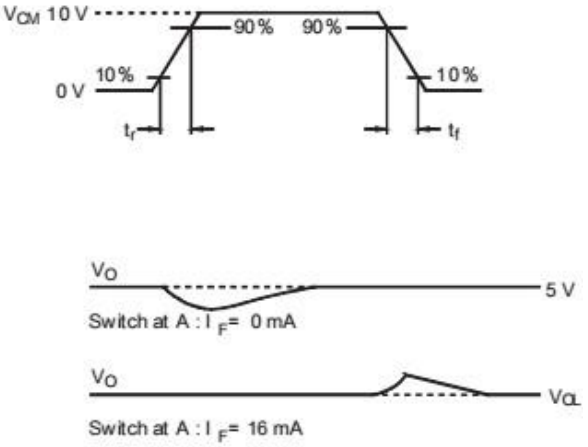
7.Test Circuits





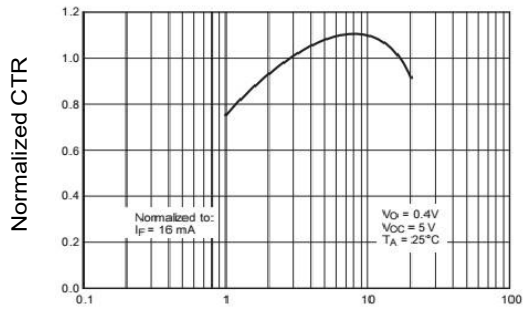
Switching Time Test Circuit





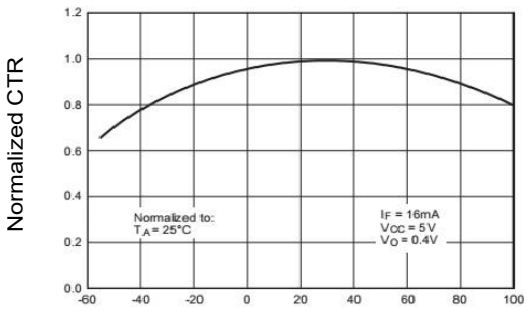
Common Mode Immunity Test Circuit

8.Typical characteristic



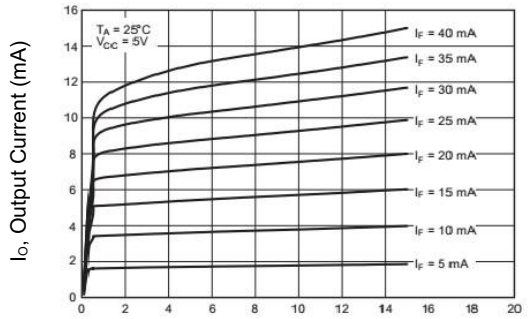
I_F, Forward Current (mA)

Figure 1: Normalized CTR vs.Forward Current



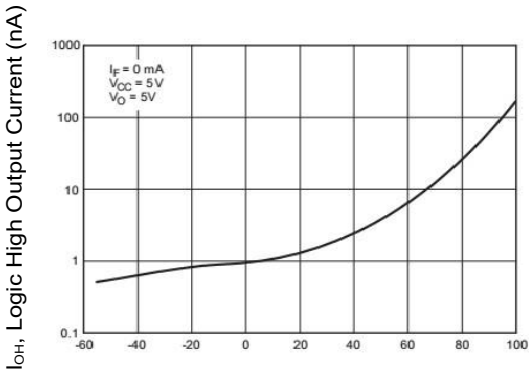
T_A, Temperature(°C)

Figure 2: Nomalized CTR vs.Temperature



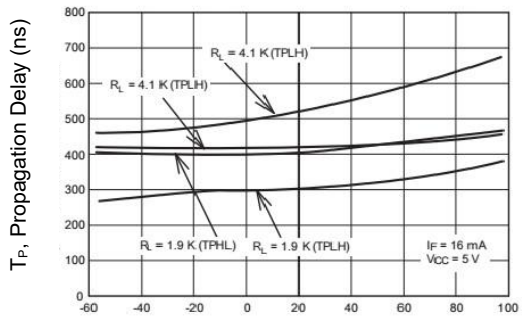
V_O, Output Voltage (V)

Figure 3: Output Current vs.Output Voltage



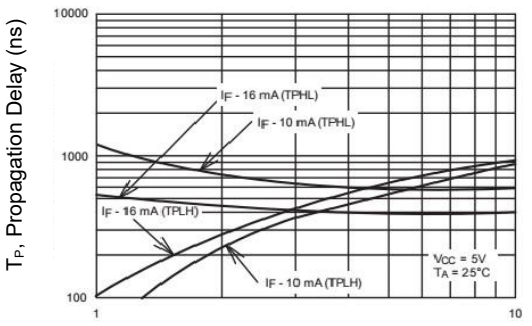
T_A, Temperature(°C)

Figure 4: Logic High Output Current vs.Temperature



T_A, Temperature(°C)

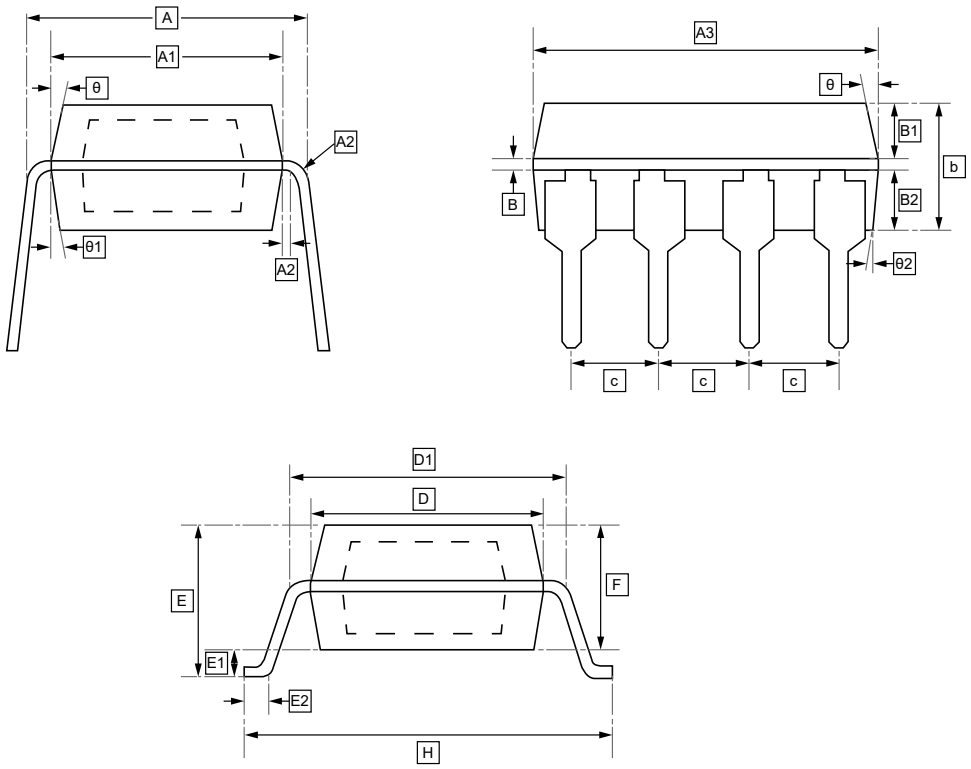
Figure 5: Prpagation Delay vs.Temperature



R_L= Load Resistance (kΩ)

Figure 6: Popagation Delay vs.Load Resistance

9.DIP-8/SOP-8 Package Outline Dimensions

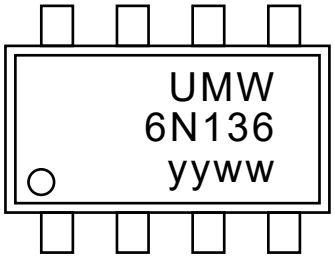


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	B2	b	c	D	D1	E
Min	7.65	6.55	0.2	9.71	0.25	1.6	1.62	3.45	2.54	6.55	7.65	4.15
Max	7.95	6.65	(typ.)	9.78	(typ.)	(typ.)	1.68	3.55	(typ.)	6.65	7.95	4.35

Symbol	E1	E2	F	H	θ	θ1	θ2
Min	0.75	0.66	3.45	10.1	12°	9°	5°
Max	(typ.)	(typ.)	3.55	10.5	(typ.)	(typ.)	(typ.)

10.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW 6N135M	6N135	DIP-8	2250	Tube and box
UMW 6N135S	6N135	SOP-8	1000	Tape and reel
UMW 6N136M	6N136	DIP-8	2250	Tube and box
UMW 6N136S	6N136	SOP-8	1000	Tape and reel

11.Disclaimer

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