UMW®

UMW FDD24AN06LA0

60V N-Channel MOSFET

1.Features

- $V_{DS\ (V)}$=60V
- I_D=40A(V_{GS}=10V)
- $R_{DS(ON)}$<19mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<24mΩ(V_{GS}=4.5V)
- Low Miller Charge
- Low Q_{rr} Body Diode

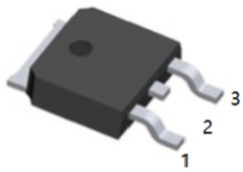
2.Applications

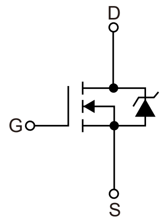
- Motor / Body Load Control
- ABS Systems
- Powertrain Management
- Injection Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 12V and 24V systems

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_C= 25°C

Parameter	Symbol	Rating	Units
Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (T_C=25°C, V_{GS}=10V)	I_D	40	A
Continuous (T_C=25°C, V_{GS}=5V)		36	A
Continuous (T_C=100°C, V_{GS}=5V)		25	A
Continuous (T_C=25°C, V_{GS}=5V, $R_{\theta JA}$=52°C/W)		7.1	A
Pulsed		Figure 4	A
Single Pulse Avalanche Energy (Note 1)	E_{AS}	32	mJ
Power Dissipation	P_D	75	W
Derate above 25°C		0.5	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Case TO-252	$R_{\theta JC}$	2	°C/W
Thermal Resistance, Junction-to-Ambient TO-252	$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction-to-Ambient TO-252,1in^2 copper pad area	$R_{\theta JA}$	52	°C/W

6.Electrical Characteristic (T$_C$=25°C unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Off Characteristics							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V		60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=50V				1	μA
		V_{GS}=0V	T_J=150°C			250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V				±100	nA
On Characteristics							
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA		1		2	V
Drain to Source On Resistance	$R_{DS(ON)}$	I_D=40A, V_{GS}=10V			16	19	mΩ
		I_D=36A, V_{GS}=5V			20	24	mΩ
Dynamic Characteristics							
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz			1850		pF
Output Capacitance	C_{oss}				180		pF
Reverse Transfer Capacitance	C_{rss}				75		pF
Total Gate Charge at 5V	$Q_{g(TOT)}$	V_{GS}=0V to 5V	V_{DD}=30V		16	21	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS}=0V to 1V	I_D=36A		1.8	2.4	nC
Gate to Source Gate Charge	Q_{gs}		I_g=1mA		6.3		nC
Gate Charge Threshold to Plateau	Q_{gs2}				4.5		nC
Gate to Drain “Miller” Charge	Q_{gd}				5		nC
Switching Characteristics (V_{GS}=5V)							
Turn-On Time	$t_{(on)}$	V_{DD}=30V, I_D=36A V_{GS}=5V, R_{GS}=9.1Ω				195	ns
Turn-On Delay Time	$t_{D(on)}$				12		ns
Rise Time	t_r				118		ns
Turn-Off DelayTime	$t_{D(off)}$				26		ns
Fall Time	t_f				41		ns
Turn-Off Time	t_{off}					101	ns

Drain–Source Diode Characteristics						
Source to Drain Diode Forward Voltage	V_{SD}	I_{SD}=36A			1.25	V
		I_{SD}=18A			1	V
Reverse Recovery Time	t_{rr}	I_F=36A, di/dt=100A/μs			34	ns
Reverse Recovery Charge	Q_{rr}	I_F=36A, di/dt=100A/μs			30	nC

Notes:

1: Starting T_J=25°C, L=80μH, I_{AS}=28A.

7.1Typical characteristic

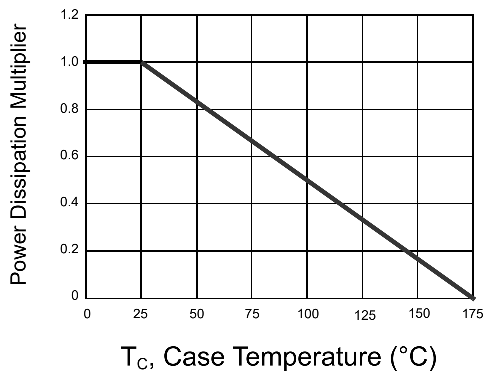


Figure 1: Normalized Power Dissipation vs Case Temperature

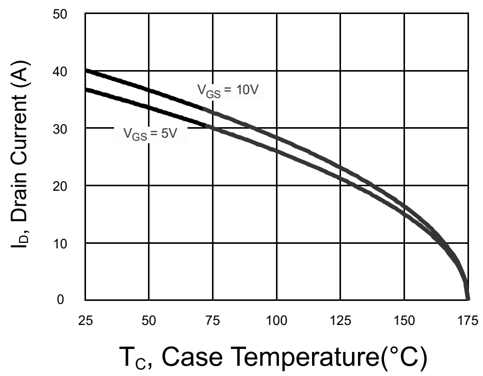


Figure 2: Maximum Continuous Drain Current vs Case Temperature

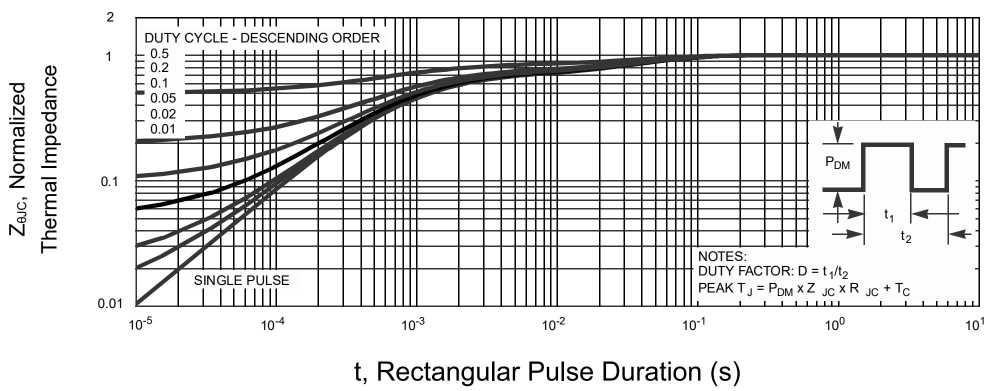


Figure 3: Normalized Maximum Transient Thermal Impedance

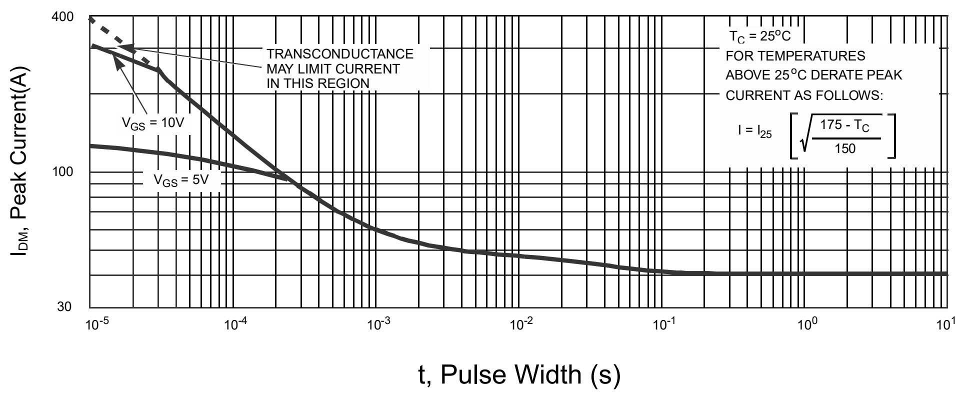


Figure 4: Peak Current Capability

7.2Typical characteristic

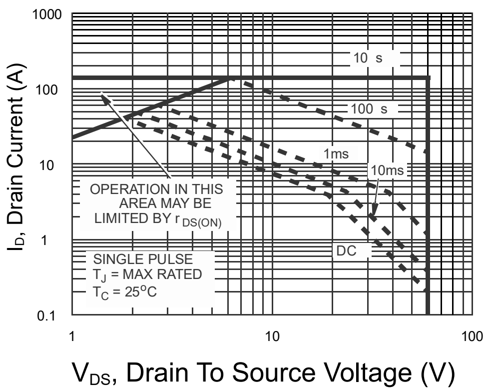


Figure 5: Forward Bias Safe Operating Area

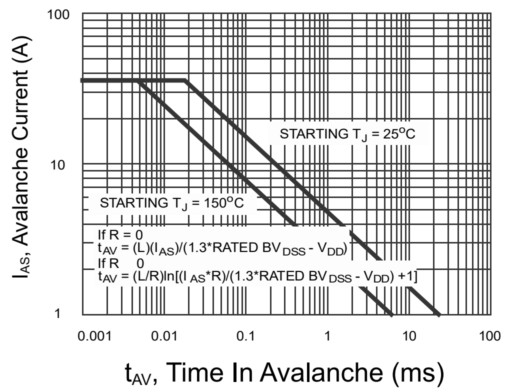


Figure 6: Unclamped Inductive Switching Capability

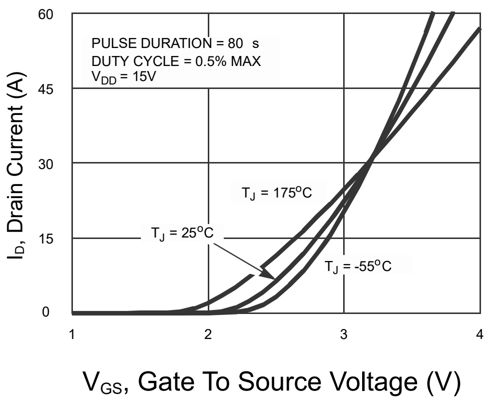


Figure 7: Transfer Characteristics

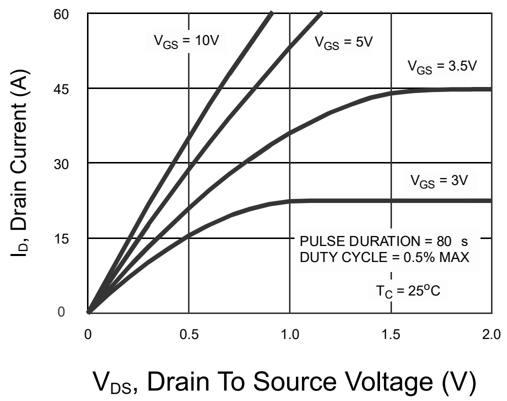


Figure 8: Saturation Characteristics

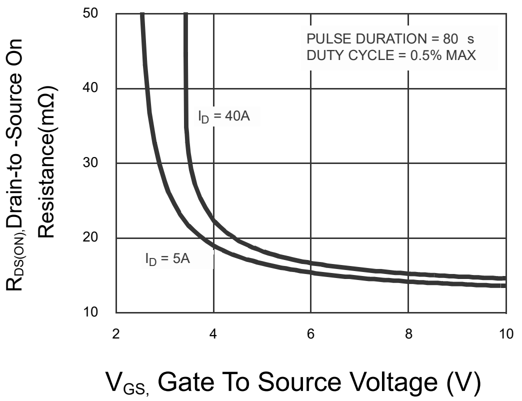


Figure 9: Drain to Source On Resistance vs Gate Voltage and Drain Current

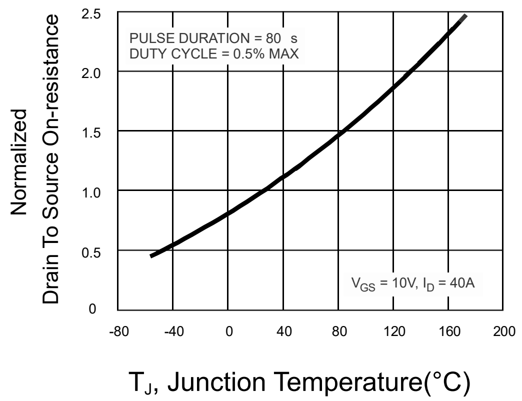


Figure 10: Normalized Drain to Source On Resistance vs Junction Temperature

7.3Typical characteristic

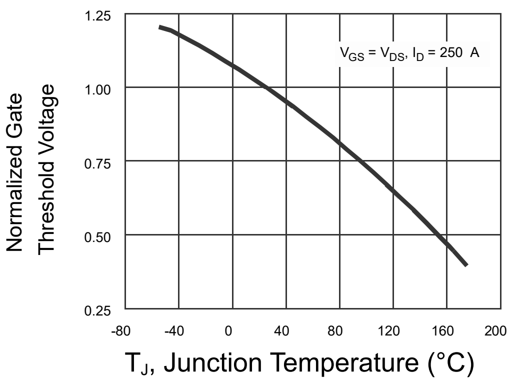


Figure 11: Normalized Gate Threshold Voltage vs Junction Temperature

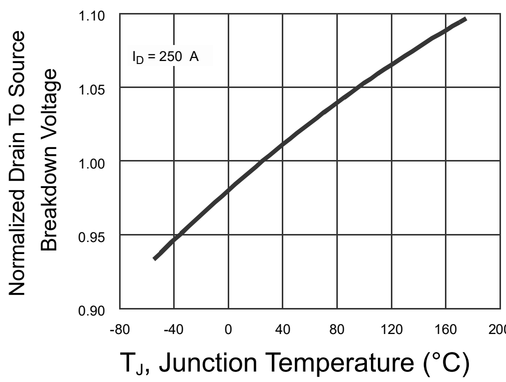


Figure 12: Normalized Drain to Source Breakdown Voltage vs Junction Temperature

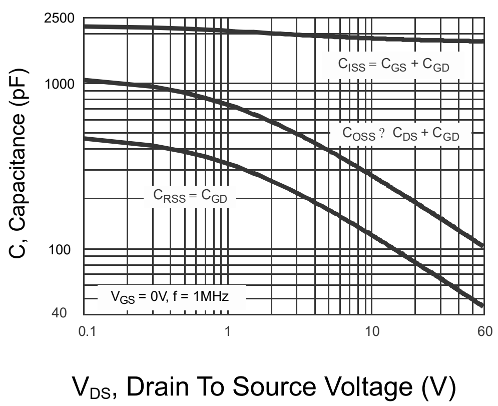


Figure 13: Capacitance vs Drain to Source Voltage

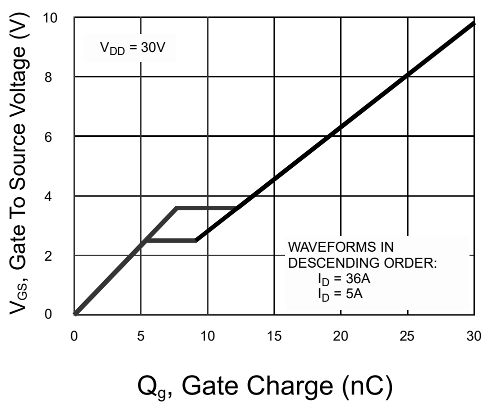


Figure 14: Gate Charge Waveforms for Constant Gate Current

7.4Typical characteristic

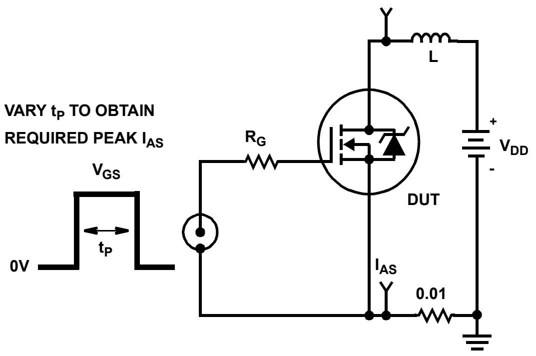


Figure 15. Unclamped Energy Test Circuit

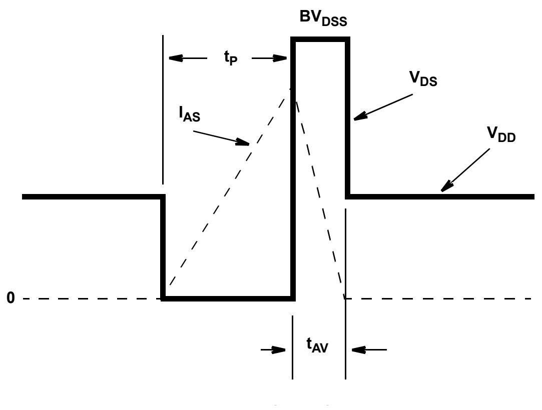


Figure 16. Unclamped Energy Waveforms

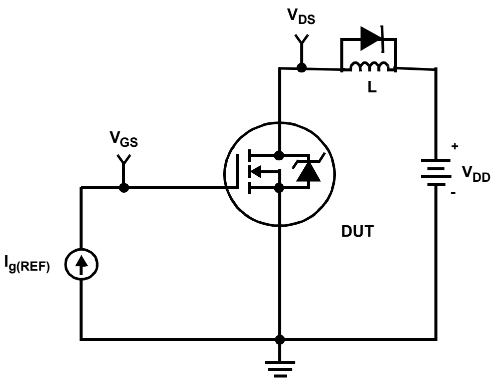


Figure 17. Gate Charge Test Circuit

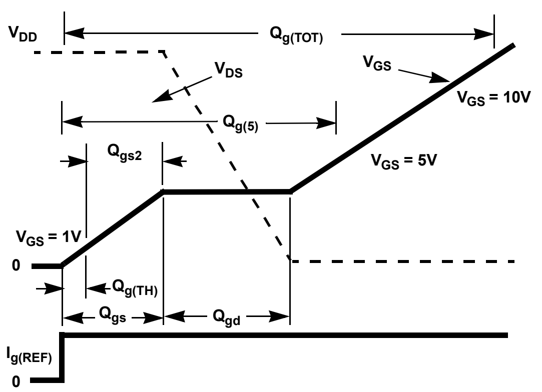


Figure 18. Gate Charge Waveforms

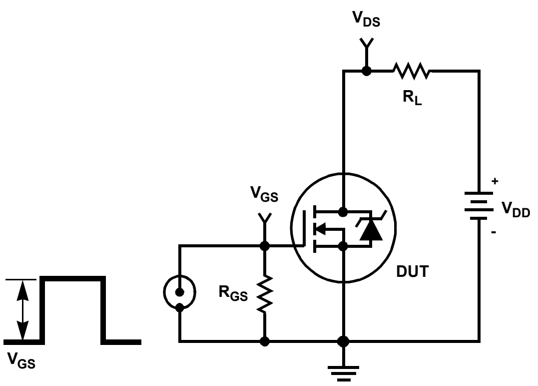


Figure 19. Switching Time Test Circuit

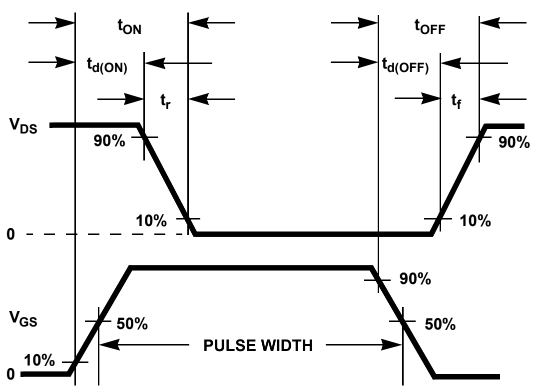


Figure 20. Switching Time Waveforms

7.5Typical characteristic

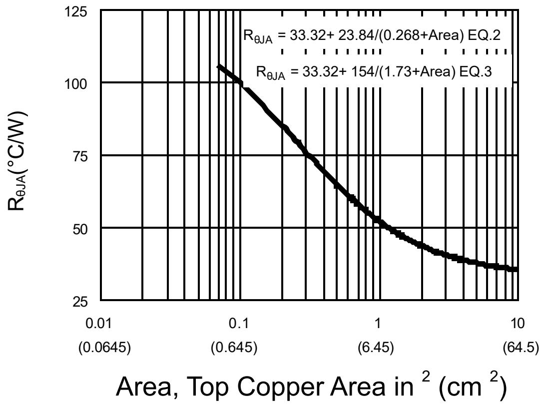


Figure 21: Thermal Resistance vs Mounting Pad Area

Notes:

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A(°C), and thermal resistance $R_{\theta JA}$(°C/W) must be reviewed to ensure that T_{JM} is never exceeded.Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM}-T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of PDM is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Figure 21 defines the RθJA for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

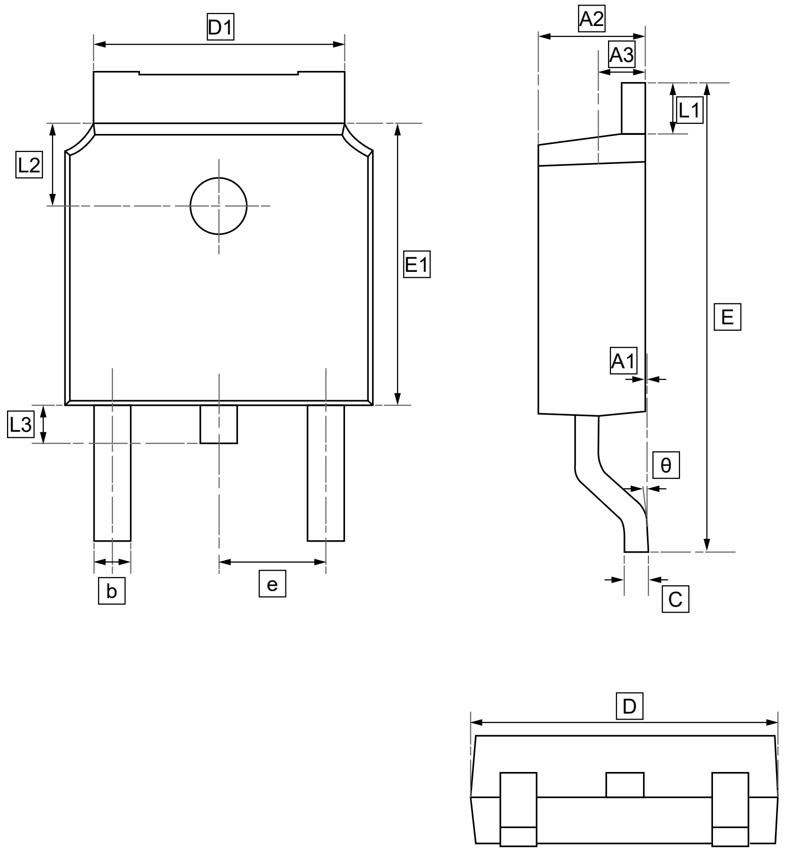
$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268+Area)} \qquad \text{(EQ. 2)}$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73+Area)} \qquad \text{(EQ. 3)}$$

Area in Centimeters Squared

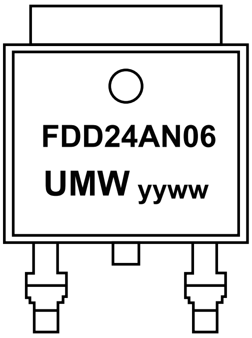
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286 BSC	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38		1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD24AN06LA0	TO-252	2500	Tape and reel

10.Disclaimer

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