UMW ADA4051

1.8V, Micropower, Zero-Drift, Rail-to-Rail Input /Output OpAmps

1.Description

The ADA4051-1 are CMOS, micropower, zero-drift operational amplifiers utilizing an innovative chopping technique. These amplifiers feature rail-to-rail input/ output swing and extremely low offset voltage while operating from a 1.8V to 5.5V power supply. In addition, these amplifiers offer high power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) while operating with a typical supply current of 13 μA per amplifier. This combination of features makes the ADA4051-1 amplifiers ideal choices for battery-powered applications where high precision and low power consumption are important.

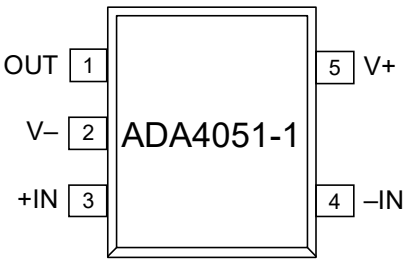
2.Features

- Very low supply current: 13μA typical
- Low offset voltage: 15μV maximum
- Offset voltage drift: 20nV/°C
- Single-supply operation: 1.8V to 5.5V
- High PSRR: 110dB minimum
- High CMRR: 110dB minimum
- Rail-to-rail input/output
- Unity-gain stable
- Extended industrial temperature range

3.Applications

- Pressure and position sensors
- Temperature measurements
- Electronic scales
- Medical instrumentation
- Battery-powered equipment
- Handheld test equipment

4.Pinning Information



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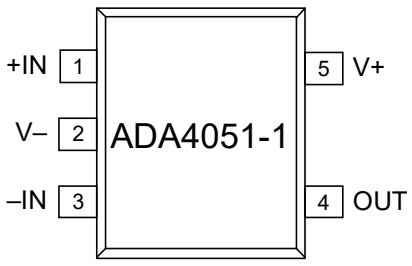


SC-70-5

5.Absolute Maximum Ratings

Parameter	Rating
supply Voltage	6 V
Input Voltage	$\pm V_{SY}$ ± 0.3V
Input Current (1)	±10mA
Differential input Voltage (2)	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +150°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Notes:

1. The input pins have clamp di odes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3V.

2. Inputs are protected against high differential voltages by internal series 1.33kΩ resistors and back -to -back diode -connected N-MOSFETs (with a typical V_T of 0.7V for V_{CM} of 0V).

6.1 Electrical Characteristics

V_{SY}=1.8V, V_{CM}= V_{SY}/2V, T_A=25°C, R_L=100kΩ to GND , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V_{OS}	0V≤V_{CM}≤1.8V		2	15	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C≤T_A≤125°C		0.02	0.1	μV/°C
Input Bias Current	I_B			5	50	pA
		-40°C≤T_A≤125°C			200	pA
Input Offset Current	I_{OS}			10	100	pA
		-40°C≤T_A≤125°C			150	pA
Input Voltage Range		-40°C≤T_A≤125°C	0		1.8	V
Common -Mode Rejection Ratio	CMRR	0V≤V_{CM}≤1.8V	105	125		dB
		-40°C≤T_A≤125°C	100			dB
Large-Signal Voltage Gain	A_{VO}	R_L=10kΩ to V_{CM}, 0.1V≤V_{OUT}≤V_{SY}-0.1V	106	130		dB
		-40°C≤T_A≤125°C	100			dB
Differential Mode	R_{IN}			8		MΩ
Input Capacitance,Differential Mode	C_{INDM}			2		pF
Input Capacitance,Common Mode	C_{INCM}			5		pF
Output Voltage High	V_{OH}	R_L=100kΩ to V_{CM}	1.796	1.799		V
		-40°C≤T_A≤125°C	1.79			V
		R_L=10kΩ to V_{CM}	1.76	1.796		V
		-40°C≤T_A≤125°C	1.7			V
Output Voltage Low	V_{OL}	R_L=100kΩ to V_{CM}		1	3	mV
		-40°C≤T_A≤125°C			9	mV
		R_L=10kΩ to V_{CM}		3	20	mV
		-40°C≤T_A≤125°C			40	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Short-Circuit Current	I_{SC}	V_{OUT}=V_{SY} or GND		13		mA
Closed-Loop Output Impedance	Z_{OUT}	f=1kHz, G=10		1		Ω
Power Supply Rejection Ratio	PSRR	1.8V≤V_{SY}≤5.5V	110	135		dB
		-40°C≤T_A≤125°C	106			dB
Supply Current per Amplifier ADA4051-1	I_{SY}	V_{OUT}=V_{SY}/2		13	17	μA
		-40°C≤T_A≤125°C			20	μA
Slew Rate	SR+	R_L=10kΩ, C_L=100pF, G=1		0.04		V/μs
	SR-	R_L=10kΩ, C_L=100pF, G=1		0.03		V/μs
Settling Time	t_s	To 0.1%, V_{IN}=1V p-p R_L=10kΩ, C_L=100pF		120		μs
Gain Bandwidth Product	GBP	C_L=100pF, G=1		115		kHz
Phase Margin	Φ_M	C_L=100pF, G=1		40		Degrees
Channel Separation	CS	V_{IN}=1.7V, f=100Hz		140		dB
Voltage Noise	e_n p-p	f=0.1Hz to 10Hz		1.96		μV p-p
Volta ge Noise Density	e_n	f=1kHz		95		nV/√Hz
Current Noise Density	i_n	f=1kHz		100		fA/√Hz

6.2 Electrical Characteristics

V_{SY}=5.0V, V_{CM}= V_{SY}/2V, T_A=25°C, R_L=100kΩ to GND , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V_{OS}	0V≤V_{CM}≤5V		2	15	μV
ADA4051 -1		-40°C≤T_A≤125°C			27	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C≤T_A≤125°C		0.02	0.1	μV/°C
Input Bias Current	I_B			20	70	pA
		-40°C≤T_A≤125°C			200	pA
Input Offset Current	I_{OS}			40	100	pA
		-40°C≤T_A≤125°C			150	pA
Input Voltage Range		-40°C≤T_A≤125°C	0		5	V
Common -Mode Rejection Ratio	CMRR	0V≤V_{CM}≤5V	110	135		dB
		-40°C≤T_A≤125°C	106			dB
Large-Signal Voltage Gain	A_{VO}	R_L=10kΩ to V_{CM},0.1V≤V_{OUT}≤V_{SY}-0.1V	115	135		dB
		-40°C≤T_A≤125°C	106			dB
Differential Mode	R_{IN}			8		MΩ
Input Capacitance,Differential Mode	C_{INDM}			2		pF
Input Capacitance,Common Mode	C_{INCM}			5		pF
Output Voltage High	V_{OH}	R_L=100kΩ to V_{CM}	4.996	4.998		V
		-40°C≤T_A≤125°C	4.985			V
		R_L=10kΩ to V_{CM}	4.96	4.99		V
		-40°C≤T_A≤125°C	4.9			V
Output Voltage Low	V_{OL}	R_L=100kΩ to V_{CM}		1	4	mV
		-40°C≤T_A≤125°C			13	mV
		R_L=10kΩ to V_{CM}		9	30	mV
		-40°C≤T_A≤125°C			90	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Short-Circuit Current	I_{SC}	V_{OUT}=V_{SY} or GND		15		mA
Closed-Loop Output Impedance	Z_{OUT}	f=1kHz, G=10		1		Ω
Power Supply Rejection Ratio	PSRR	1.8V≤V_{SY}≤5.5V	110	135		dB
		-40°C≤T_A≤125°C	106			dB
Supply Current per Amplifier ADA4051-1	I_{SY}	V_{OUT}=V_{SY}/2		13	17	μA
		-40°C≤T_A≤125°C			20	μA
Slew Rate	SR+	R_L=10kΩ, C_L=100pF, G=1		0.06		V/μs
	SR-	R_L=10kΩ, C_L=100pF, G=1		0.04		V/μs
Settling Time	t_s	To 0.1%, V_{IN}=1V p-p		110		μs
		R_L=10kΩ, C_L=100pF				
Gain Bandwidth Product	GBP	C_L=100pF, G=1		125		kHz
Phase Margin	Φ_M	C_L=100pF, G=1		40		Degrees
Channel Separation	CS	V_{IN}=4.99V, f=100Hz		140		dB
Voltage Noise	e_n p-p	f=0.1Hz to 10Hz		1.96		μV p-p
Volta ge Noise Density	e_n	f=1kHz		95		nV/√Hz
Current Noise Density	i_n	f=1kHz		100		fA/√Hz

7.1 Typical Characteristic

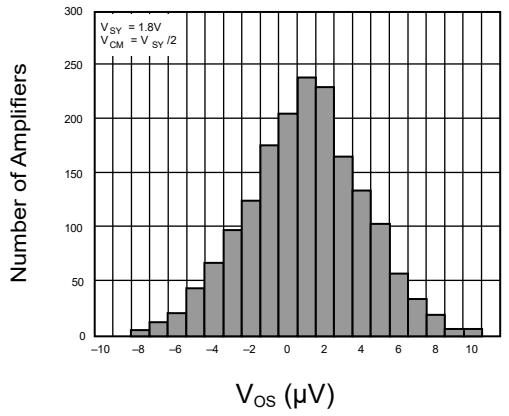


Figure 1: Input Offset Voltage Distribution

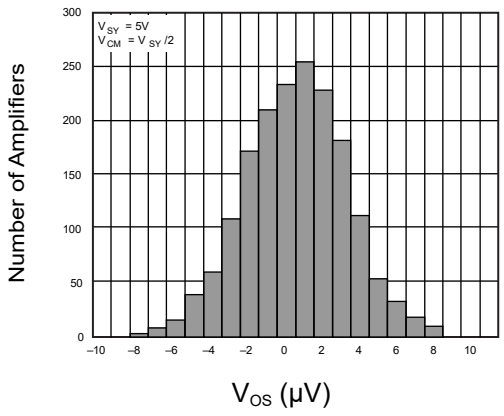


Figure 2: Input Offset Voltage Distribution

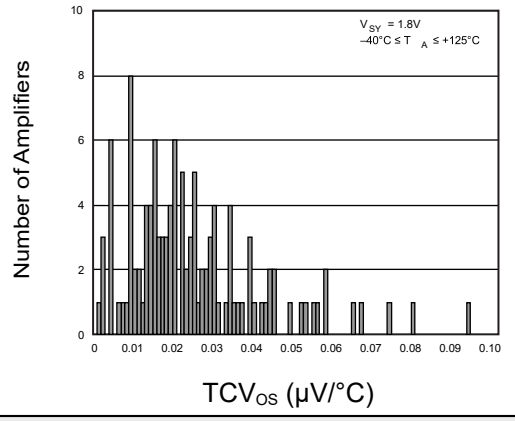


Figure 3: Input Offset Voltage Drift Distribution with Temperature

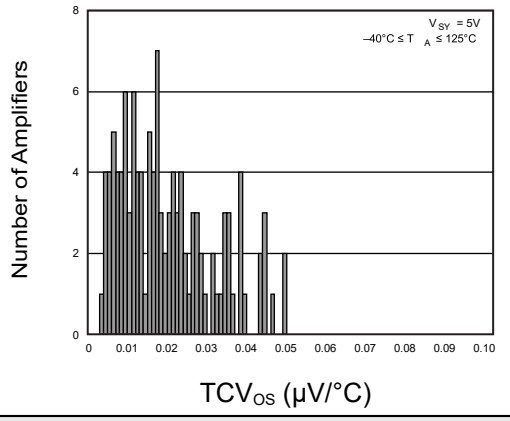


Figure 4: Input Offset Voltage Drift Distribution with Temperature

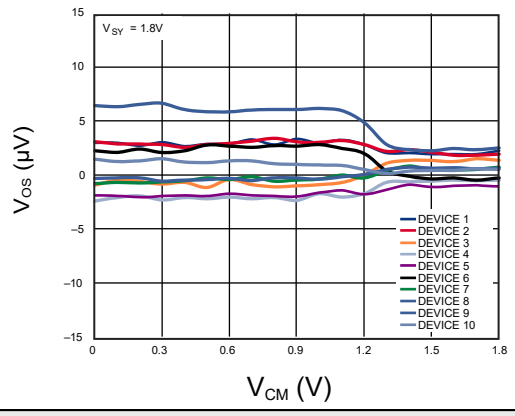


Figure 5: Input Offset Voltage vs. Input Common-Mode Voltage

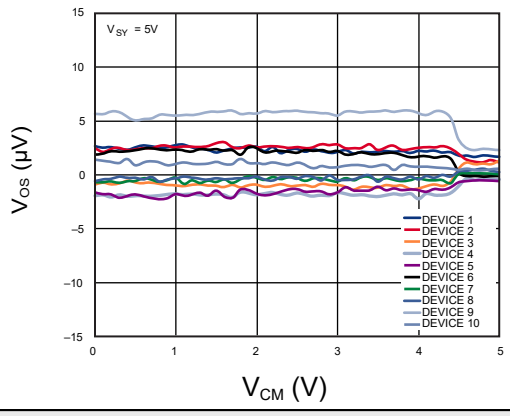


Figure 6: Input Offset Voltage vs. Input Common -Mode Voltage

7.2 Typical Characteristic

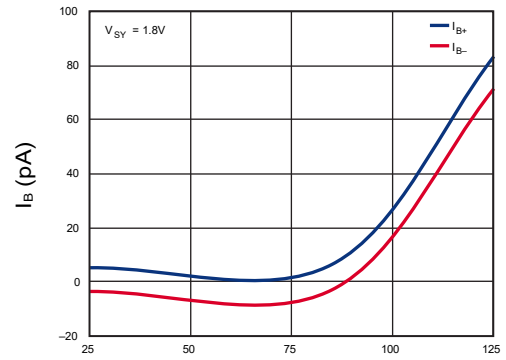


Figure 7: Input Bias Current vs. Temperature

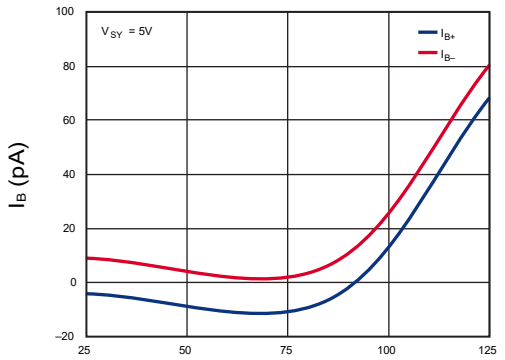


Figure 8: Input Bias Current vs. Temperature

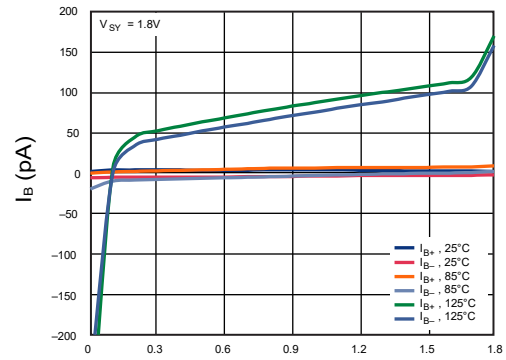


Figure 9: Input Bias Current vs. Common-Mode Voltage and Temperature

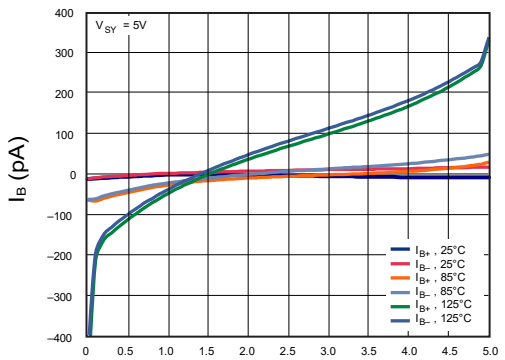


Figure 10: Input Bias Current vs. Common-Mode Voltage and Temperature

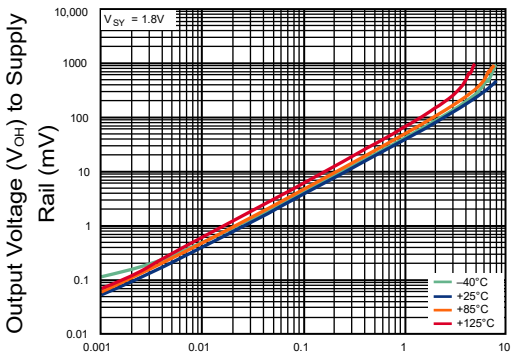


Figure 11: Output Voltage (V_{OH}) to Supply Rail vs. Load Current and Temperature

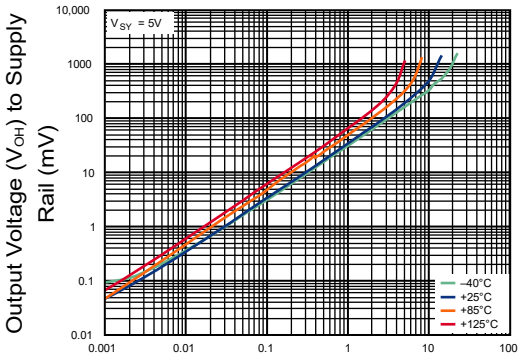


Figure 12: Output Voltage (V_{OH}) to Supply Rail vs. Load Current and Temperature

7.3 Typical Characteristic

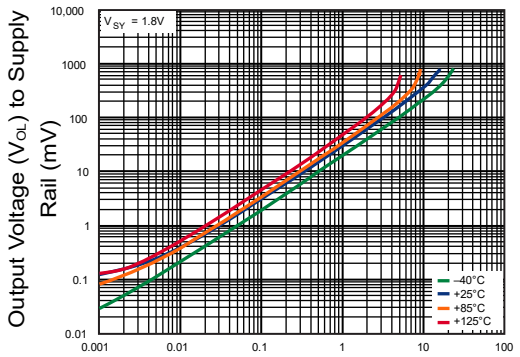


Figure 13: Output Voltage (V_{OL}) to Supply Rail vs. Load Current and Temperature

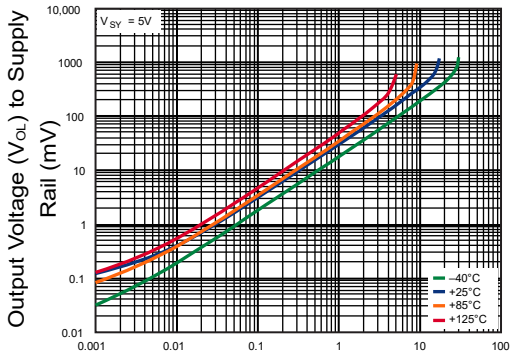


Figure 14: Output Voltage (V_{OL}) to Supply Rail vs. Load Current and Temperature

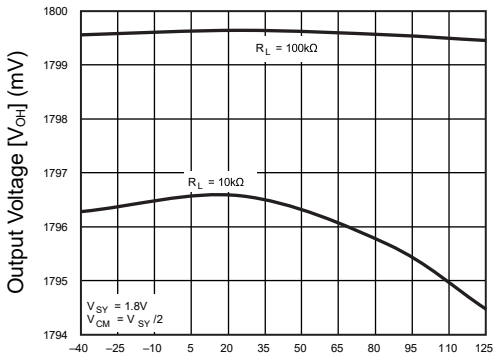


Figure 15: Output Voltage (V_{OH}) vs. Temperature

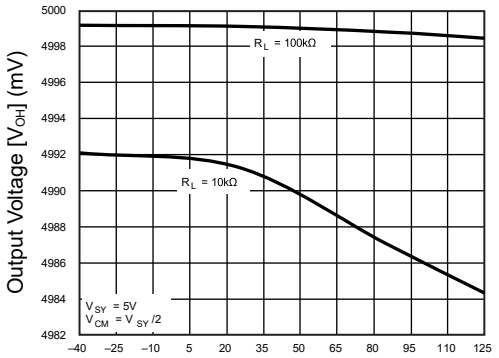


Figure 16: Output Voltage (V_{OH}) vs. Temperature

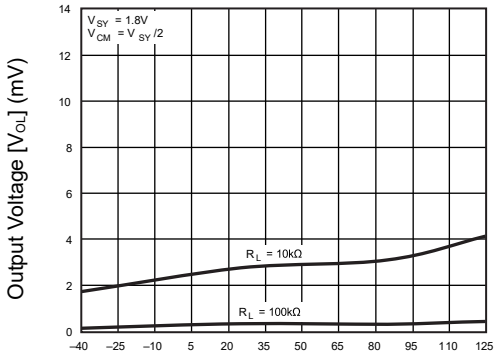


Figure 17: Output Voltage (V_{OL}) vs. Temperature

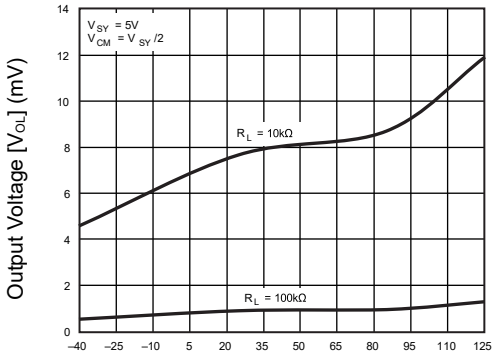


Figure 18: Output Voltage (V_{OL}) vs. Temperature

7.4 Typical Characteristic

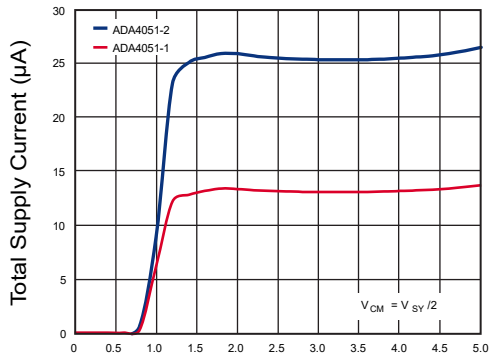


Figure 19: Total Supply Current vs. Supply Voltage

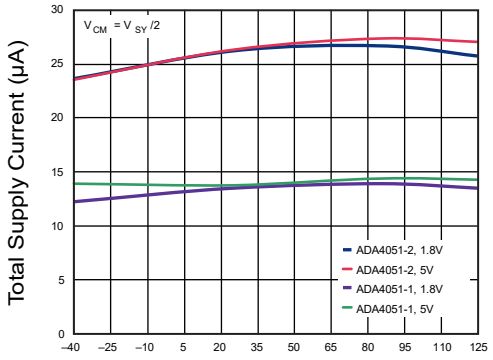


Figure 20: Total Supply Current vs. Temperature

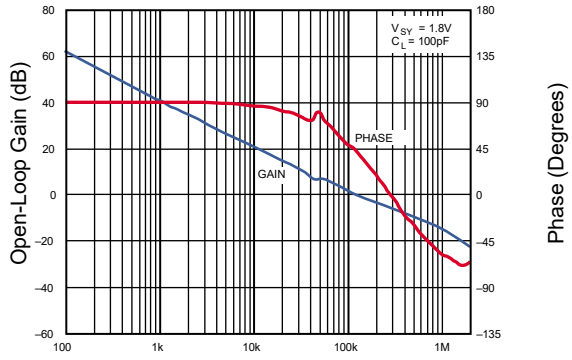


Figure 21: . Open-Loop Gain and Phase vs. Frequency

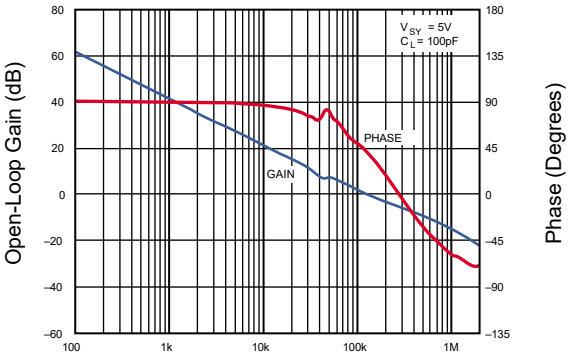


Figure 22: Open-Loop Gain and Phase vs. Frequency

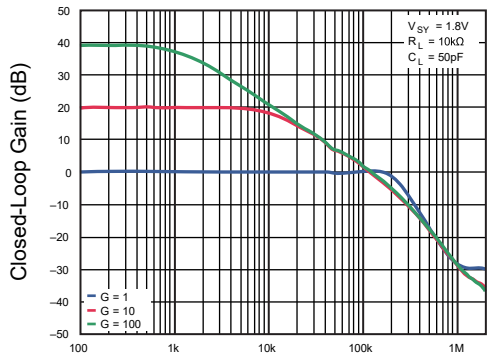


Figure 23: Closed-Loop Gain vs. Frequency

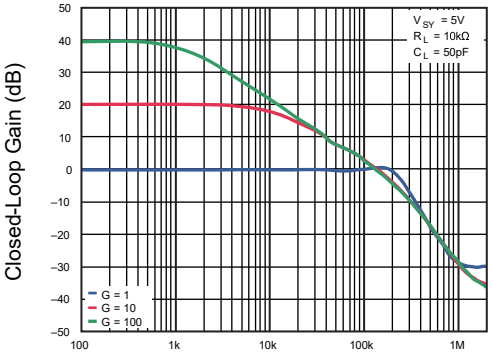


Figure 24: Closed-Loop Gain vs. Frequency

7.5 Typical Characteristic

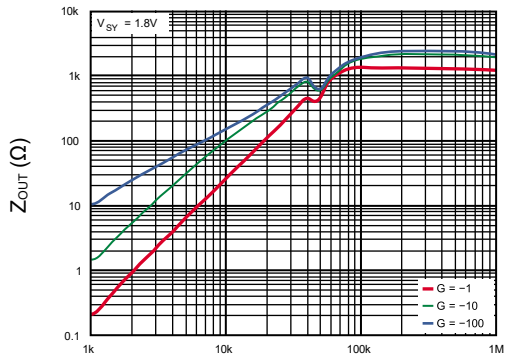


Figure 25: Output Impedance vs. Frequency

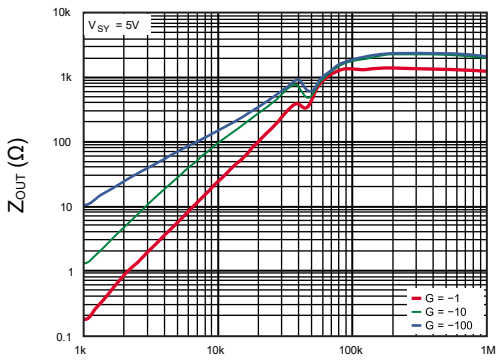


Figure 26: Output Impedance vs. Frequency

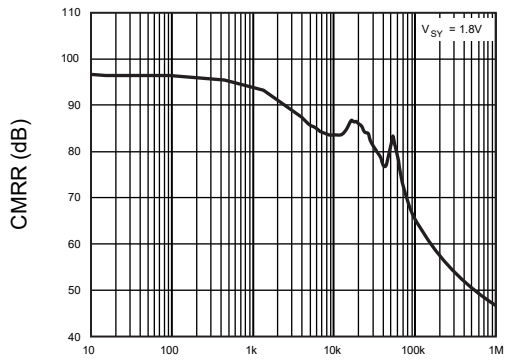


Figure 27: CMRR vs. Frequency

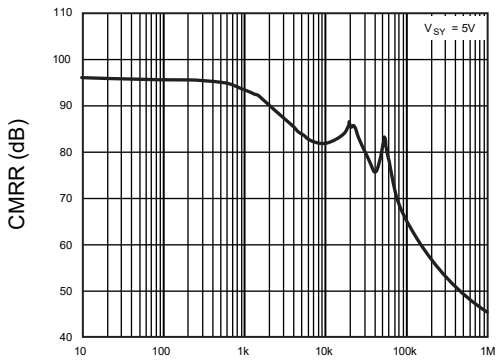


Figure 28: CMRR vs. Frequency

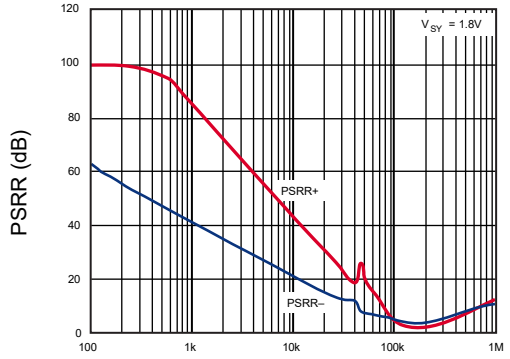


Figure 29: PSRR vs. Frequency

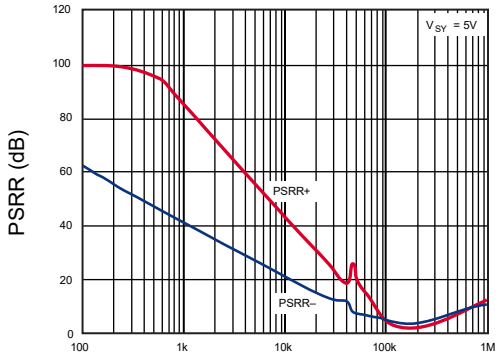


Figure 30: PSRR vs. Frequency

7.6 Typical Characteristic

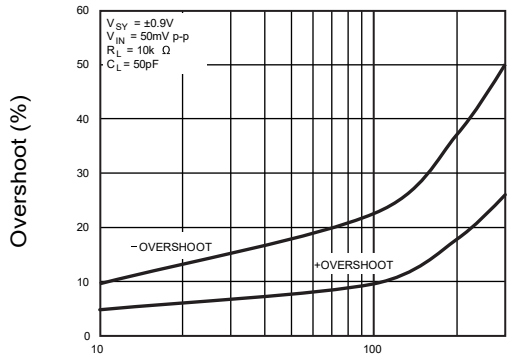


Figure 31: Small-Signal Overshoot vs. Load Capacitance

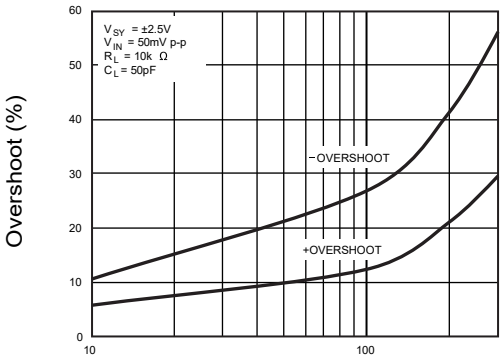


Figure 32: Small-Signal Overshoot vs. Load Capacitance

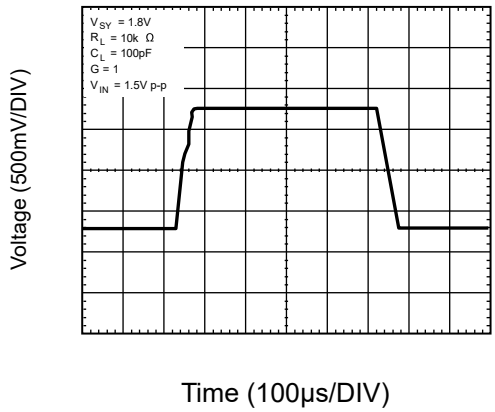


Figure 33: Large-Signal Transient Response

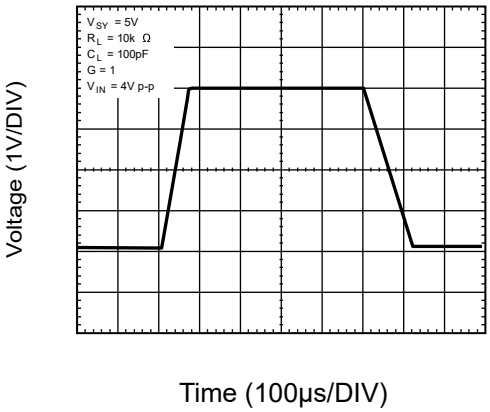


Figure 34: Large-Signal Transient Response

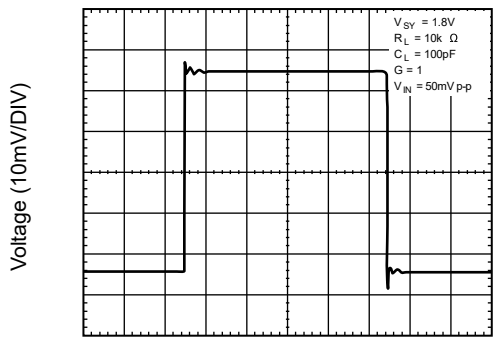


Figure 35: Small-Signal Transient Response

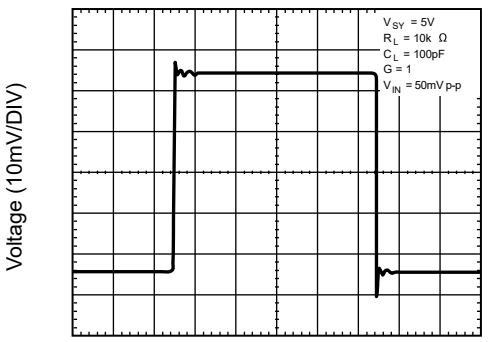


Figure 36: Small-Signal Transient Response

7.7 Typical Characteristic

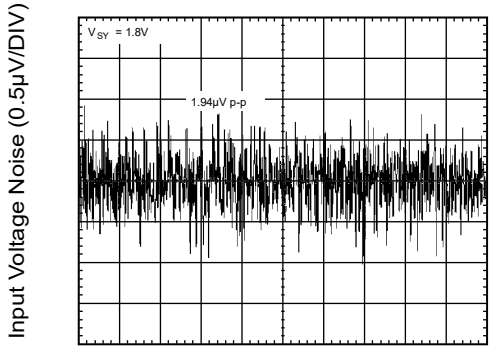


Figure 37: Input Voltage Noise, 0.1 Hz to 10 Hz

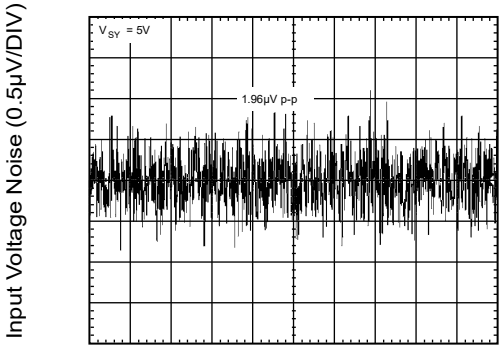


Figure 38: Input Voltage Noise, 0.1 Hz to 10 Hz

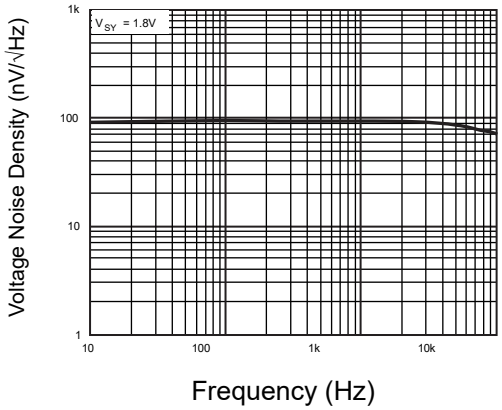


Figure 39: Voltage Noise Density vs. Frequency

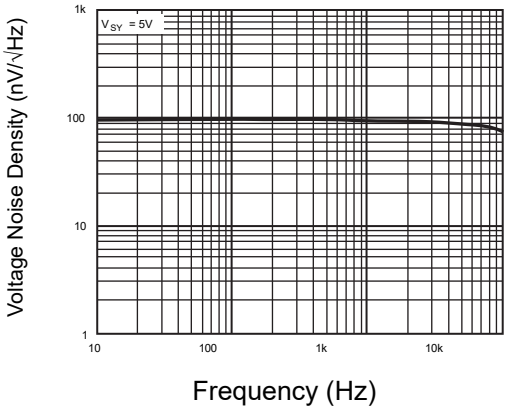


Figure 40: Voltage Noise Density vs. Frequency

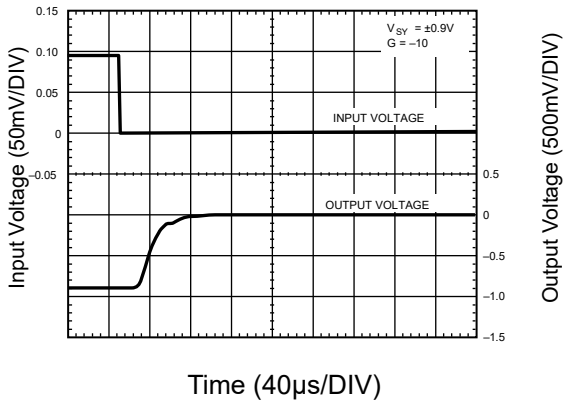


Figure 41: Positive Overload Recovery

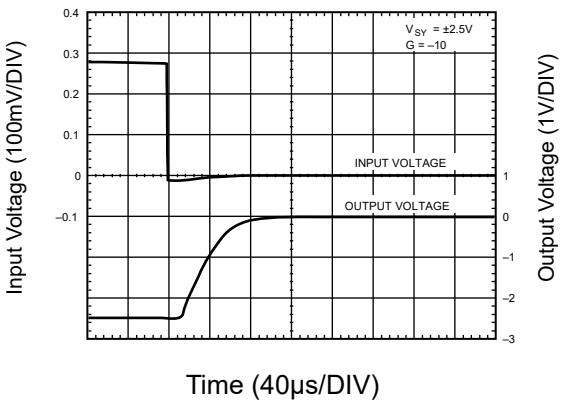


Figure 42: Positive Overload Recovery

7.8 Typical Characteristic

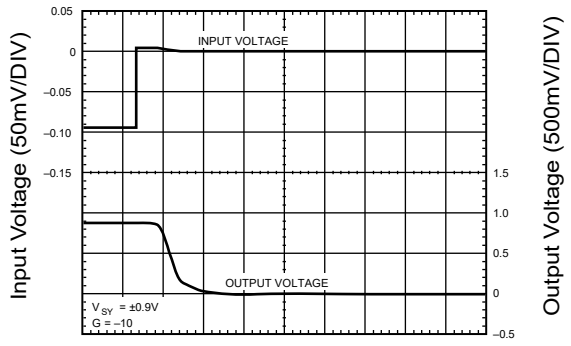


Figure 43: Negative Overload Recovery

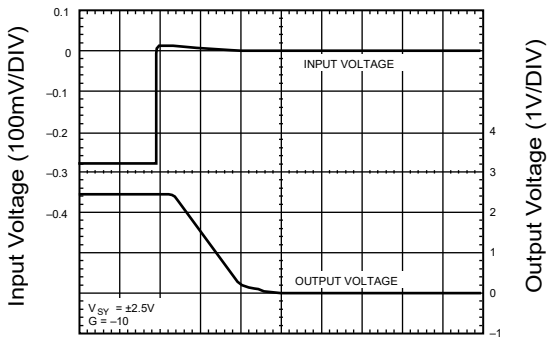


Figure 44: Negative Overload Recovery

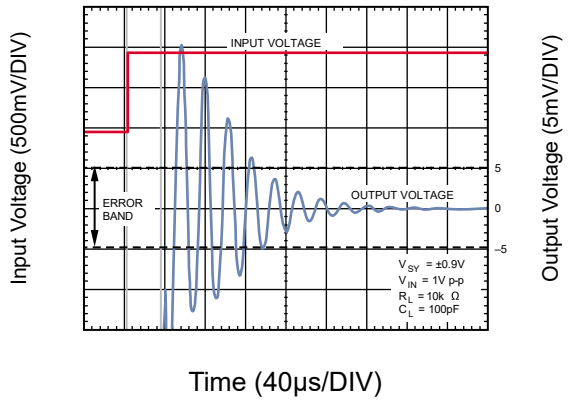


Figure 45: Positive Settling Time to 0.1%

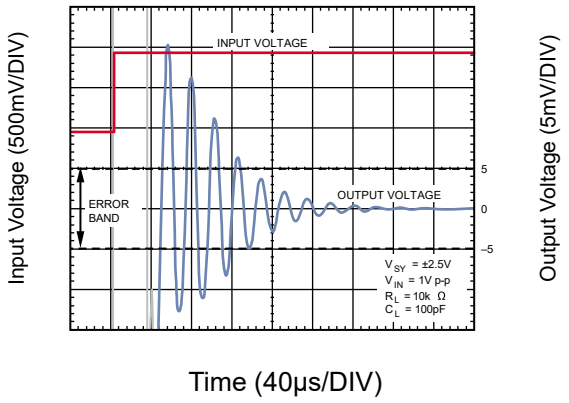


Figure 46: Positive Settling Time to 0.1%

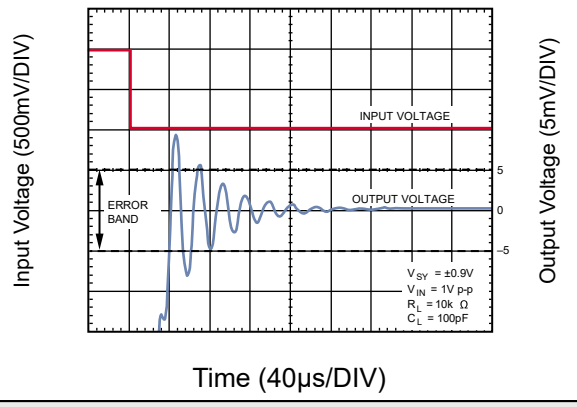


Figure 47: Negative Settling Time to 0.1%

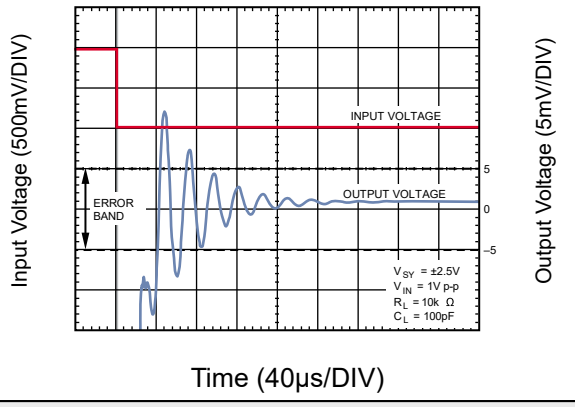


Figure 48: Negative Settling Time to 0.1%

7.9 Typical Characteristic

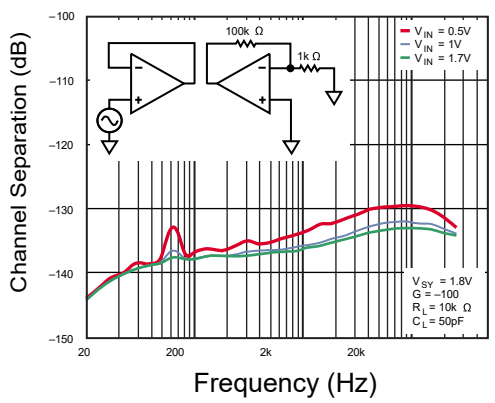


Figure 49: Channel Separation vs. Frequency

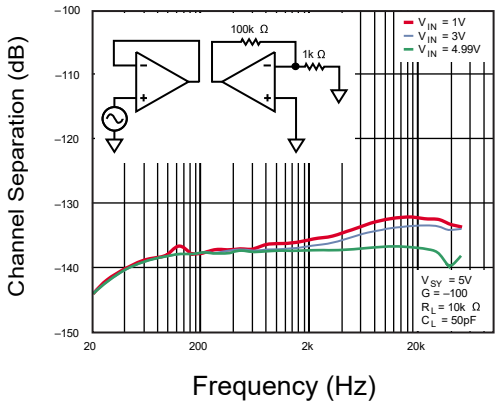


Figure 50: Channel Separation vs. Frequency

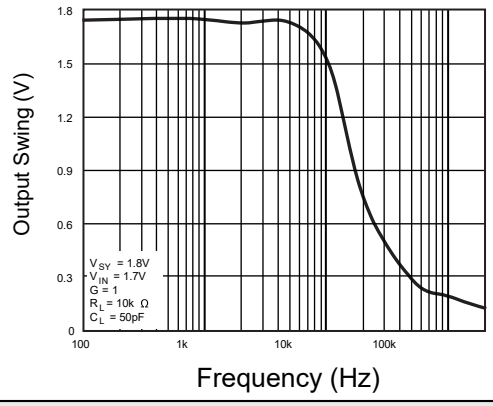


Figure 51: Output Swing vs. Frequency

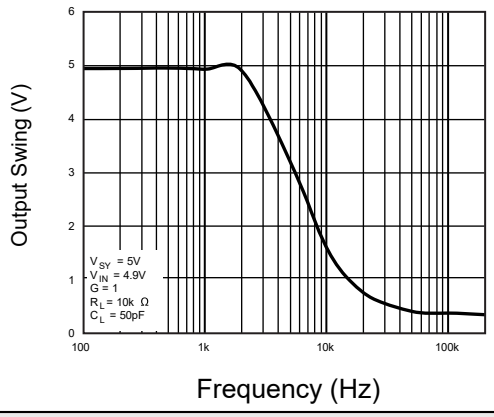


Figure 52: Output Swing vs. Frequency

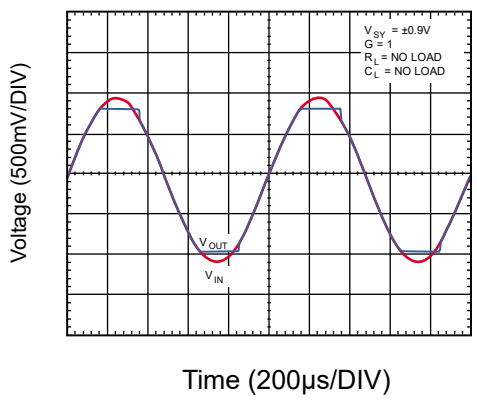


Figure 53: No Phase Reversal

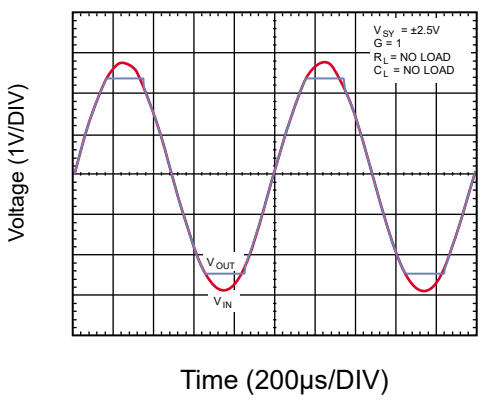
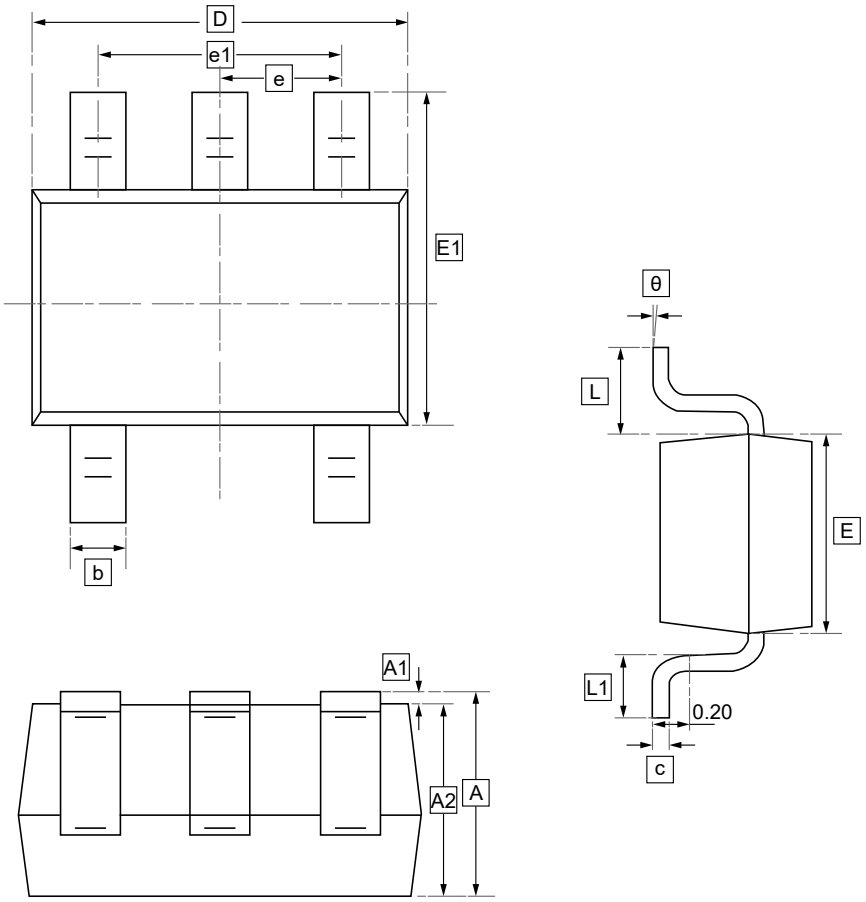


Figure 54: No Phase Reversal

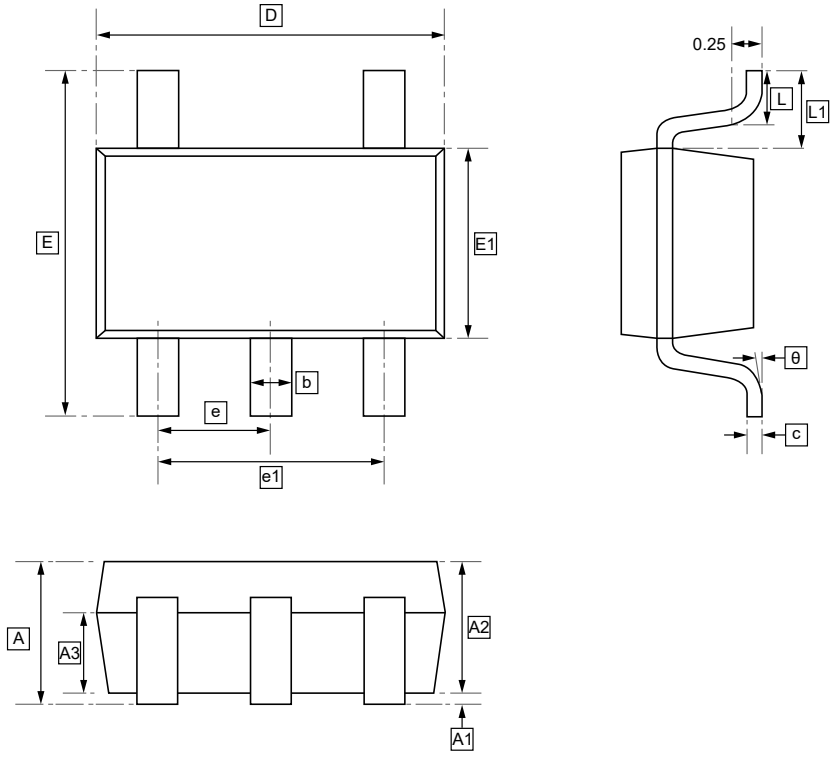
8.1 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	2.05	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

8.2 SOT-23-5 Package Outline Dimensions

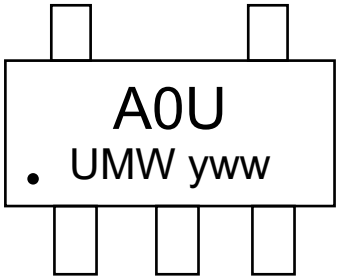


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	e1	L
Min	-	0.01	1.00	0.60	0.33	0.11	2.82	2.60	1.50	0.90	1.90	0.30
Max	1.25	0.08	1.20	0.70	0.41	0.20	3.02	3.00	1.70	1.00	BSC	0.60

Symbol	L1	θ
Min	0.55	0°
Max	0.75	8°

9.Ordering Information



yww: Batch Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW ADA4051-1AKSZ	A0U	SC70-5	3000	Tape and reel
UMW ADA4051-1ARJZ	A0U	SOT23-5	3000	Tape and reel

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