UMW RFD14N05LSM

60V N-Channel MOSFET

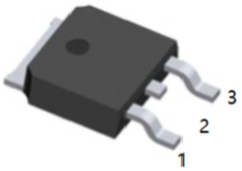
1.Features

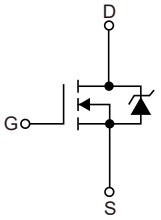
- $V_{DS\ (V)}$=60V
- $R_{DS(ON)}$<100mΩ(V_{GS}=5V)
- 175°C Operating Temperature
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve

2.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view





3.Absolute Maximum Ratings T_C= 25°C

Parameter	Symbol	Rating	Units
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS}= 20kΩ)(Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	14	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UiS Curve	
Power Dissipation	P_D	48	W
Derate above 25°C		0.32	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	°C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	°C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	°C

Notes

1. T_J=25°C to 150°C.

4.Electrical Characteristic (T_C=25°C unless otherwise noted)

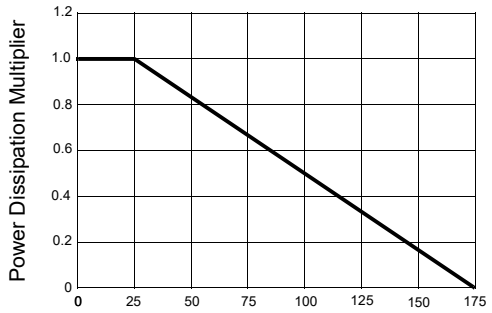
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA, Figure 13		60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA,Figure 12		1		2	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V				1	μA
		V_{DS}=40V, V_{GS}=0V, T_C=150°C				50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±10V				±100	nA
Drain to Source On Resistance (Note 2)	$R_{DS(ON)}$	V_{GS}=5V, I_D=14A, Figures 9,11				100	mΩ
Turn-On Time	$t_{(on)}$	V_{DD}=25V, I_D=7A R_L=3.57Ω, V_{GS}=5V R_{GS}=0.6Ω				60	ns
Turn-On Delay Time	$t_{D(on)}$				13		ns
Rise Time	t_r				24		ns
Turn-Off Delay Time	$t_{D(off)}$				42		ns
Fall Time	t_f				16		ns
Turn-Off Time	$t_{(off)}$					100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS}=0V to 10V	V_{DD}=40V, I_D=14A R_L=2.86Ω Figures 20, 21			40	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS}=0V to 5V				25	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS}=0V to 1V				1.5	nC
Input Capacitance	C_{iss}	V_{DS}=-25V, V_{GS}=0V, f=1MHz Figure 14			670		pF
Output Capacitance	C_{oss}				185		pF
Reverse Transfer Capacitance	C_{rss}				50		pF
Thermal Resistance Junction to Case	$R_{\theta JC}$					3.125	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-252				100	°C/W
Source to Drain Diode Specifications							
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD}=14A				1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD}=14A, dI_{SD}/dt=100A/μs				125	ns

Notes:

2. Pulse Test: Pulse Width ≤300ms, Duty Cycle ≤2%.

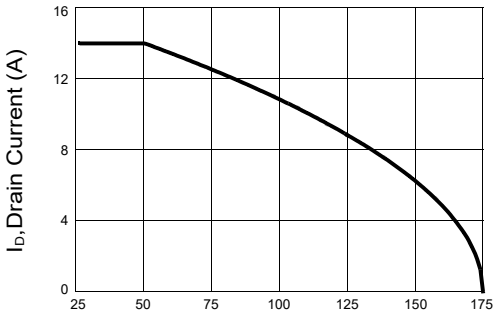
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

5.1Typical characteristic



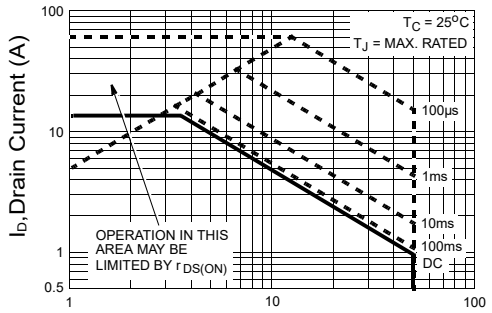
T_C,Case Temperature (°C)

Figure 1: Normalized Power Dissipation Vs Case Temperature



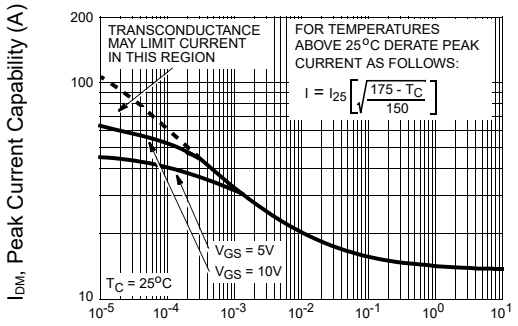
T_C,Case Temperature (°C)

Figure 2: Maximum Continuous Drain Current Vs Temperature



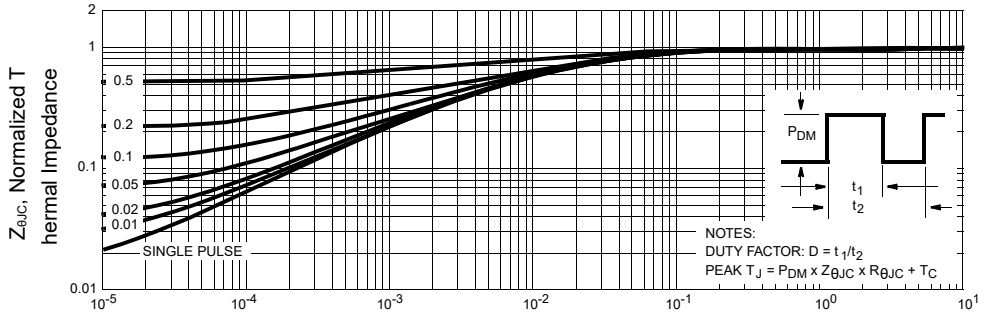
V_{DS},Drain-to-Source Voltage (V)

Figure 3: Forward Bias Safe Operating Area



t, Pulse Width (s)

Figure 4: Peak Current Capability



t, Rectangular Pulse Duration (s)

Figure 5: Normalized Maximum Transient Thermal Impedance

5.2Typical characteristic

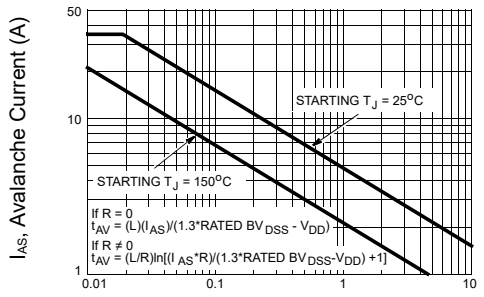


Figure 6: Unclamped Inductive Switching

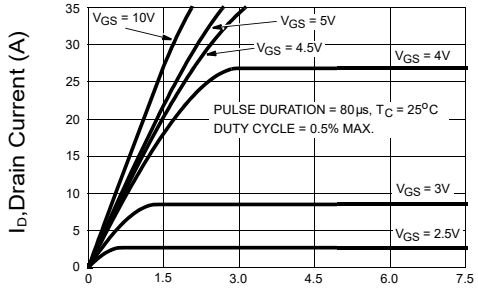


Figure 7: Saturation Characteristics

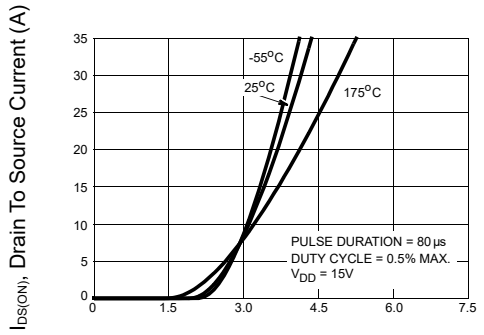


Figure 8: Transfer Characteristics

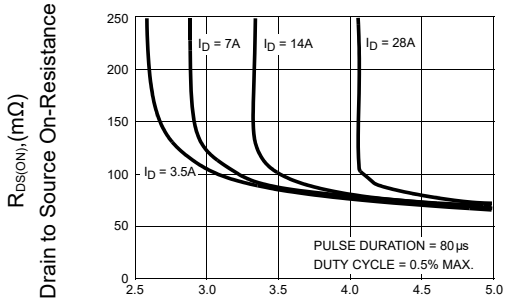


Figure 9: Drain To Source On Resistance Vs Gate Voltage And Drain Current

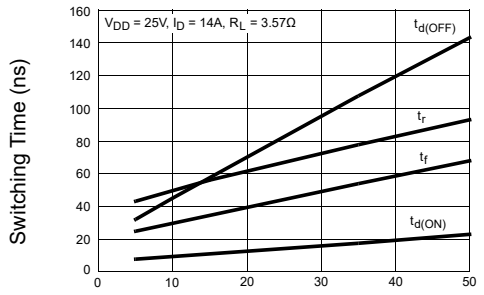


Figure 10: Switching Time Vs Gate Resistance

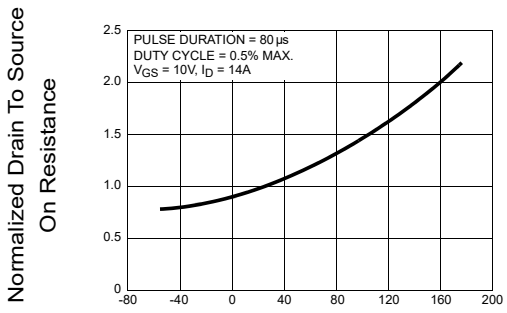


Figure 11: Normalized Drain To Source On Resistance Vs Junction Temperature

5.3Typical characteristic

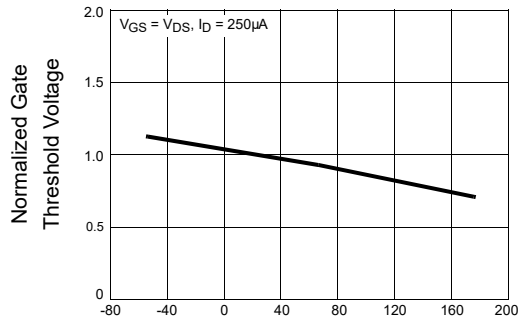


Figure 12: Normalized Gate Threshold Voltage Vs Junction Temperature

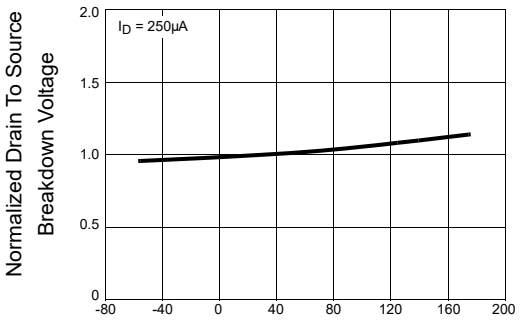


Figure 13: Normalized Drain To Source Breakdown Voltage Vs Junction Temperature

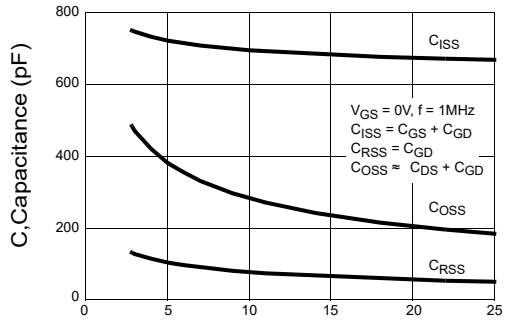


Figure 14: Capacitance Vs Drain To Source Voltage

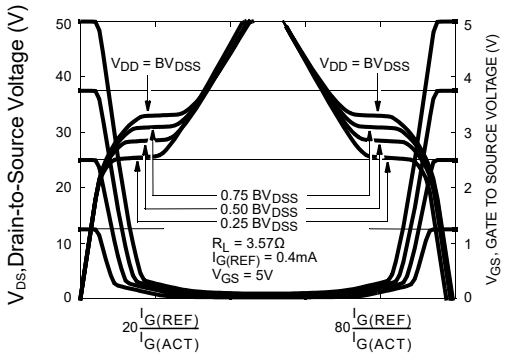


Figure 15: Transconductance Vs Drain Current

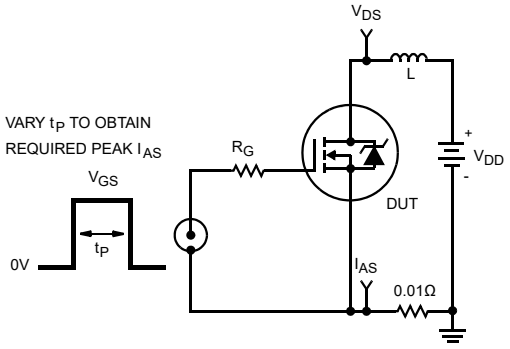


Figure 16: Unclamped Energy Test Circuit

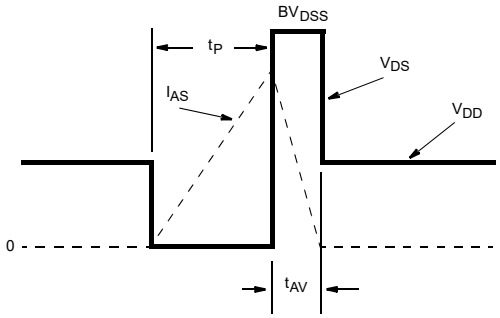


Figure 17: Unclamped Energy Waveforms

6.Test Circuits and Waveforms

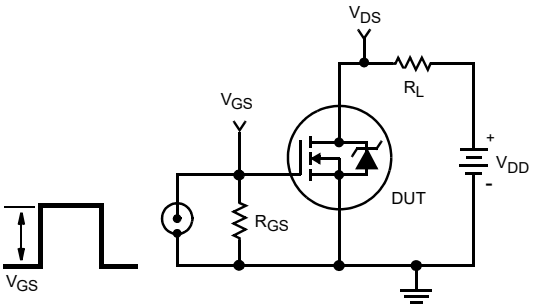


Figure 18: Switching Time Test Circuit

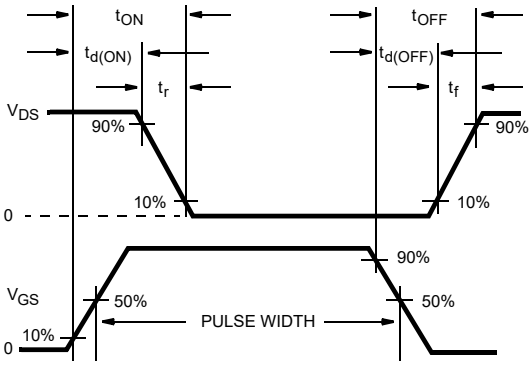


Figure 19: Resistive Switching Waveforms

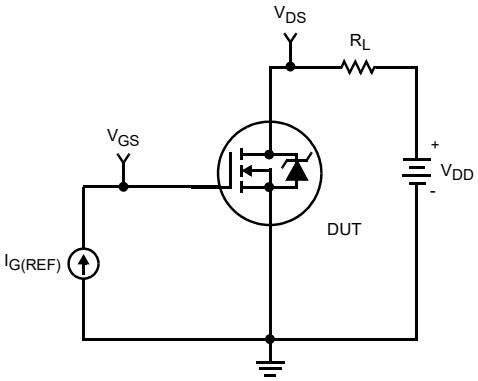


Figure 20: Gate Charge Test Circuit

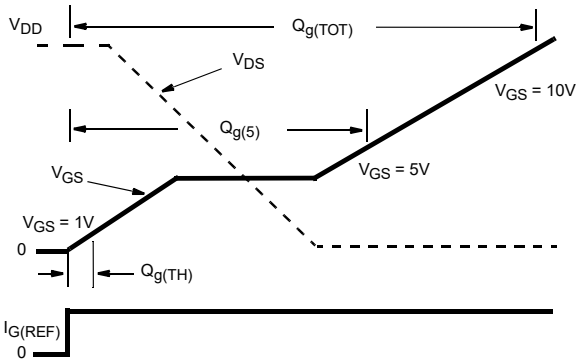
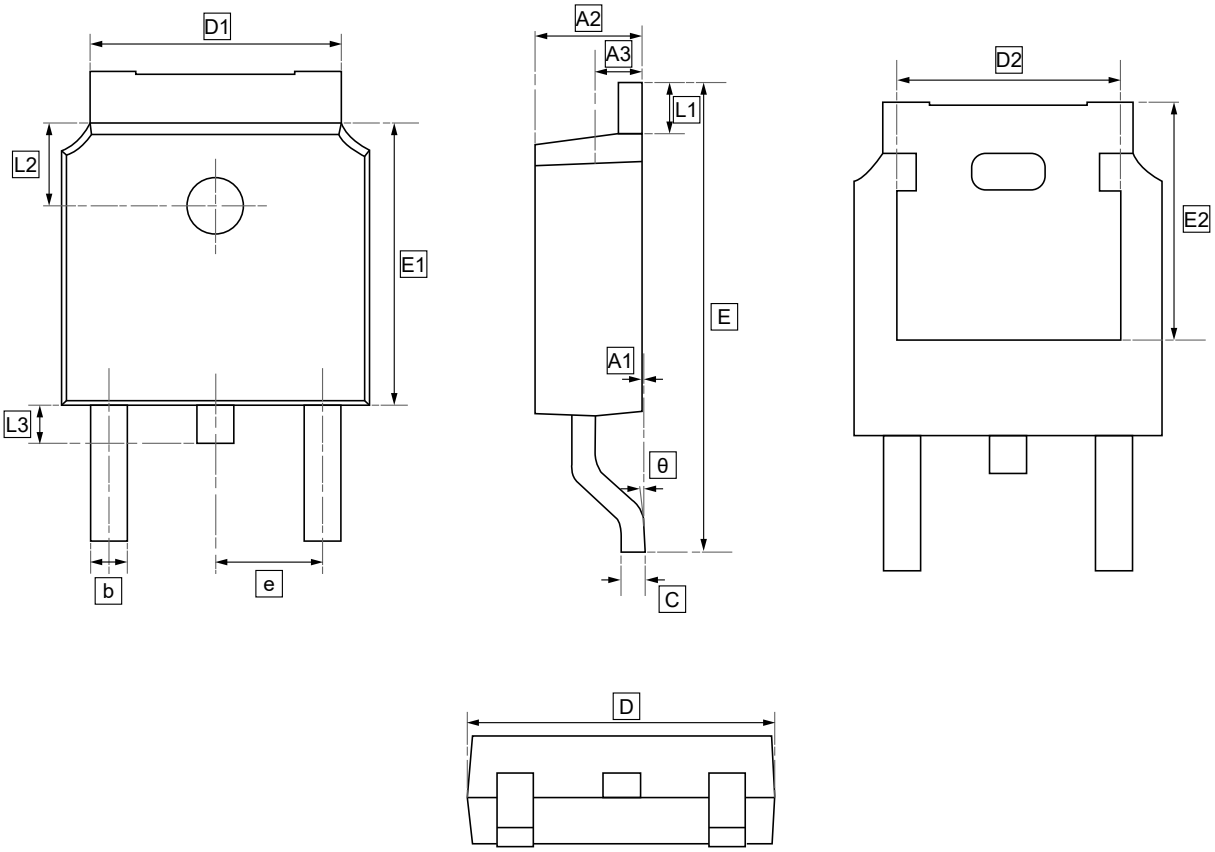


Figure 21: Gate Charge Waveforms

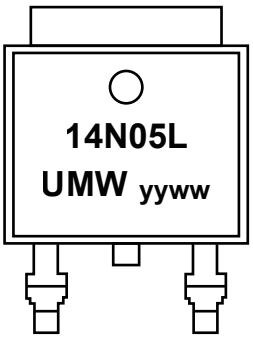
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW RFD14N05LSM	TO-252	2500	Tape and reel

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