

1. Description

This P-Channel MOSFET has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 25V).

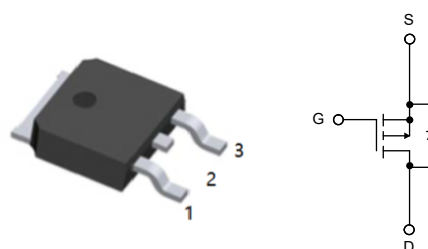
2. Features

- $V_{DS(V)} = -30V$
- $I_D = -40A$
- $R_{DS(ON)} < 14m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 21m\Omega (V_{GS} = -2.5V)$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

3. Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view



4. Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter			Symbol	Rating	Units
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	± 25	
Continuous Drain Current	@ $T_C = 25^\circ C$	(Note 3)	I_D	-40	A
	@ $T_A = 25^\circ C$	(Note 1a)		-11	
	Pulsed	(Note 1a)		-100	
Power Dissipation	@ $T_C = 25^\circ C$	(Note 3)	P_D	52	W
	@ $T_A = 25^\circ C$	(Note 1a)		3.8	
	@ $T_A = 25^\circ C$	(Note 1b)		1.6	
Operating and Storage Junction Temperature Range			T_J, T_{STG}	-55 to 175	$^\circ C$



5. Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	2.9	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1b)	$R_{\theta JA}$	96	°C/W



6. Electrical Characteristic ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 4)						
Single Pulse Drain-Source Avalanche Energy	E_{AS}	$I_D=-11\text{A}$		42		mJ
Maximum Drain-Source Avalanche Current	I_{AS}			-11		A
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=-250\mu\text{A}$ Referenced to 25°C		-24		mV/ $^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24\text{V}, V_{GS}=0\text{V}$			-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 25\text{V}, V_{DS}=0\text{V}$			± 100	nA
On Characteristics (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1	-1.8	-3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	$I_D=-250\mu\text{A}$ Referenced to 25°C		5		mV/ $^{\circ}\text{C}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10\text{V}, I_D=-11\text{A}$		14	20	m Ω
		$V_{GS}=-4.5\text{V}, I_D=-9\text{A}$		21	30	m Ω
On-State Drain Current	$I_{D(on)}$	$V_{GS}=-10\text{V}, V_{DS}=-5\text{V}$	-20			A
Forward Transconductance	g_{FS}	$V_{DS}=-5\text{V}, I_D=-11\text{A}$		26		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=-15\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		1715		pF
Output Capacitance	C_{oss}			440		pF
Reverse Transfer Capacitance	C_{rss}			225		pF
Gate Resistance	R_g	$V_{GS}=15\text{mV}, f=1\text{MHz}$		3.6		Ω

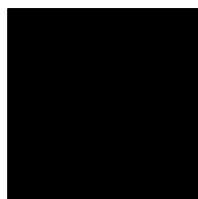


Switching Characteristics (Note 2)						
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=-15V, I_D=-1A$ $V_{GS}=-10V, R_{GEN}=6\Omega$		17	31	ns
Turn-On Rise Time	t_r			11	21	ns
Turn-Off Delay Time	$t_{D(off)}$			43	68	ns
Turn-Off Fall Time	t_f			21	34	ns
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-11A$ $V_{GS}=-5V$		17	24	nC
Gate-Source Charge	Q_{gs}			9		nC
Gate-Drain Charge	Q_{gd}			4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
Drain–Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-3.2A$ (Note 2)		-0.8	-1.2	V
Diode Reverse Recovery Time	t_{rr}	$I_F=-11A$		26		ns
Diode Reverse Recovery Charge	Q_{rr}	$diF/dt = 100A/\mu s$		13		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}=40^{\circ}C/W$ when mounted
on a 1in² pad of 2oz copper.



b) $R_{\theta JA}= 96^{\circ}C/W$ when mounted
on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at $T_C=25^{\circ}C$ and $R_{DS(ON)}$ is at $T_{J(max)}$ and $V_{GS}=10V$.

4. Starting $T_J=25^{\circ}C$, $L=0.69mH$, $I_{AS}=-11A$.



7.1 Typical characteristic

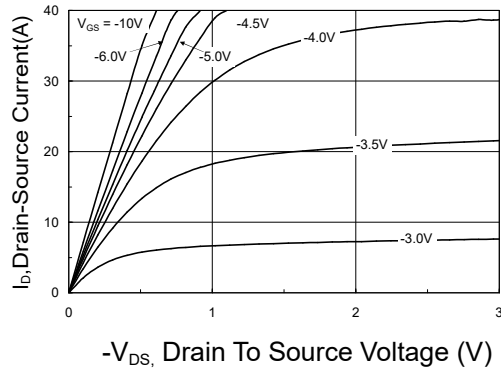


Figure 1: On-Region Characteristics

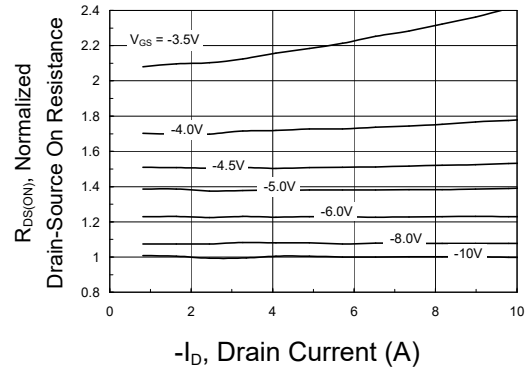


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage

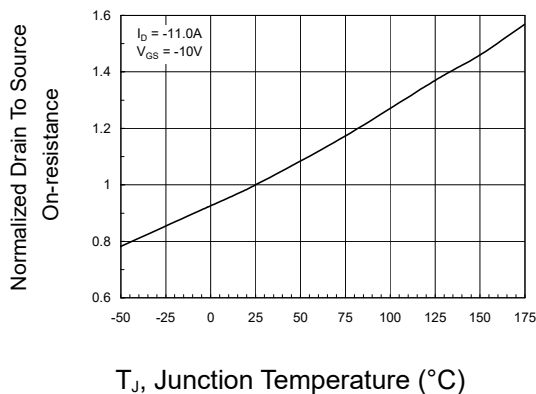


Figure 3: On-Resistance Variation with Temperature

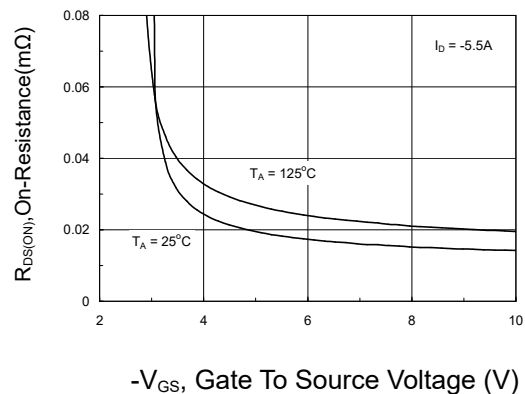


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

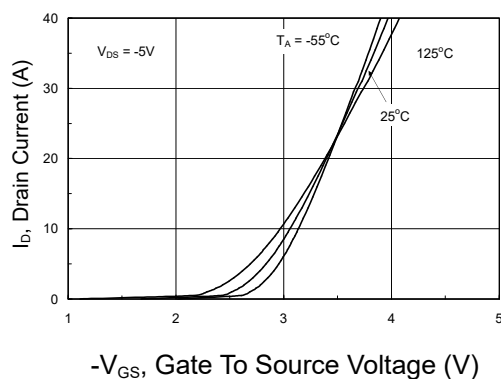


Figure 5: Transfer Characteristics

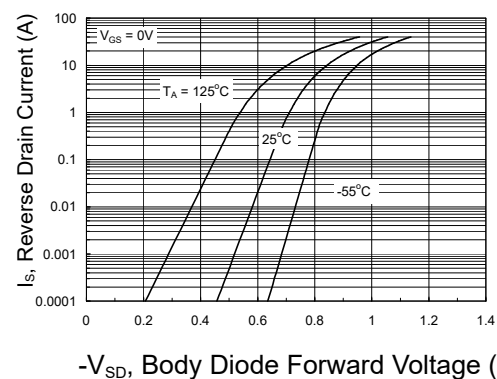


Figure 6: Body Diode Forward Voltage Variation with Source Current and Temperature



7.2 Typical characteristic

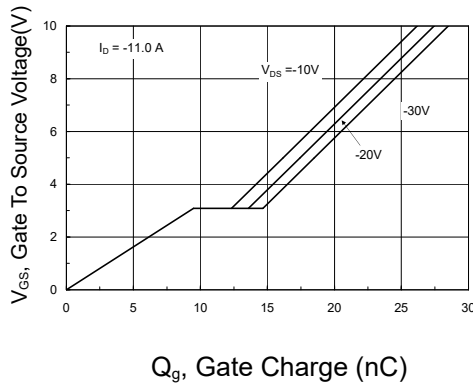


Figure 7: Gate Charge Characteristics

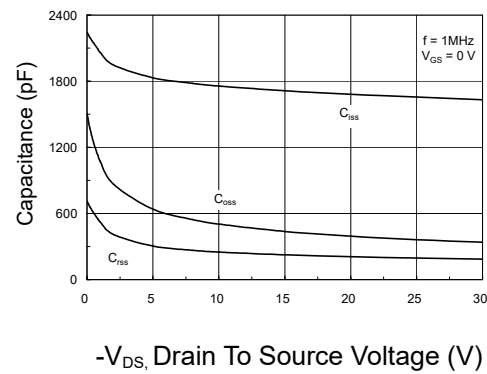


Figure 8: Capacitance Characteristics

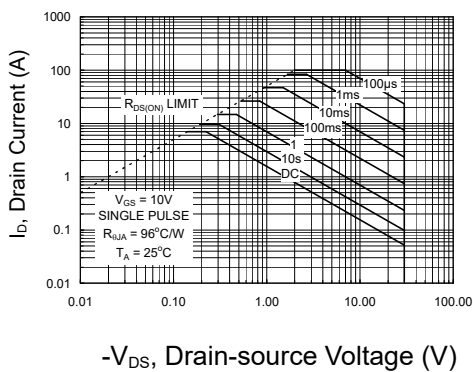


Figure 9: Maximum Safe Operating Area

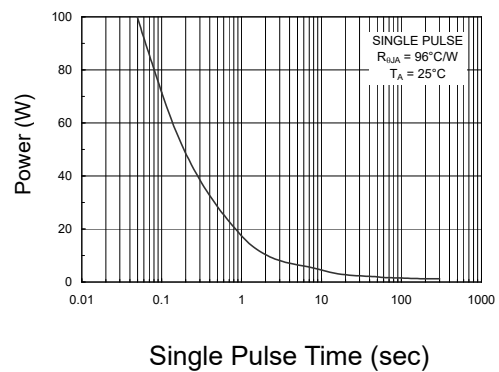


Figure 10: Single Pulse Maximum Power Dissipation

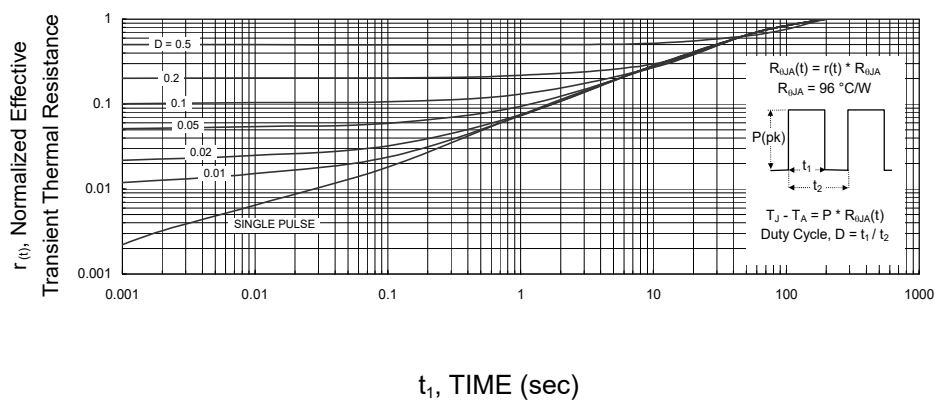
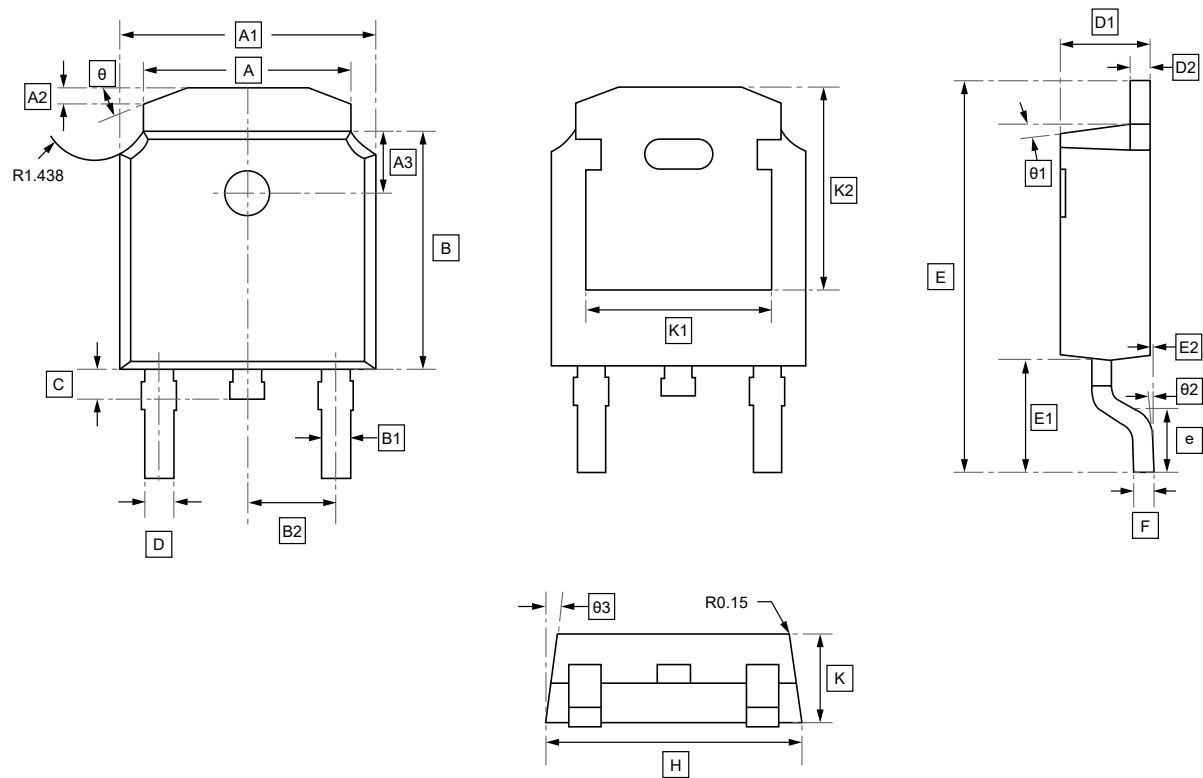


Figure 11: Transient Thermal Response Curve



8.TO-252 Package Outline Dimensions



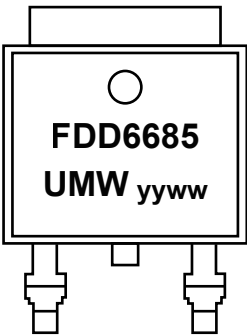
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	B2	C	D	D1	D2	E
Min	5.20	6.50	0.40	1.40	6.00	0.740	2.286	0.60	0.74	2.15	0.50	9.80
Max	5.46	6.70	(typ)	1.80	6.20	0.940	(typ)	1.0	0.86	2.45	(typ)	10.40

Symbol	E1	E2	e	F	H	K	K1	K2	θ	θ1	θ2	θ3
Min	2.60	0.00	1.65	0.50	6.50	2.15	4.63	5.10	20°	7°	0°	7°
Max	3.20	0.127	(typ)	0.60	6.70	2.45	5.03	5.50	(typ)	(typ)	8°	(typ)



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD6685	TO-252	2500	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.