

1.Description

Power SOT-223 P-Channel enhancement mode power field effect transistors especially tailored to minimize on state resistance and provide superior switching performance.

2.2Features

- High power and current handling capability in a widely used surface mount package.

2.1Features

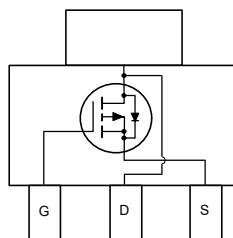
- $V_{DS(V)} = -30V$
- $I_D = -7.5A$
- $R_{DS(ON)} < 25m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 30m\Omega (V_{GS} = -4.5V)$

- High density cell design for extremely low $R_{DS(ON)}$

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

SOT-223
top view



4.Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	-30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current - Continuous (Note 1a)	I_D	-7.5	A
-Pulsed		± 20	A
Power Dissipation for Single Operation (Note 1a)	P_D	3	W
(Note 1b)		1.3	W
(Note 1c)		1.1	W
Storage Temperature Range	T_J, T_{STG}	-65 to 150	$^\circ C$



5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	42	°C/W
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	12	°C/W



6. Electrical Characteristic ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$			-1	μA
		$T_J=55^{\circ}\text{C}$			-10	μA
Gate - Body Leakage, Forward	I_{GSSF}	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$			100	nA
Gate - Body Leakage, Reverse	I_{GSSR}	$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1	-1.5	-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10\text{V}$, $I_D=-7.5\text{A}$		15	25	$\text{m}\Omega$
		$V_{DS}=-4.5\text{V}$, $I_D=-6\text{A}$		19	30	$\text{m}\Omega$
On-State Drain Current	$I_{D(on)}$	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-20			A
		$V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$	-10			A
Forward Transconductance	G_{fs}	$V_{DS}=-10\text{V}$, $I_D=-7.5\text{A}$		13		S
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		1440		pF
Output Capacitance	C_{oss}			905		pF
Reverse Transfer Capacitance	C_{rss}			355		pF
Turn-On DelayTime	$t_{D(on)}$	$V_{DD}=-15\text{V}$, $I_D=-7\text{A}$ $V_{GEN}=-10\text{V}$, $R_{GEN}=12\Omega$		10	20	ns
Turn-On Rise Time	t_r			65	120	ns
Turn-Off DelayTime	$t_{D(off)}$			70	130	ns
Turn-Off Fall Time	t_f			70	130	ns
Total Gate Charge	Q_g	$V_{GS}=-10\text{V}$, $V_{DS}=-10\text{V}$ $I_D=-7.5\text{A}$		47	67	nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			12		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-2.5	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=-2.5\text{A}$ (Note 2)		-0.85	-1.2	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0\text{V}$, $I_F=-2.5\text{A}$, $dI_F/dt=100\text{A}/\mu\text{s}$			140	ns



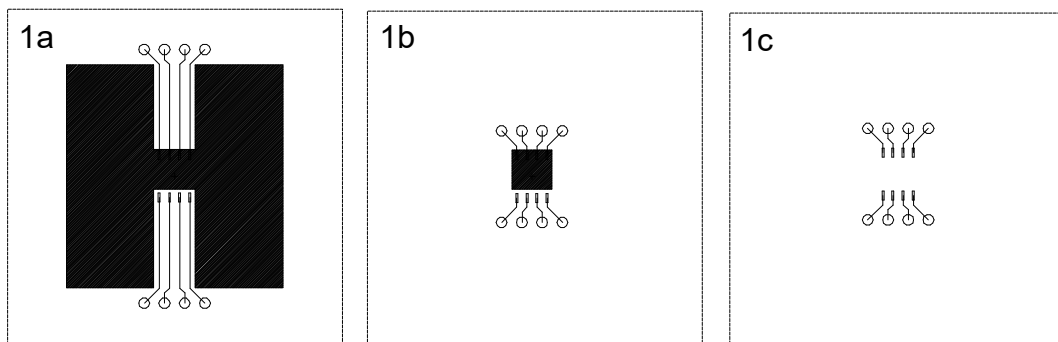
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is defined by users.

For general reference: Applications on 4.5"x5" FR-4 PCB under still air environment, typical $R_{\theta JA}$ is found to be:

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA(t)}} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA(t)}} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

- a. 42°C/W when mounted on a 1 in² pad of 2oz copper.
- b. 95°C/W when mounted on a 0.066in² pad of 2oz copper.
- c. 110°C/W when mounted on a 0.00123 in² pad of 2oz copper.

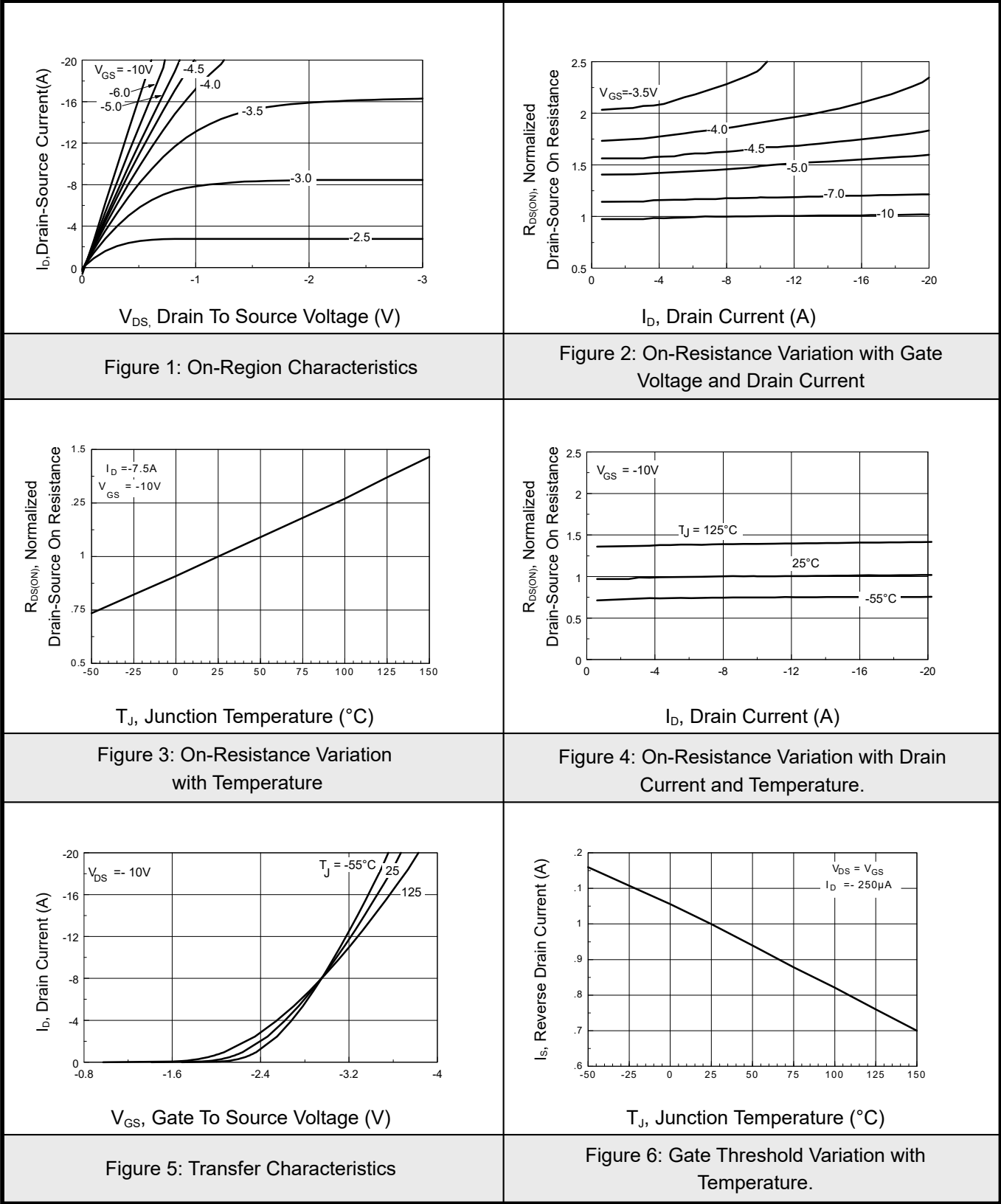


Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.



7.1Typical characteristic





7.2 Typical characteristic

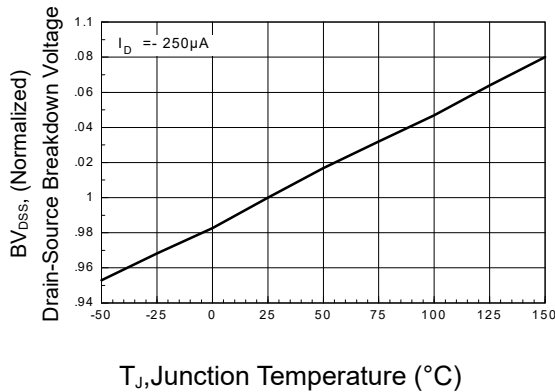


Figure 7: Breakdown Voltage Variation with Temperature

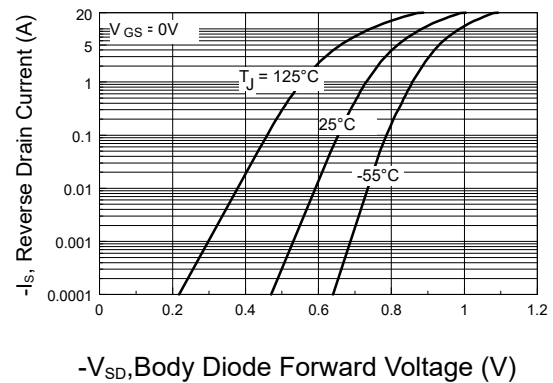


Figure 8: Body Diode Forward Voltage Variation with Current and Temperature

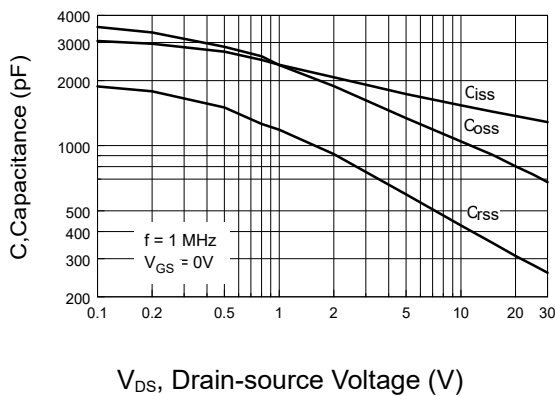


Figure 9: Capacitance Characteristics

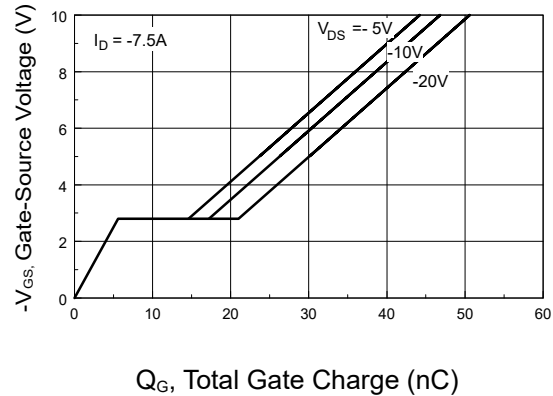


Figure 10: Gate Charge Characteristics

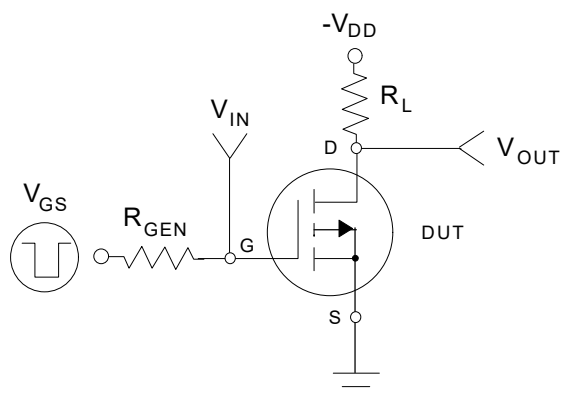


Figure 11: Switching Test Circuit

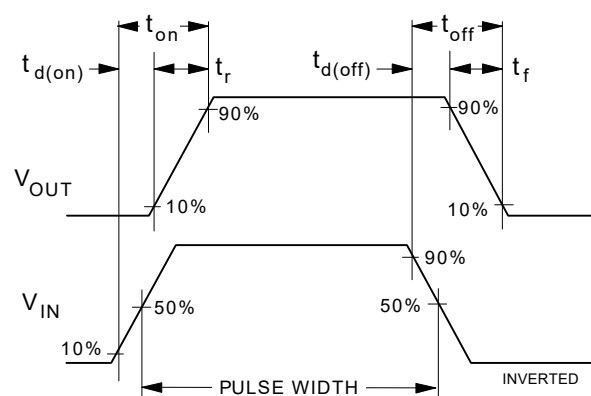


Figure 12: Switching Waveforms



7.3 Typical characteristic

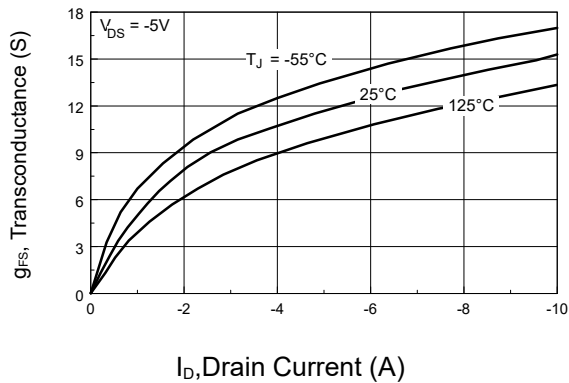


Figure 13: Transconductance Variation with Drain Current and Temperature

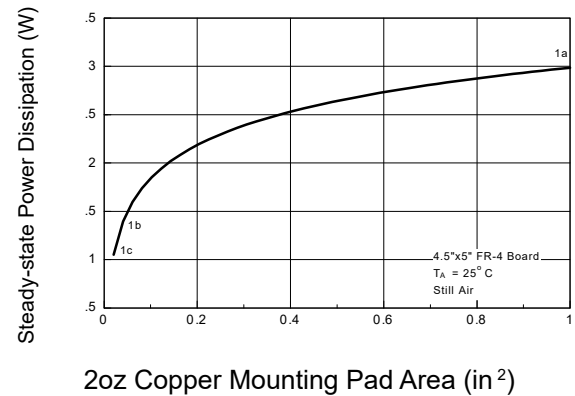


Figure 14: SOT-223 Maximum Steady-state Power Dissipation versus Copper Mounting Pad Area

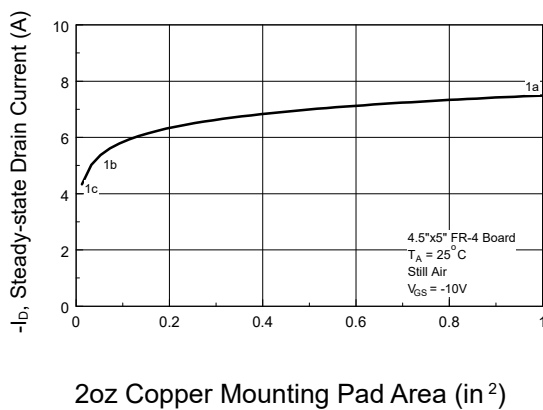


Figure 15: Maximum Steady-State Drain Current versus Copper Mounting Pad Area

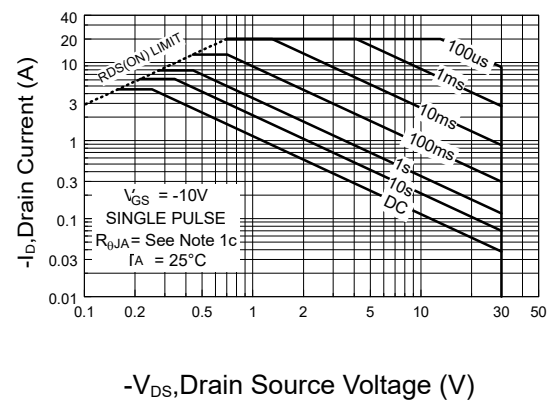


Figure 16: Maximum Safe Operating Area

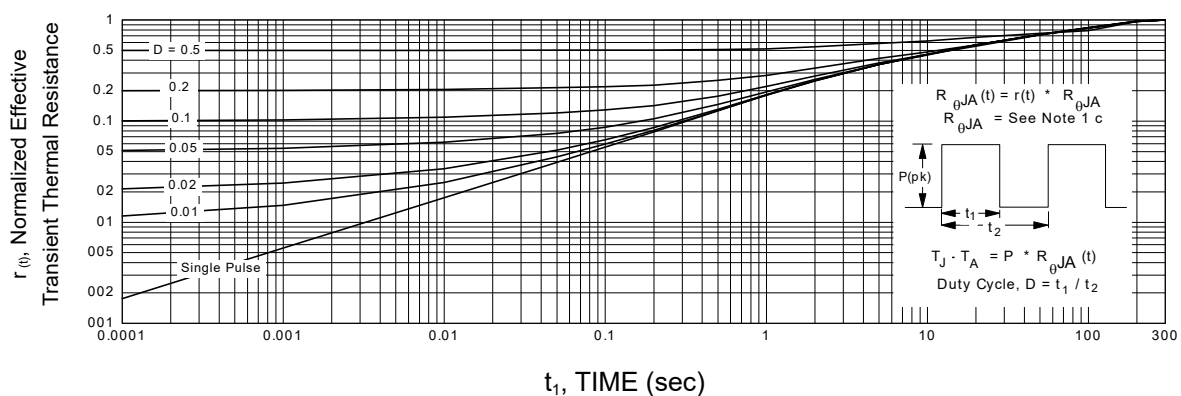
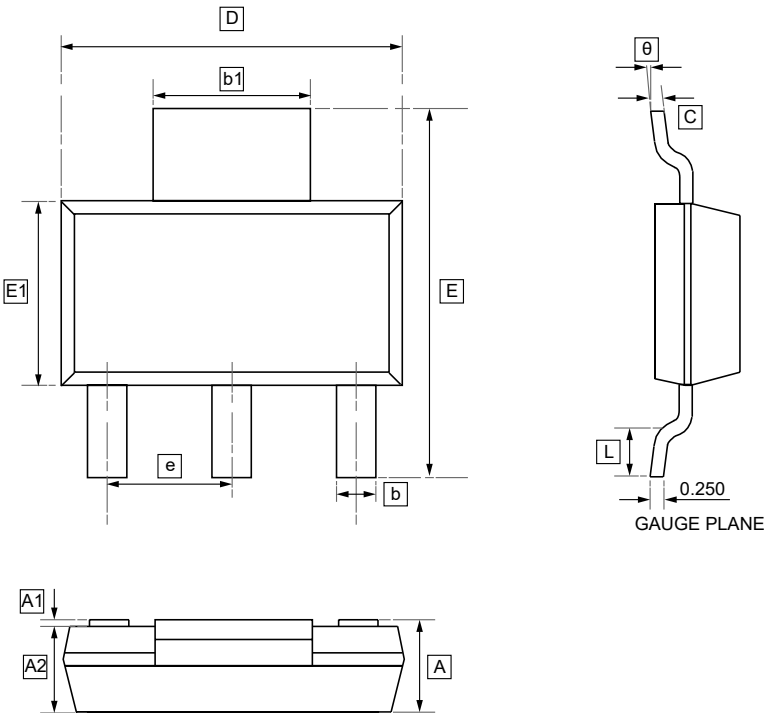


Figure 17: Transient Thermal Response Curve



8.SOT-223 Package Outline Dimensions

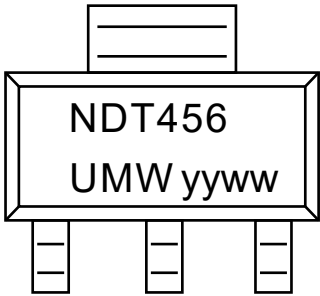


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	D	E	E1	e	L	θ
Min	-	0.020	1.500	0.660	2.900	0.230	6.300	6.700	3.300	2.300	0.750	0°
Max	1.800	0.100	1.700	0.840	3.100	0.350	6.700	7.300	3.700	BSC	-	10°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NDT456P	SOT-223	2500	Tape and reel



10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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