

1.Features

- $V_{DS(V)}=20V$
- $I_D=8.7A$
- $R_{DS(ON)}<22m\Omega(V_{GS}=4.5V)$
- RoHS Compliant, Halogen-Free
- Compatible with Existing Surface Mount Techniques

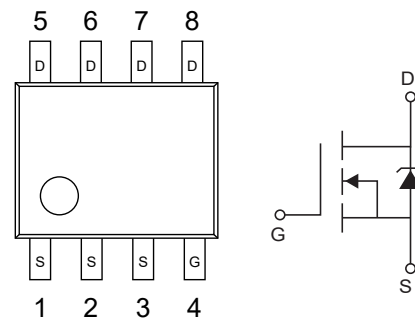
2.Benefits

- Multi-Vendor Compatibility
- Easier Manufacturing
- Environmentally
- Increased Reliability

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter		Symbol	Rating	Units
10 Sec. Pulsed Drain Current, $V_{GS}=4.5V$	$T_A=25^{\circ}C$	I_D	10	A
Continuous Drain Current, $V_{GS}=4.5V$	$T_A=25^{\circ}C$		8.7	A
Continuous Drain Current, $V_{GS}=4.5V$	$T_A=70^{\circ}C$		7	A
Pulsed Drain Current ①		I_{DM}	35	A
Power Dissipation	$T_A=25^{\circ}C$	P_D	2.5	W
Linear Derating Factor			0.02	W/ $^{\circ}C$
Gate-to-Source Voltage		V_{GS}	± 12	V
Peak Diode Recovery dv/dt ②		dv/dt	5	V/nS
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}C$

5.Thermal Resistance Rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		62.5	$^{\circ}C/W$



6. Electrical Characteristics $T_J=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	$I_D=1\text{mA}$, Reference to 25°C		0.044		$\text{V}/^{\circ}\text{C}$
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=4.5\text{V}$, $I_D=4.1\text{A}$ ③			22	m Ω
		$V_{GS}=2.7\text{V}$, $I_D=3.5\text{A}$ ③			30	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.7			V
Forward Transconductance	g_{FS}	$V_{DS}=15\text{V}$, $I_D=4.1\text{A}$	11			S
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$			1	μA
		$V_{DS}=16\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^{\circ}\text{C}$			25	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS}=12\text{V}$			100	nA
Gate-to-Source Reverse Leakage		$V_{GS}=-12\text{V}$			-100	
Total Gate Charge	Q_g	$I_D=4.1\text{A}$			48	nC
Gate-to-Source Charge	Q_{gs}	$V_{DS}=16\text{V}$, $V_{GS}=4.5\text{V}$			5.1	
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig. 6 and 12 ③			20	
Turn-On Delay Time	$t_{D(on)}$	$V_{DD}=10\text{V}$		13		ns
Rise Time	t_r	$I_D=4.1\text{A}$		72		ns
Turn-Off Delay Time	$t_{D(off)}$	$R_G=6\Omega$		65		ns
Internal Drain inductance	L_D	$R_D=2.4\Omega$, See Fig. 10 ③		2.5		ns
Fall Time	t_f	Between lead tip and center of die contact		92		nH
Internal Source inductance	L_S			4		
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}$		1600		pF
Output Capacitance	C_{oss}	$V_{DS}=15\text{V}$		690		pF
Reverse Transfer Capacitance	C_{rss}	$f=1.0\text{MHz}$, See Fig.		310		pF



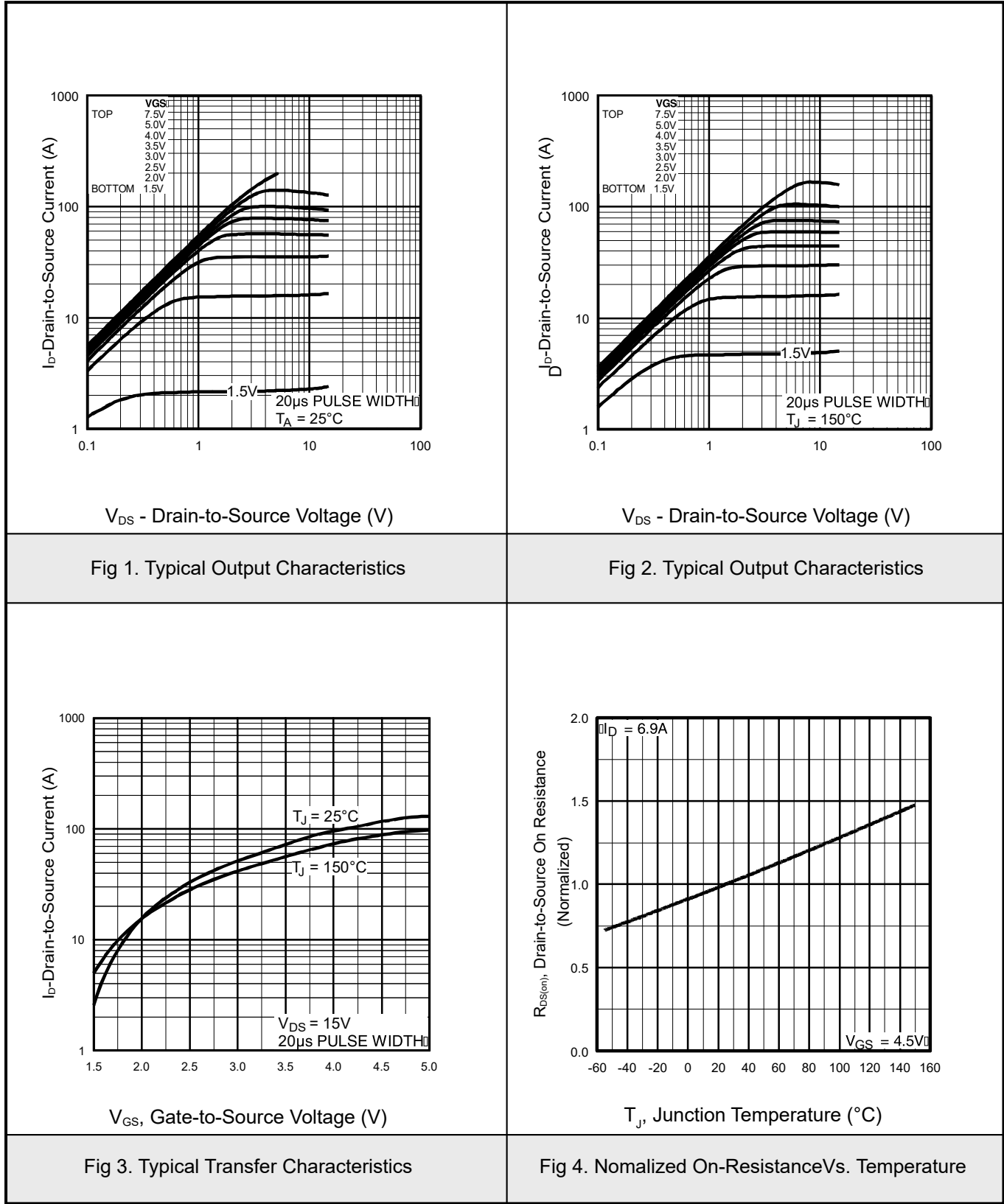
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			3.1	A
Pulsed Source Current (Body Diode) ①	I_{SM}				35	
Diode Forward Voltage	V_{SD}	$T_J=25^{\circ}\text{C}, I_S=2\text{A}, V_{GS}=0\text{V}$ ③			1	V
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, I_F=4.1\text{A}$		39	59	ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$ ③		42	63	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max.junction temperature.(See fig.11)
- ② $I_{SD} \leq 4.1\text{A}$, $di/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^{\circ}\text{C}$.
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

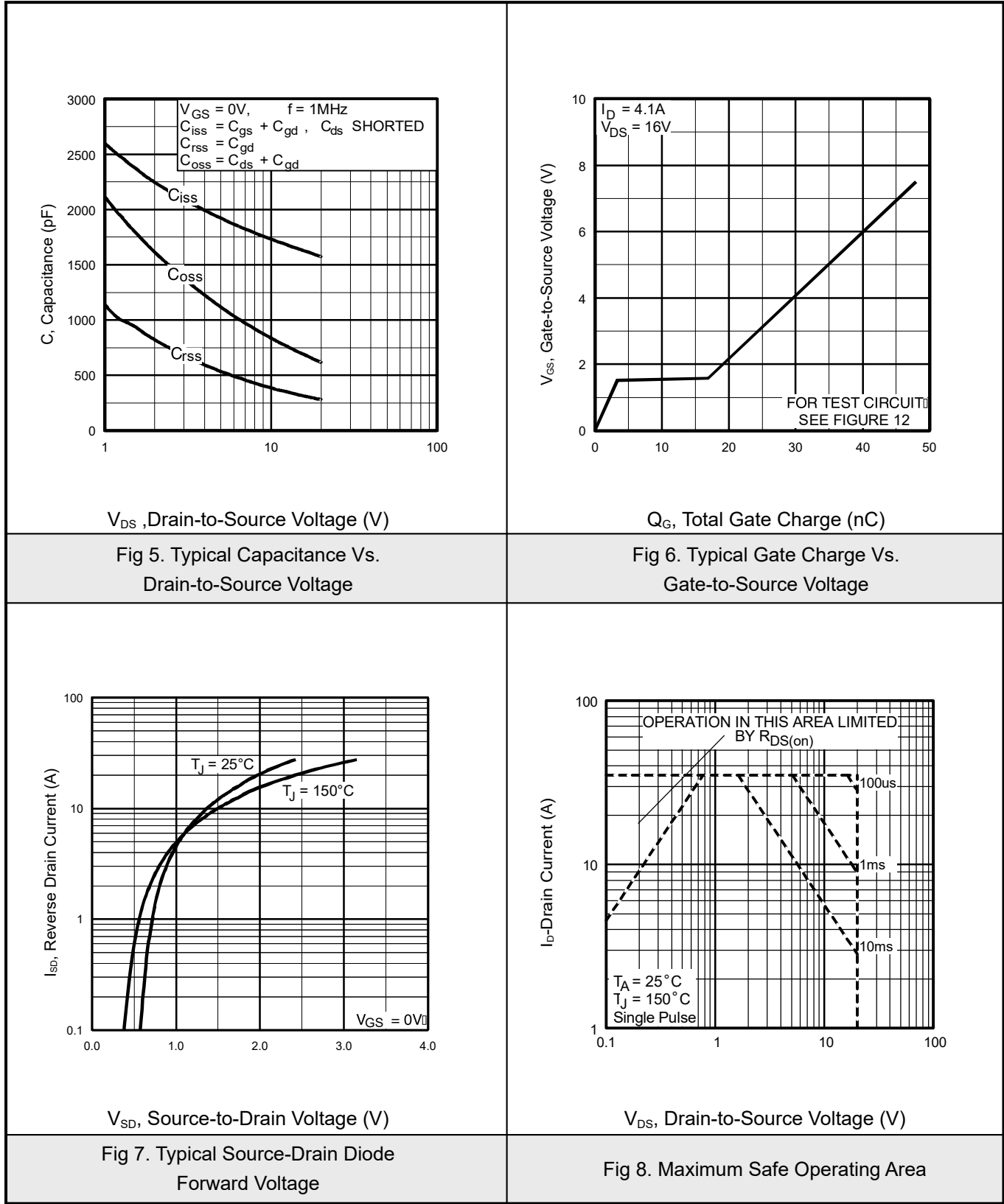


7.1Typical Characterisitics





7.2Typical Characteristics





7.3Typical Characterisitics

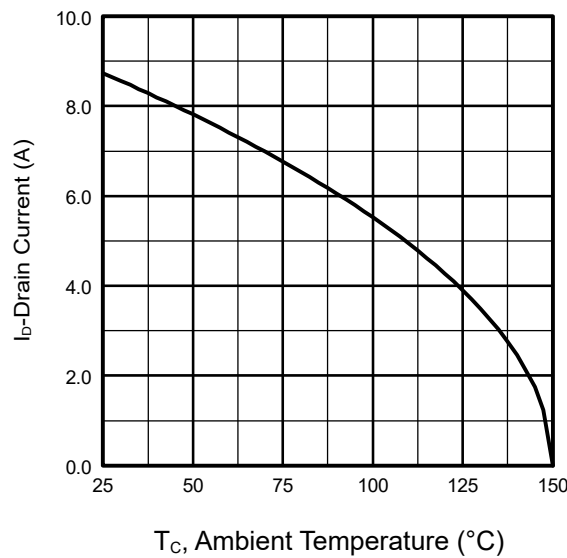


Fig 9. Maximum Drain Current Vs.AmbientTemperature

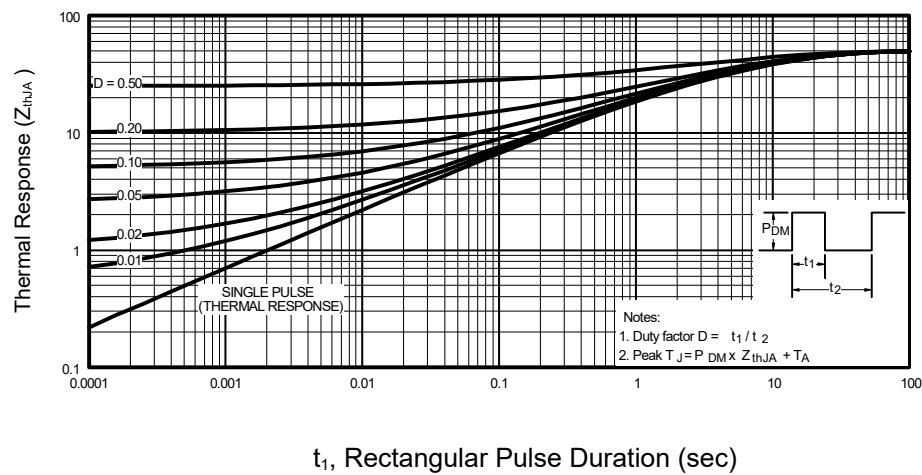


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



7.4 Typical Characteristics

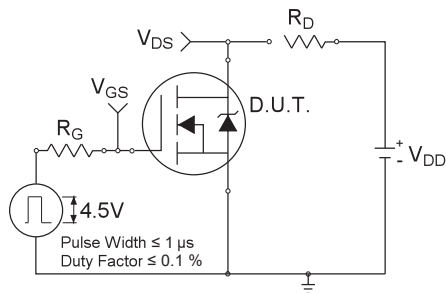


Fig 11a. Switching Time Test Circuit

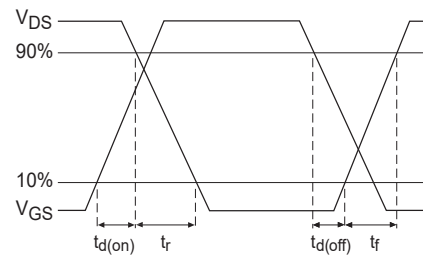


Fig 11b. Switching Time Waveforms

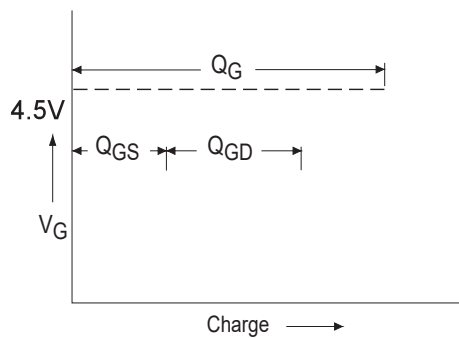


Fig 12a. Basic Gate Charge Waveform

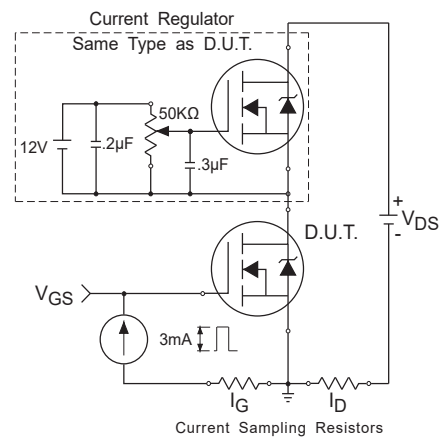
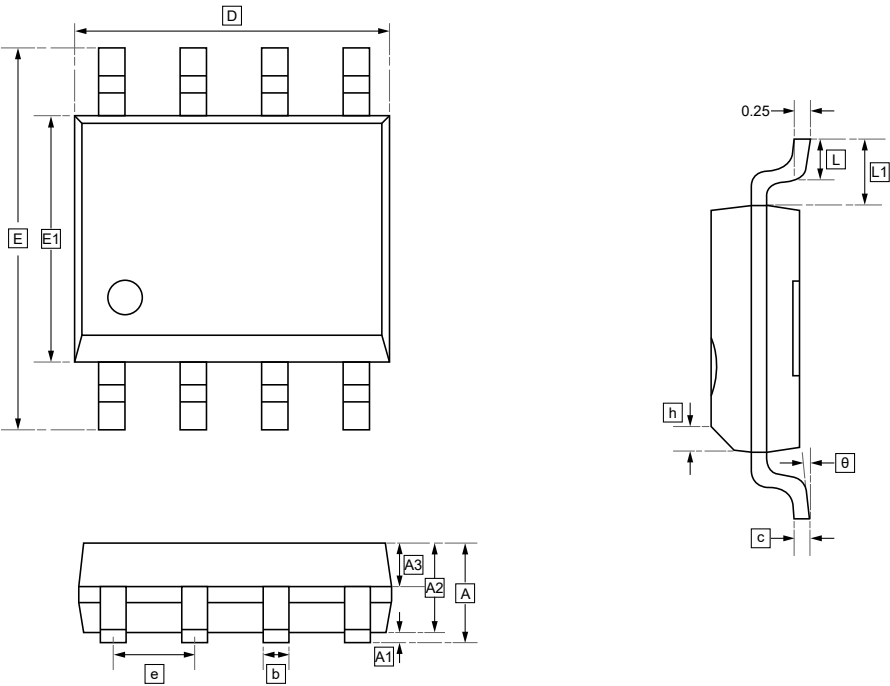


Fig 12b. Gate Charge Test Circuit



8.SOP-8 Package Outline Dimensions



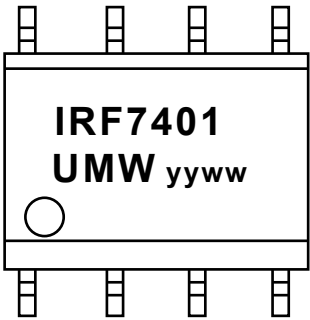
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7401TR	SOP-8	3000	Tape and reel



10.Disclaimer

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