

1.Features

- $V_{DSS} = -30V$
- $R_{DS(ON)} < 11.6m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 18m\Omega (V_{GS} = -4.5V)$
- RoHS Compliant
- High performance trench technology
- for extremely low $R_{DS(ON)}$

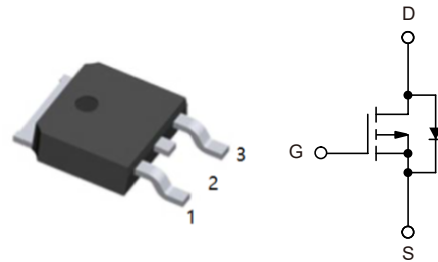
2.Applications

- Inverter
- Power Supplies

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view



4.Absolute Maximum Ratings $T_A = 25^\circ C$

Parameter			Symbol	Rating	Units
Drain-Source Voltage			V _{DSS}	-30	V
Drain-Source Avalanche Voltage (maximum)		(Note 4)	V _{DS(Avalanche)}	-40	
Gate-Source Voltage			V _{GSS}	±25	
Continuous Drain Current	@T _C =25°C	(Note 3)	I _D	-55	A
	@T _A =25°C	(Note 1a)		-13	
	Pulsed	(Note 1a)		-100	
Power Dissipation	@T _C =25°C	(Note 3)	P _D	57	W
	@T _A =25°C	(Note 1a)		3.1	
	@T _A =25°C	(Note 1b)		1.3	
Operating and Storage Junction Temperature Range			T _J , T _{STG}	-55 to 150	°C



5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1b)	$R_{\theta JA}$	96	°C/W



6. Electrical Characteristic ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Energy (Single Pulse)	E_{AS}	$V_{DD}=-35\text{V}$, $I_D=-11\text{A}$, $L=1\text{mH}$		61		mJ
Drain-Source Avalanche Current	I_{AS}			-14		A
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-28\text{V}$, $V_{GS}=0\text{V}$			-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 25\text{V}$, $V_{DS}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1	-16	-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10\text{V}$, $I_D=-14\text{A}$		9.7	11.6	m Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-11\text{A}$		14.4	18	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5\text{V}$, $I_D=-14\text{A}$		35		S
Input Capacitance	C_{iss}	$V_{DS}=-20\text{V}$, $V_{GS}=0\text{V}$ $f=1\text{MHz}$		2370		pF
Output Capacitance	C_{oss}			470		pF
Reverse Transfer Capacitance	C_{rss}			250		pF
Gate Resistance	R_g	$f=1\text{MHz}$		3.6		Ω
Turn-On DelayTime	$t_{D(on)}$	$V_{DD}=-20\text{V}$, $I_D=-1\text{A}$ $V_{GS}=-10\text{V}$, $R_{GEN}=6\Omega$		18	32	ns
Turn-On Rise Time	t_r			10	20	ns
Turn-Off DelayTime	$t_{D(off)}$			62	100	ns
Turn-Off Fall Time	t_f			36	58	ns
Total Gate Charge, $V_{GS} = -10\text{V}$	Q_g	$V_{DS}=-20\text{V}$, $I_D=-14\text{A}$		45	63	nC
Total Gate Charge, $V_{GS} = -5\text{V}$	Q_g			25	35	nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			10		nC
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=-14\text{A}$ (Note 2)		-0.8	-1.2	V
Diode Reverse Recovery Time	t_{rr}	$I_F=-14\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		28		ns
Diode Reverse Recovery Charge	Q_{rr}			15		nC



Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



■ a) $R_{\theta JA}=40^{\circ}\text{C/W}$ when mounted
 ■ on a 1in² pad of 2oz copper.



■ b) $R_{\theta JA}=96^{\circ}\text{C/W}$ when mounted
 ■ on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at $T_C=25^{\circ}\text{C}$ and $R_{DS(ON)}$ is at $T_{J(max)}$ and $V_{GS}=10\text{V}$. Package current limitation is 21A

4. $BV_{(avalanche)}$ Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.



7.1 Typical characteristic

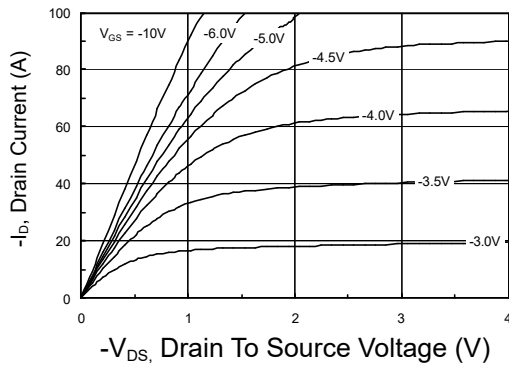


Figure 1: On-Region Characteristics

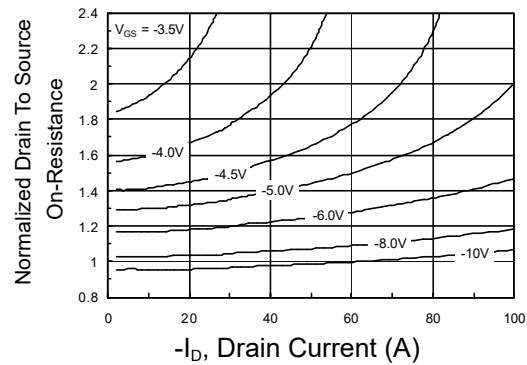


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

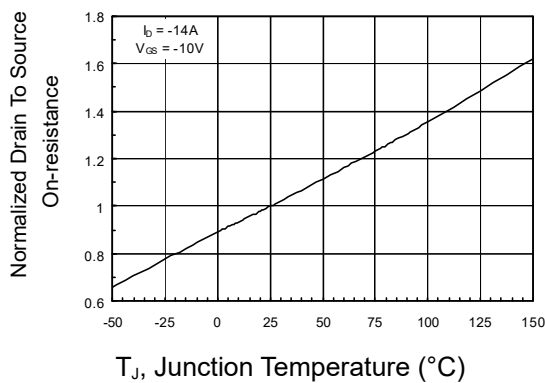


Figure 3: Normalized On Resistance vs Junction Temperature

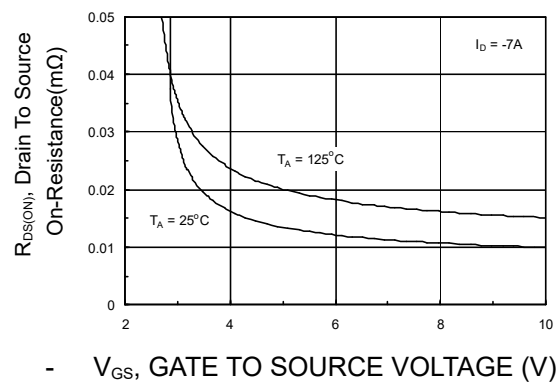


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

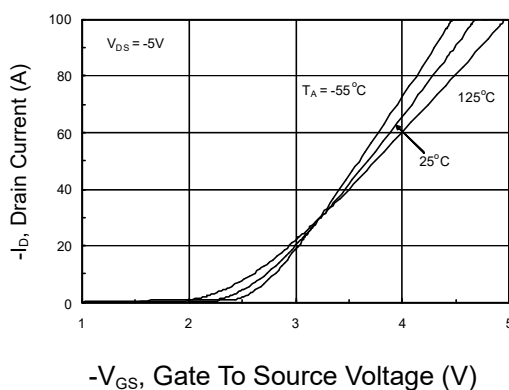


Figure 5: Transfer Characteristics

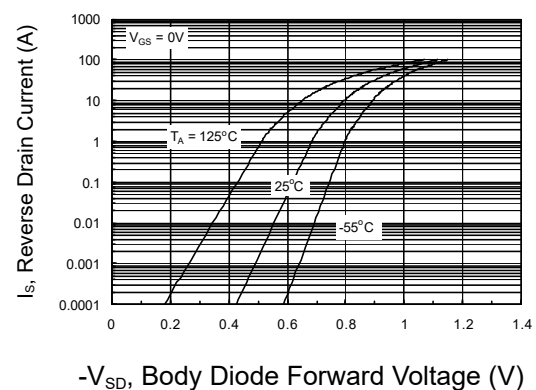
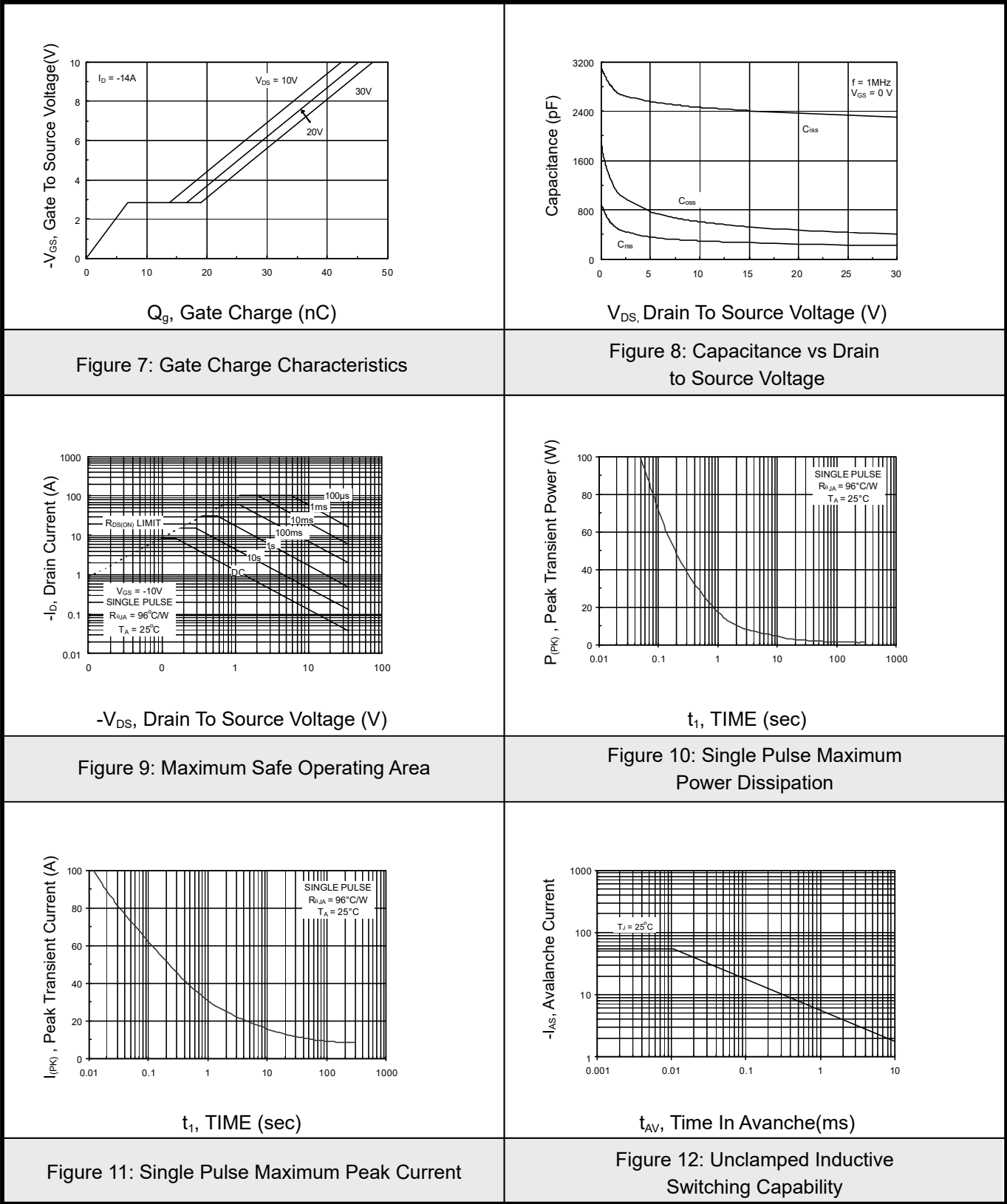


Figure 6: Source to Drain Diode Forward Voltage vs Source Current

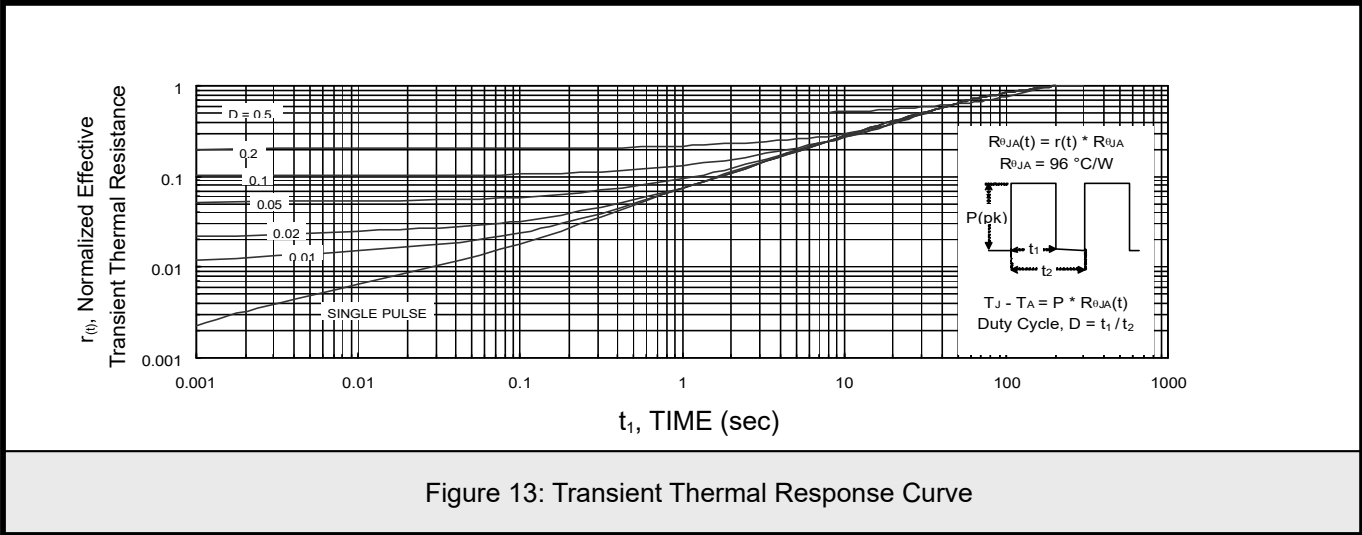


7.2Typical characteristic





7.3Typical characteristic





8. Test Circuits and Waveforms

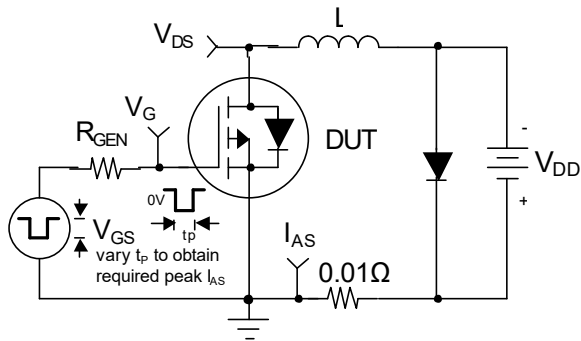


Figure 14. Unclamped Inductive Load Test Circuit

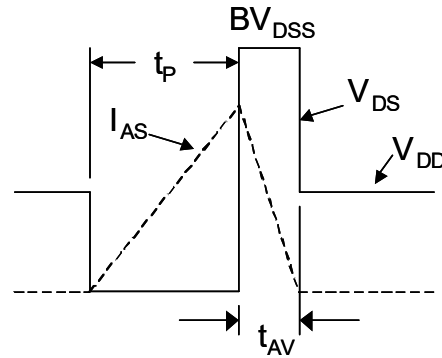


Figure 15. Unclamped Inductive Waveforms

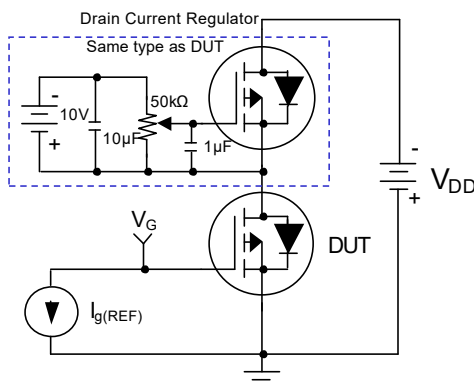


Figure 16. Gate Charge Test Circuit

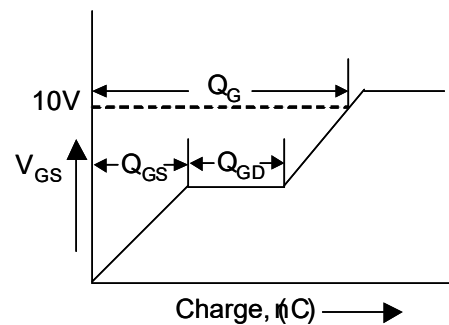


Figure 17. Gate Charge Waveform

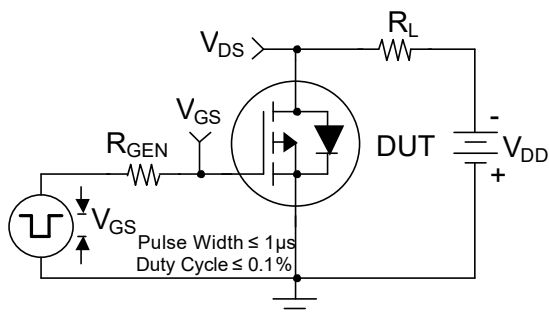


Figure 18. Switching Time Test Circuit

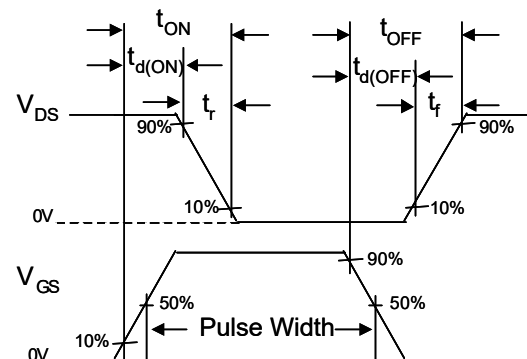
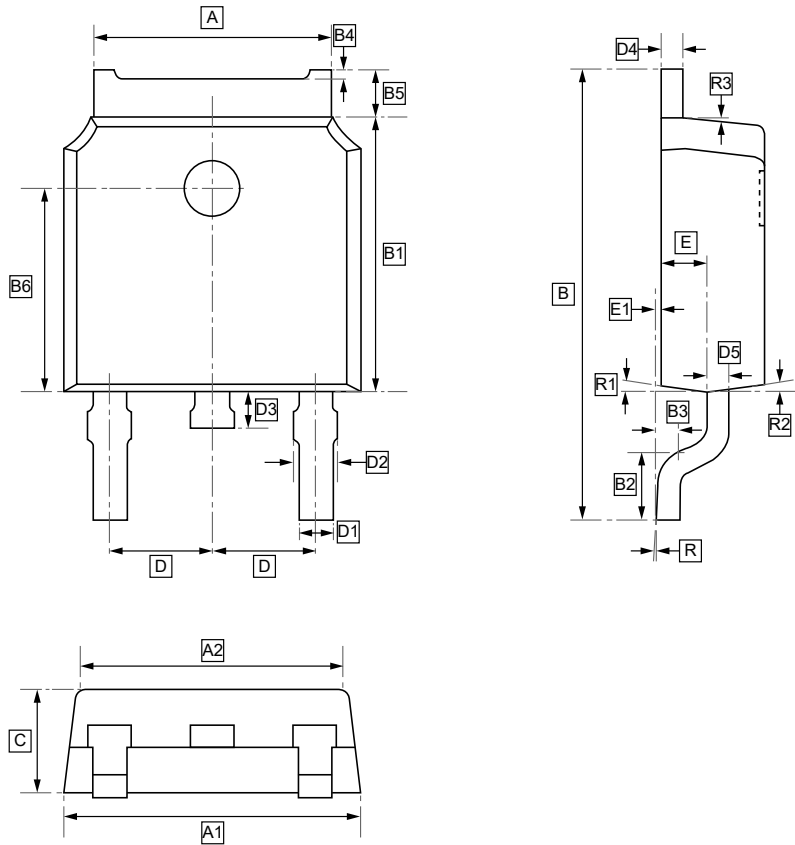


Figure 19. Switching Time Waveforms



9.TO-252 Package Outline Dimensions



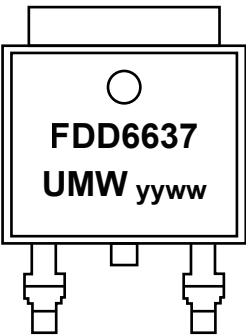
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	B3	B4	B5	B6	C	D
Min	5.1	6.4	5.6	9.5	5.9	1.35	0.4	0.1	0.85	4.35	2.15	2.286
Max	5.5	6.8	6.0	10.3	6.3	1.65	0.6	(typ.)	1.05	4.65	2.45	(typ.)

Symbol	D1	D2	D3	D4	D5	E	E1	R	R1	R2	R3
Min	0.66	0.81	0.65	0.42	0.42	0.86	0.05	0°	7°	7°	7°
Max	0.86	1.01	0.95	0.58	0.58	1.16	0.05	6°	(typ.)	(typ.)	(typ.)



10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD6637	TO-252	2500	Tape and reel



11.Disclaimer

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