1.Description

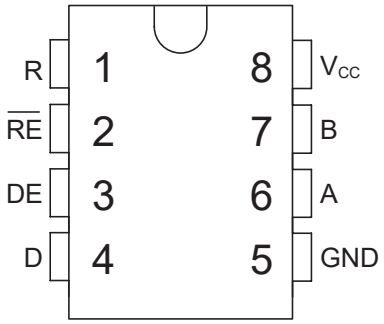
The SN75LBC184 and SN65LBC184 are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

The SN75LBC184 and SN65LBC184 can with stand overvoltage transients of 400-W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

2.Features

- Integrated Transient Voltage Suppression
- ESD Protection for Bus Terminals Exceeds:
  ±30 kV IEC 61000-4-2, Contact Discharge
  ±15 kV IEC 61000-4-2, Air-Gap Discharge
  ±15 kV EIA/JEDEC Human Body Model
- Circuit Damage Protection of 400-W Peak (Typical) Per IEC 61000-4-5
- Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths 250-kbps in Electrically Noisy Environments
- 1/4 Unit Load Allows for 128 Devices Connected on Bus
- Open-Circuit Fail-Safe Receiver Design
- Thermal Shutdown Protection
- Power-Up/-Down Glitch Protection
- Each Transceiver Meets or Exceeds the Requirements of TIA/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) Standards
- Low Disabled Supply Current 300 μA Max
- Pin Compatible With SN75176
- Applications:
  − Industrial Networks
  − Utility Meters
  − Motor Control

3.Pinning Information



SOP-8

4.Functional Logic Diagram (Positive Logic)

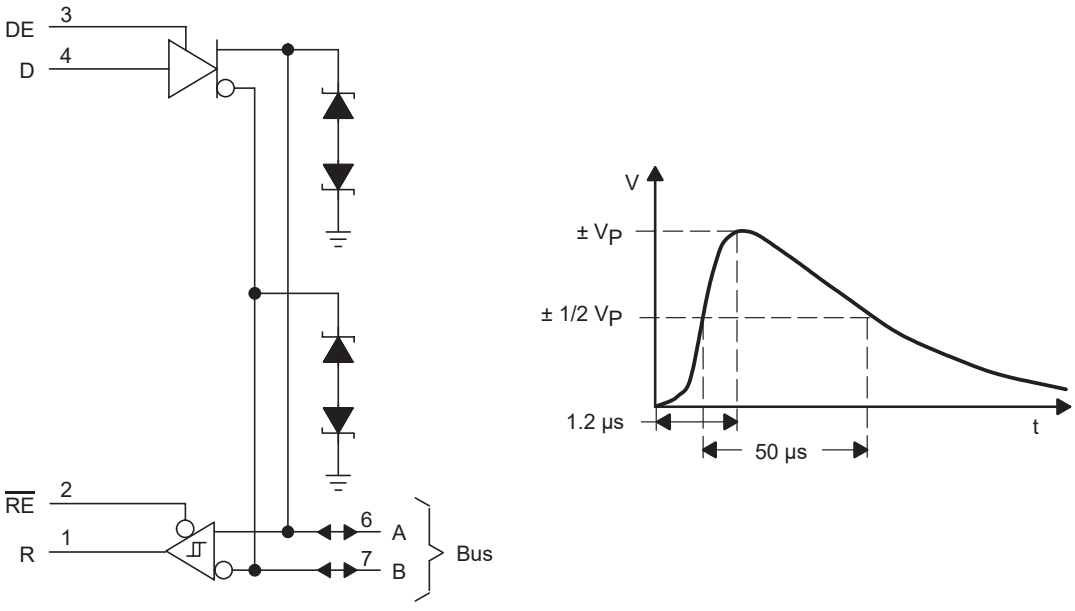


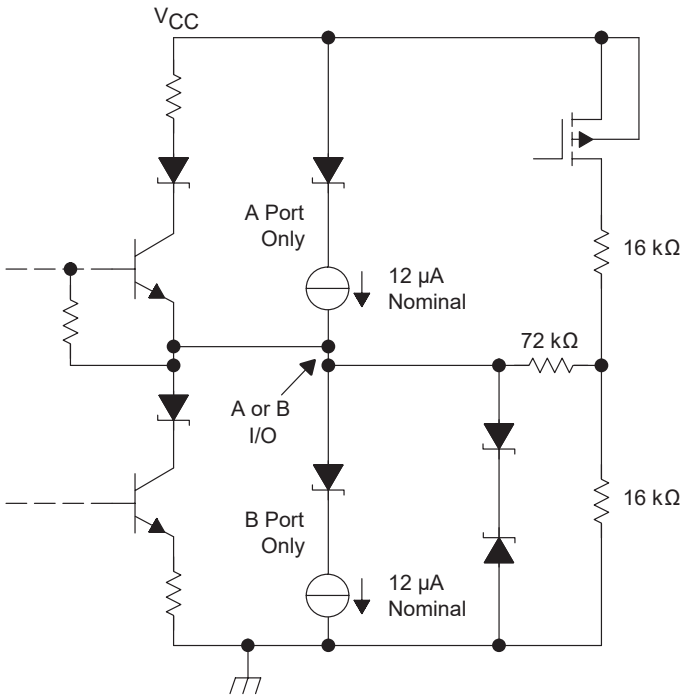
Figure 1. Surge Waveform — Combination Wave

5.Description (Continued)

A biexponential function defined by separate rise and fall times for voltage and current simulates the combination wave. The standard 1.2μs/50 μs combination waveform is shown in Figure1 and in the test description in Figure 15. The device also includes additional desirable features for party-line data buses in electrically noisy environment applications including industrial process control. The differential-driver design incorporates slew-rate-controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows longer unterminated cable runs and longer stub lengths from the main backbone than possible with uncontrolled and faster voltage transitions. A unique receiver design provides a fail-safe output of a high level when the inputs are left floating (open circuit). The SN75LBC184 and SN65LBC184 receiver also includes a high input resistance equivalent to one-fourth unit load allowing connection of up to 128 similar devices on the bus.

The SN75LBC184 is characterized for operation from -20°C to 85°C. The SN65LBC184 is characterized from −40°C to 105°C.

6.Schematic of Inputs And Outputs



Driver Function Table

Input	Enable	Outputs	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

Receiver Function Table

Differential Inputs	Enable	Output
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2V$	L	H
$-0.2V < V_{ID} < 0.2V$	L	?
$V_{ID} \leq -0.2V$	L	L
X	H	Z
Open	L	H

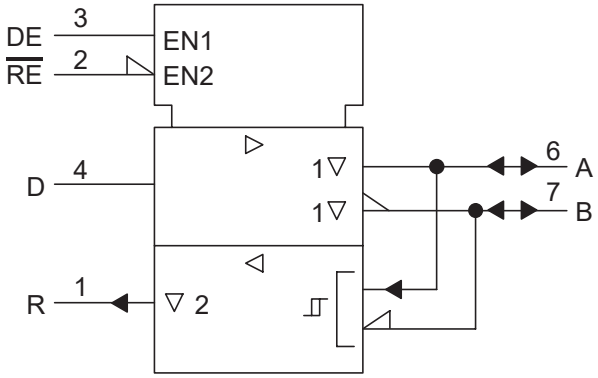
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

Available Options

T_A	Package	
	PLASTIC SMALL-OUTLINE† (JEDEC MS-012)	PLASTIC DUAL-IN-LINE PACKAGE (JEDEC MS-001)
-0°C to 70°C	SN75LBC184D	SN75LBC184P
−40°C to 105°C	SN65LBC184D	SN65LBC184P

† Add R suffix for taped and reel.

7.Logic Symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

8.Absolute Maximum Ratings Over Operating Free−air Temperature Range

(unless otherwise noted)†

Parameter	Value
Supply voltage, V_{CC} (see Note 1)	−0.5V to 7V
Continuous voltage range at any bus terminal	−15V to 15V
Data input/output voltage	−0.3V to 7V
Receiver output current, I_O	±20mA
Electrostatic discharge: Contact discharge (IEC61000-4-2) A, B, GND (see Note 2)	30kV
Air discharge (IEC61000-4-2) A, B, GND (see Note 2)	15kV
Human body model (see Note 3) A, B, GND (see Note 2)	15kV
All pins	3kV
All terminals (Class 3A) (see Note 2)	8kV
All terminals (Class 3B) (see Note 2)	1200V
Continuous total power dissipation (see Note 4)	Internally Limited

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

2. GND and bus terminal ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.

3. Tested in accordance with JEDEC Standard 22, Test Method A114-A.

4. The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the Dissipation Rating Table.

Dissipation Rating Table

Package	$T_A \leq 25°C$	Above $T_A=25°C$	$T_A=70°C$	$T_A=85°C$
	Power Rating	Derating Factor	Power Rating	Power Rating
D	725mW	5.8mW/°C	464mW	377mW
P	1150mW	9.2mW/°C	736mW	598mW

9.Recommended Operating Conditions

Parameter		Symbol	Min‡	Typ	Max	Units
Supply voltage		V_{CC}	4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode)		V_I or V_{IC}	-7		12	V
High-level input voltage	D, DE, and RE	V_{IH}	2			V
Low-level input voltage	D, DE, and RE	V_{IL}			0.8	V
Differential input voltage		V_{ID}			12	V
High-level output current	Driver	I_{OH}	-60			mA
	Receiver		-8			mA
Low-level output current	Driver	I_{OL}			60	mA
	Receiver				4	mA
Operating free-air temperature	SN75LBC184	T_A	0		70	°C
	SN65LBC184		-40		105	°C

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.

10.Electrical Characteristics Over Recommended Operating Conditions

(unless otherwise noted)

Parameter		Symbol	Conditions	Min	Typ†	Max	Units
Supply current	I_{CC}	NA	DE=$\overline{RE}$=5V, No Load		12	25	mA
			DE=0V, $\overline{RE}$=5V, No Load		175	300	μA
High-level input current (D, DE, $\overline{RE}$)	I_{IH}	NA	V_I=2.4V			50	μA
Low-level input current (D, DE, $\overline{RE}$)	I_{IL}	NA	V_I=0.4V	-50			μA
Short-circuit output current (see Note 5)	I_{OS}	NA	V_O=-7V	-250	-120		mA
			V_O=V_{CC}			250	mA
			V_O=12V			250	mA
High-impedance output current	I_{OZ}	NA					mA
Output voltage	V_O	V_{oa}, V_{ob}	I_O=0	0		V_{CC}	V
Peak-to-peak change in common mode output voltage during state transitions	$V_{OC(PP)}$	NA	See Figures 5 and 6		0.8		V
Common-mode output voltage	V_{OC}	$\lvert V_{OS}\rvert$	See Figure 4	1		3	V
Magnitude of change, common mode steady-state output voltage	$\lvert\Delta V_{OC(SS)}\rvert$	$\lvert V_{OS}-\overline{V}_{OS}\rvert$	See Figure 5			0.1	V
Magnitude of differential output voltage $\lvert V_A - V_B\rvert$	$\lvert V_{OD}\rvert$	V_O	I_O=0	1.5		6	V
			R_L=54 Ω, See Figure 4	1.5			V
Change in differential voltage magnitude between logic states	$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	R_L=54 Ω			0.1	V

† All typical values are measured with T_A=25°C and V_{CC}=5V.

Note 5: This parameter is measured with only one output being driven at a time.

11.Switching Characteristics Over Recommended Operating Conditions

(unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential output delay time low-to-high-level output	$t_{d(DH)}$	R_L=54Ω, C=50pF See Figure 5			1.3	μs
Differential-output delay time high-to-low-level output	$t_{d(DL)}$				1.3	μs
Propagation delay time, low-to-high-level output	t_{PLH}			0.5	1.3	μs
Propagation delay time, high-to-low-level output	t_{PHL}			0.5	1.3	μs
Pulse skew ($\|t_{d(DH)} - t_{d(DL)}\|$)	$t_{sk(p)}$			75	150	μs
Rise time, single ended	t_r		0.25		1.2	μs
Fall time, single ended	t_f		0.25		1.2	μs
Output enable time to high level	t_{PZH}	R_L=110Ω, See Figure 2			3.5	μs
Output enable time to low level	t_{PZL}	R_L=110Ω, See Figure 3			3.5	μs
Output disable time from high level	t_{PHZ}	R_L=110Ω, See Figure 2			2	μs
Output disable time from low level	t_{PLZ}	R_L=110Ω, See Figure 3			2	μs

12.Electrical Characteristics Over Recommended Operating Conditions

(unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ†	Max	Units
Supply current (total package)	I_{CC}	DE=$\overline{RE}$=0V, No Load				3.9	mA
		DE=0V, $\overline{RE}$=5V, No Load				300	μA
Input current	I_I	Other input=0V	V_I=12V			250	μA
			V_I=12V, V_{CC}=0			250	μA
			V_I=-7V	-200			μA
			V_I=-7V, V_{CC}=0	-200			μA
High-impedance-state output current	I_{OZ}	V_O=0.4V to 2.4V				±100	μA
Input hysteresis voltage	V_{hys}				70		mV
Positive-going input threshold voltage	V_{IT+}					200	mV
Negative-going input threshold voltage	V_{IT-}			-200			mV
High-level output voltage	V_{OH}	I_{OH}=-8mA, Figure 7		2.8			V
Low-level output voltage	V_{OL}	I_{OL}=4mA, Figure 7				0.4	V

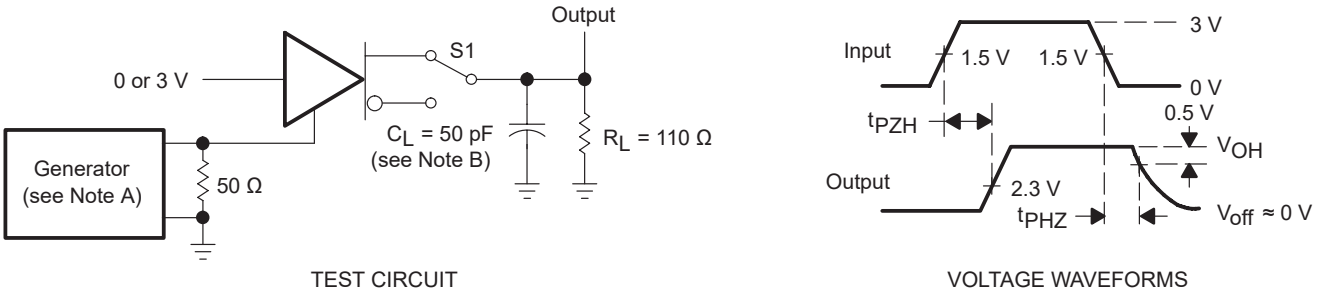
† All typical values are at V_{CC}=5V, T_A =25°C.

13.Switching Characteristics Over Recommended Operating Conditions

(unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Propagation delay time, low-to-high-level output	t_{PLH}	C_L=50pF, See Figure 7			150	ns
Propagation delay time, high-to-low-level output	t_{PHL}				15	ns
Pulse skew ($\|t_{pHL} - t_{pLH}\|$)	$t_{sk(p)}$				50	ns
Rise time, single ended	t_r	See Figure 7		20		ns
Fall time, single ended	t_f			20		ns
Output enable time to high level	t_{PZH}	See Figure 8			100	ns
Output enable time to low level	t_{PZL}				100	ns
Output disable time from high level	t_{PHZ}				100	ns
Output disable time from low level	t_{PLZ}				100	ns

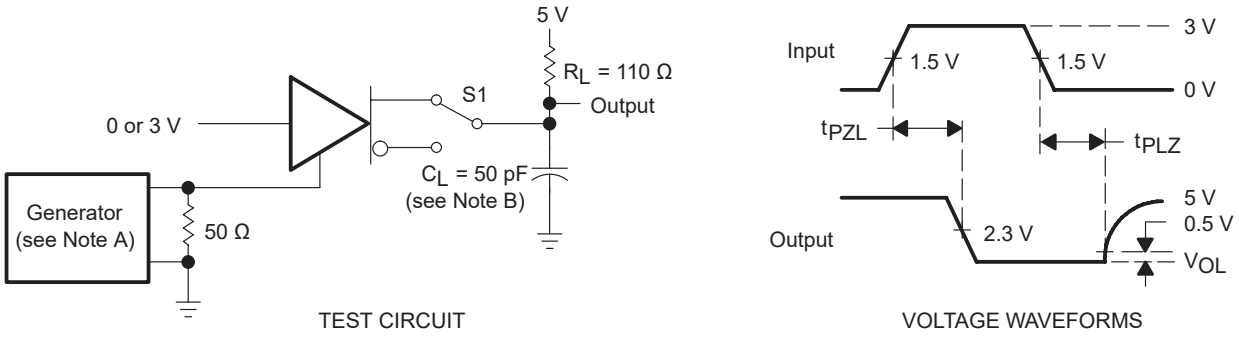
14.Parameter Measurement Information



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR=1.25kHz, 50% duty cycle t_r ≤10ns, t_f ≤ 10ns, Z_O=50Ω.

B. C_L includes probe and jig capacitance.

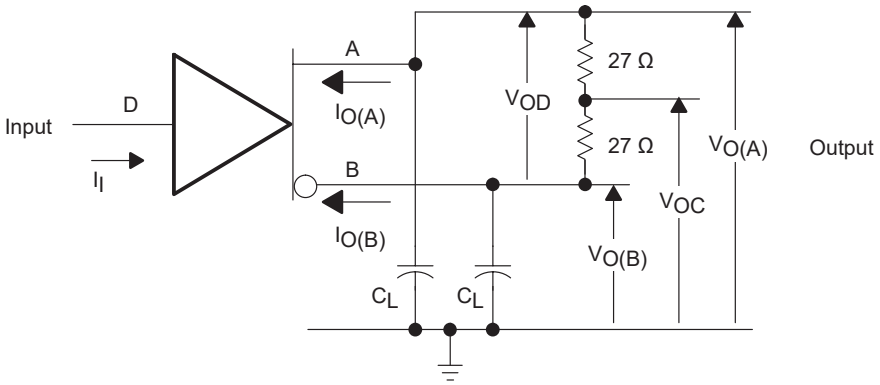
Figure 2. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR=1.25kHz, 50% duty cycle t_r ≤10ns, t_f ≤ 10ns, Z_O=50Ω.

B. C_L includes probe and jig capacitance.

Figure 3. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



NOTES: A. Resistance values are in ohms and are 1% tolerance.

B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit, Voltage, and Current Definitions

15.Parameter Measurement Information

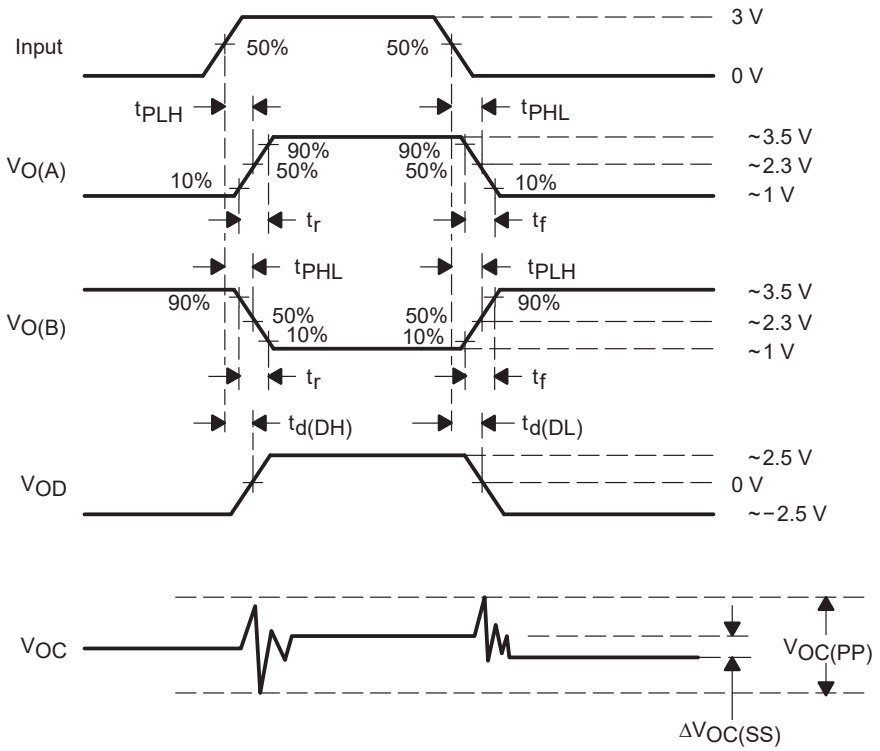
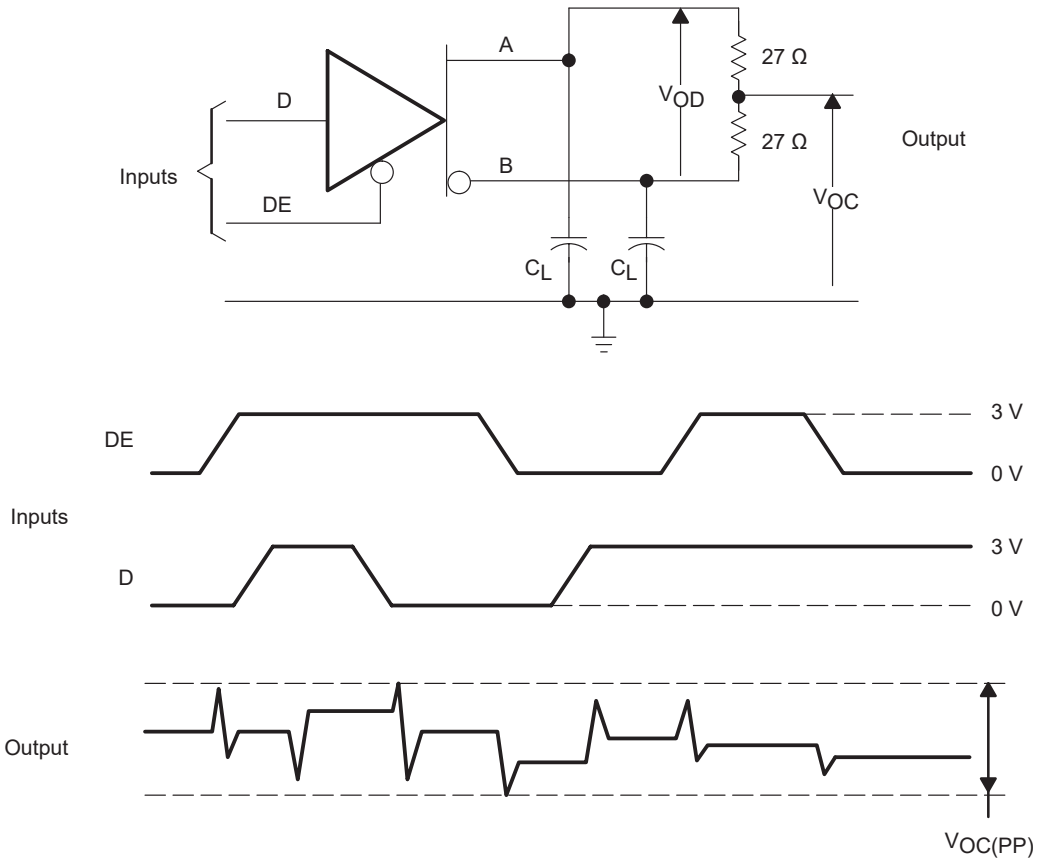


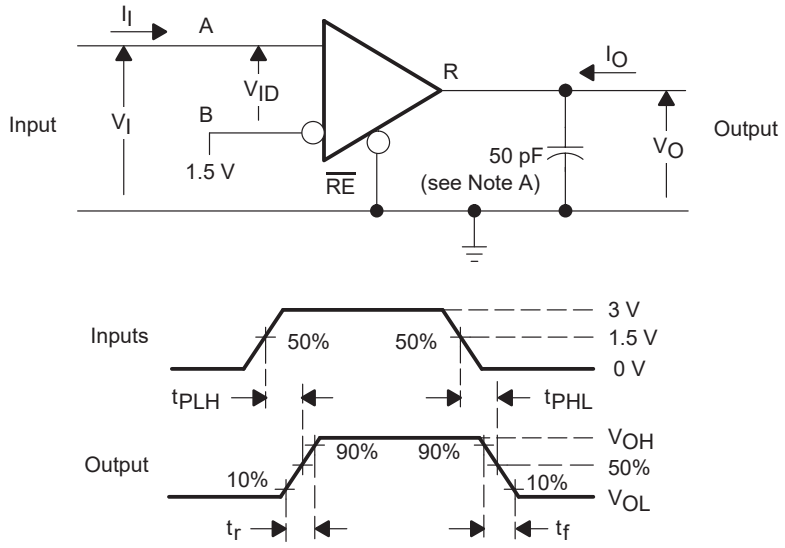
Figure 5. Driver Timing, Voltage and Current Waveforms



NOTES: A. Resistance values are in ohms and are 1% tolerance.

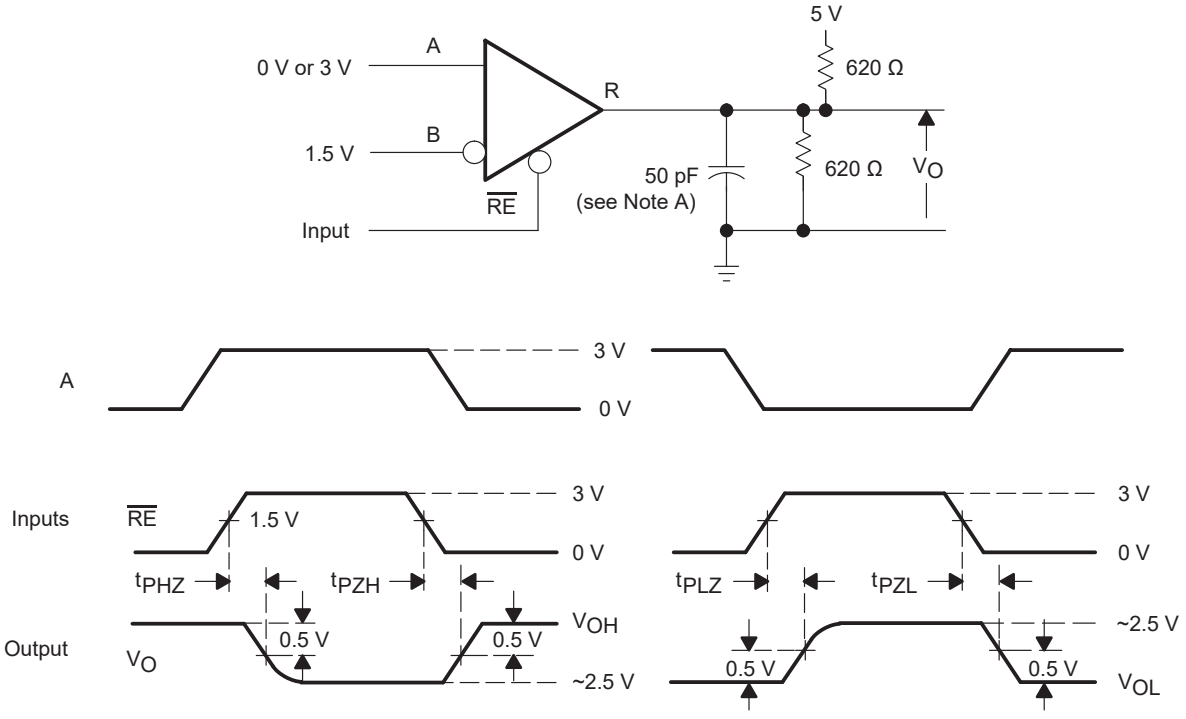
B. C_L includes probe and jig capacitance (± 10%).

Figure 6. Driver $V_{OC(PP)}$ Test Circuit and Waveforms



NOTE A: This value includes probe and jig capacitance (± 10%).

Figure 7. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



NOTE A: This value includes probe and jig capacitance (± 10%).

Figure 8. Receiver t_{PZL}, t_{PLZ}, t_{PZH}, and t_{PHZ} Test Circuit and Voltage Waveforms

16.Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD}=V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant.

Driver Functions

Input(1)	Enable	Outputs		Function
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. When the transceiver is disconnected from the bus, the receiver provides a failsafe high output.

Receiver Functions

Differential Input	Enable(1)	Output	Function
$V_{ID}=V_A - V_B$	$\overline{RE}$	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
OPEN	L	H	Receiver failsafe High

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

17.Typical Characterisitics

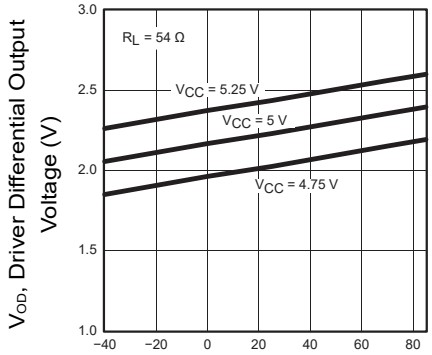


Figure 9: Driver Differential Output Voltage vs Free-air Temperature

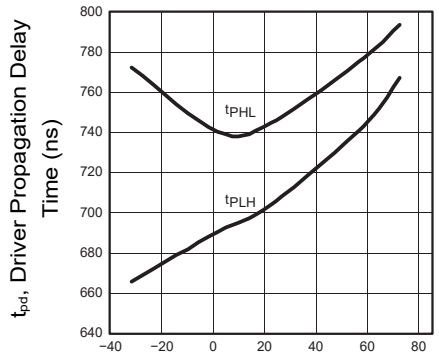


Figure 10: Driver Propagation Delay Time vs Free-air Temperature

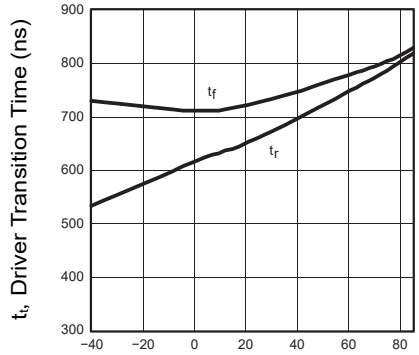


Figure 11: Driver Transition Time vs Free-air Temperature

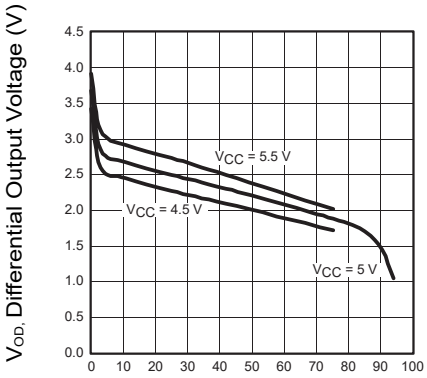


Figure 12: Differential Output Voltage vs Output Current

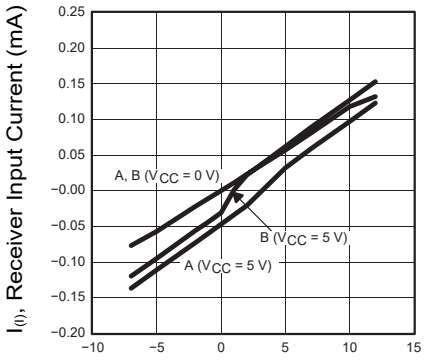
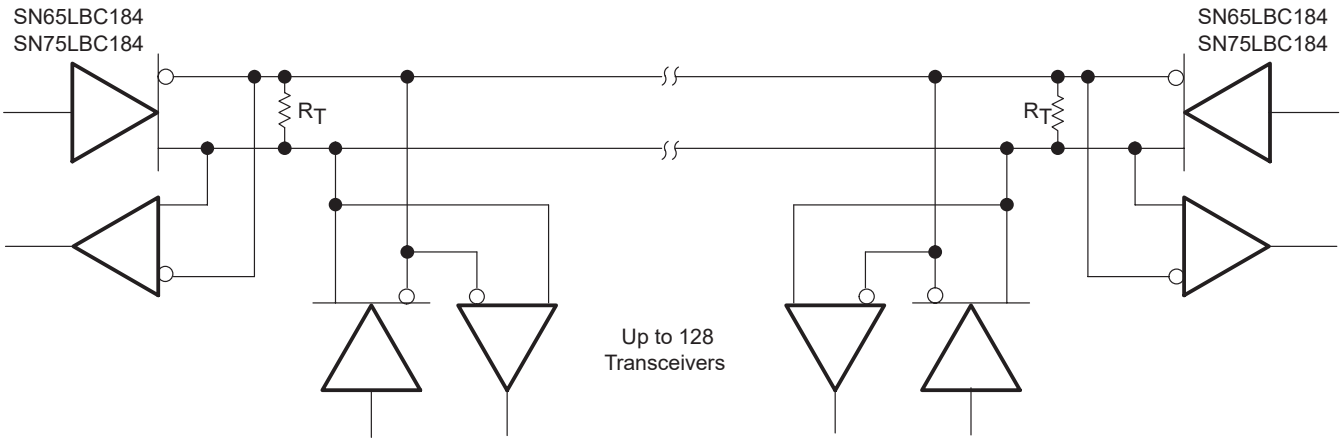


Figure 13: Receiver Input Current vs Input Voltage

18.Application Information



NOTE A: The line should be terminated at both ends in its characteristic impedance (R_T=Z_O). Stub lengths off the main line should be kept as short as possible.

Figure 14. Typical Application Circuit

'LBC184 test description

The 'LBC184 is tested against the IEC 61000-4-5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50-μs open-circuit voltage waveform and a 8-/20-μs short-circuit current waveform shown in Figure 15. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2Ω. The setup for the overvoltage stress is shown in Figure 16 with all testing performed with power applied to the 'LBC184 circuit.

NOTE High voltage transient testing is done on a sampling basis.

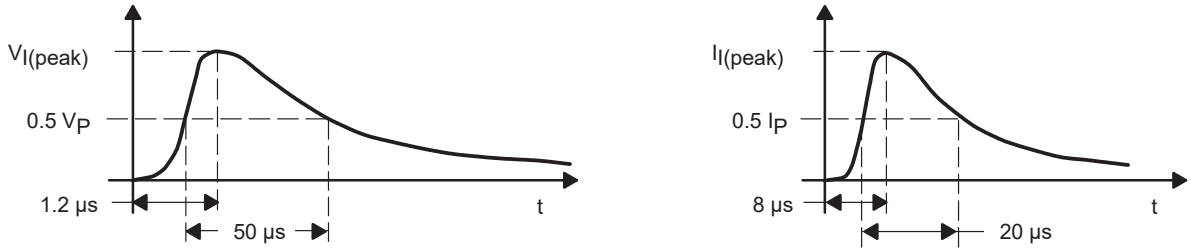


Figure 15. Short-Circuit Current Waveforms

The ’LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The ’LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A & B) across ground as shown in Figure 16.

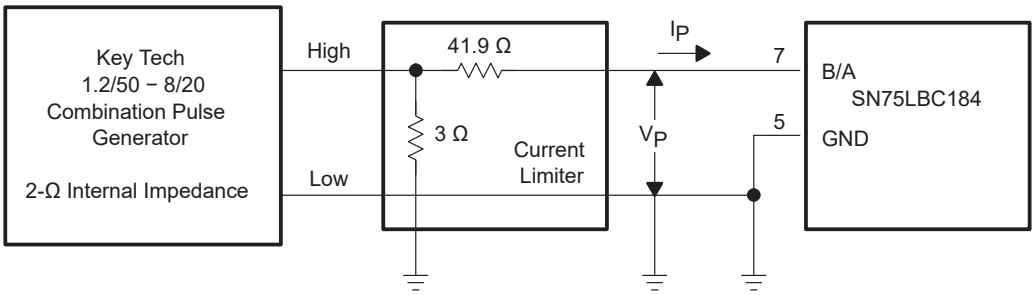


Figure 16. Overvoltage-Stress Test Circuit

An example waveform as seen by the ’LBC184 is shown in Figure 17. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 16V, peak current of 33.6 A yielding an absorbed peak power of 538 W.

NOTE: A circuit reset may be required to ensure normal data communications following a transient noise pulse of greater than 250 W peak.

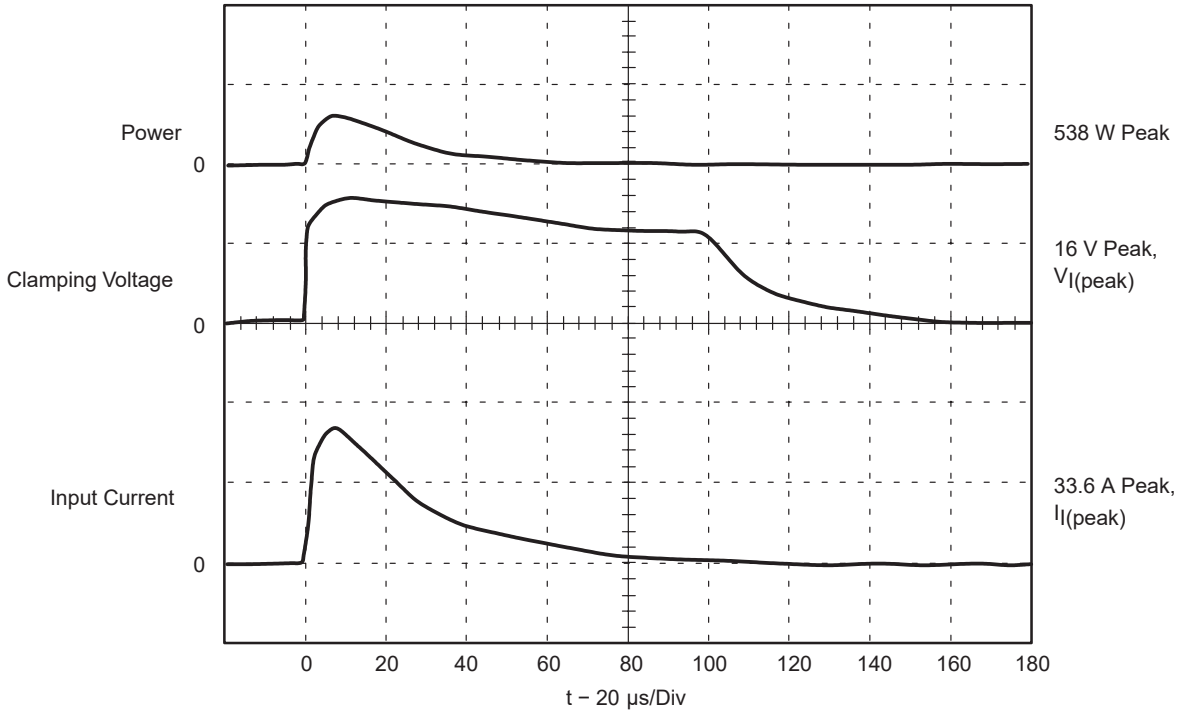
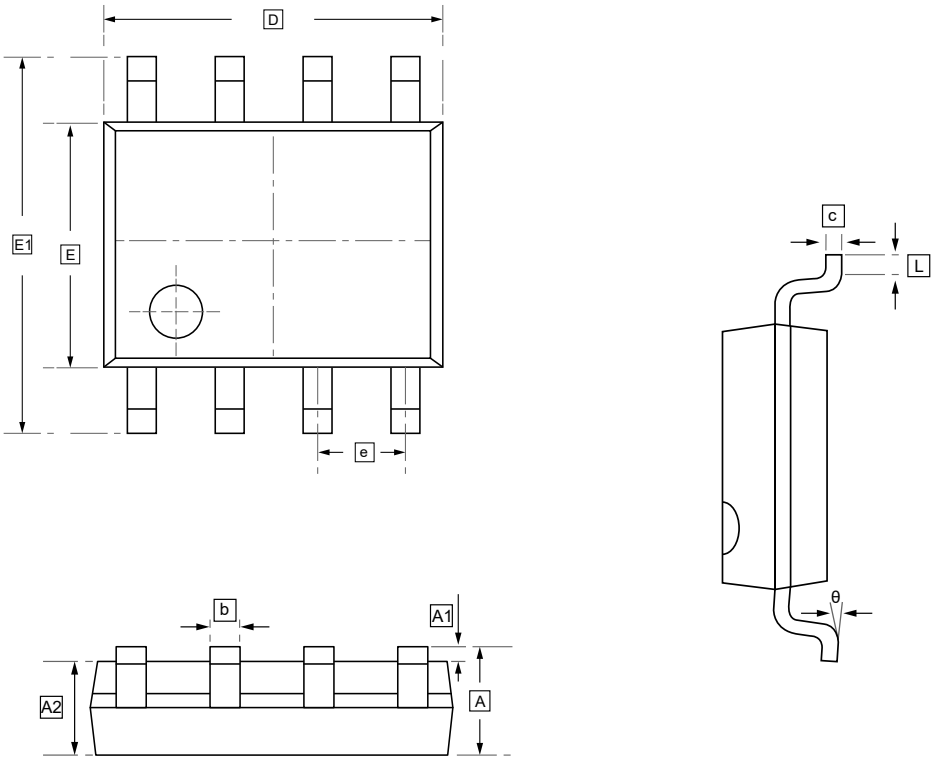


Figure 17. Typical Surge Waveform Measured At Terminals 5 and 7

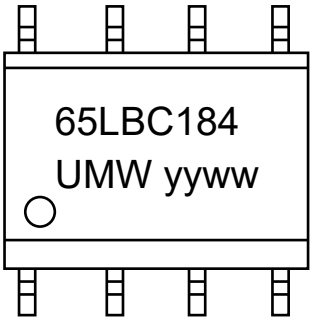
19.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

20.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW SN65LBC184DR	65LBC184	SOP-8	2500	Tape and reel
UMW SN75LBC184DR	75LBC184	SOP-8	2500	Tape and reel

21.Disclaimer

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