UMW AO4447A

-30V P-Channel MOSFET

1.Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- ESD Protected
- RoHS and Halogen-Free Compliant

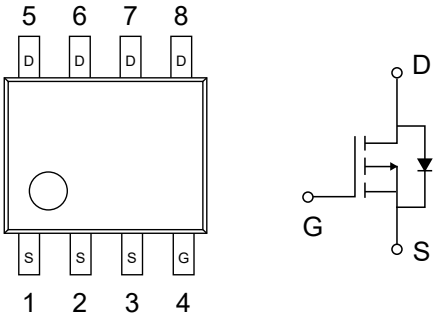
2.Features

- $V_{DS\ (V)}$=-30V
- I_D=-18.5A(V_{GS}=-10V)
- $R_{DS(ON)}$＜5.8mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$＜8.2mΩ(V_{GS}=-4.5V)

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A=25°C	I_D	-18.5	A
	T_A=70°C		-14.5	
Pulsed Drain Current [c]		I_{DM}	-74	
Avalanche Current [c]		I_{AS}	54	
Avalanche energy L=0.1mH [c]		E_{AS}	146	mJ
Power Dissipation [B]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient	Steady-State		59	75	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V			-1	μA
		T_J=55°C			-5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±16V			±10	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1.2	-1.7	-2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-18.5A		4.7	5.8	mΩ
		V_{GS}=-4.5V, I_D=-16A		6.3	8.2	
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-18.5A		65		S
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V		-0.66	-1	V
Maximum Body-Diode Continuous Current	I_S				-4	A
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz		5020		pF
Output Capacitance	C_{oss}			815		
Reverse Transfer Capacitance	C_{rss}			615		
Gate resistance	R_g	f=1MHz		125	250	Ω
Total Gate Charge	Q_g(10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-18.5A		93	130	nC
Total Gate Charge	Q_g(4.5V)			46		
Gate Source Charge	Q_{gs}			14		
Gate Drain Charge	Q_{gd}			21		
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, R_L=0.8Ω, R_{GEN}=3Ω		180		ns
Turn-On Rise Time	t_r			280		
Turn-Off DelayTime	$t_{D(off)}$			1400		
Body Diode Reverse Recovery Time	t_{rr}	I_F=-18.5A, dI/dt=500A/μs		17		
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=-18.5A, dI/dt=500A/μs		53		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

7.1Typical characteristic

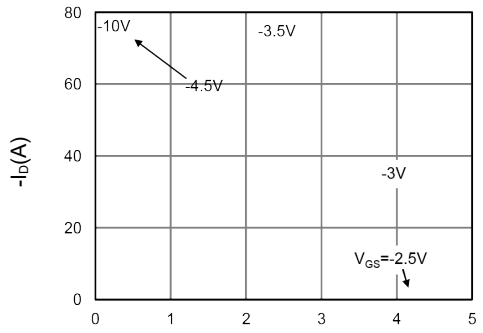


Fig 1: On-Region Characteristics (Note E)

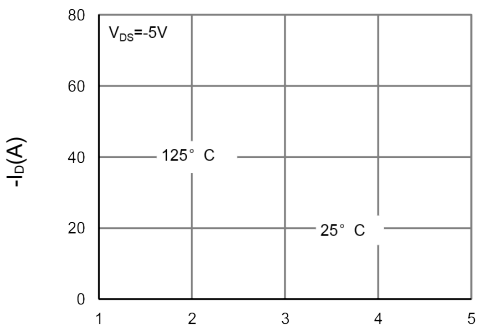


Figure 2: Transfer Characteristics (Note E)

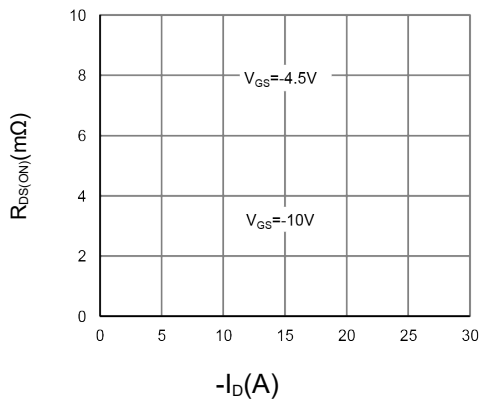


Figure 3: Voltage (Note E)

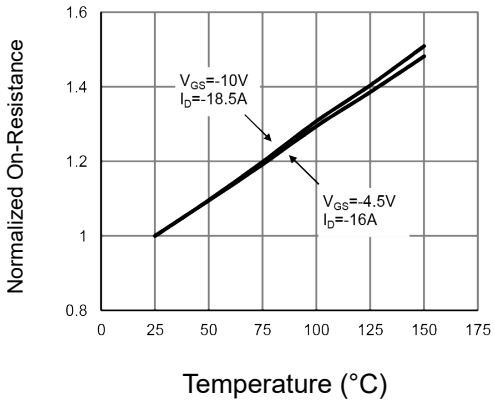


Figure 4: (Note E)

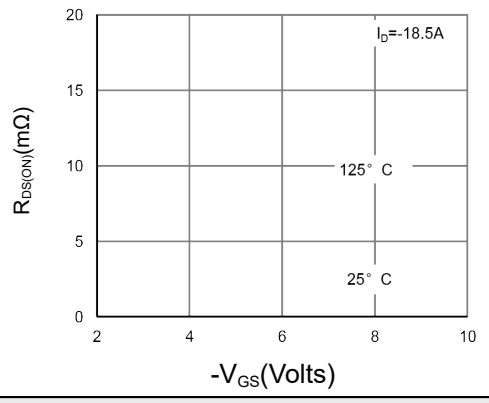


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

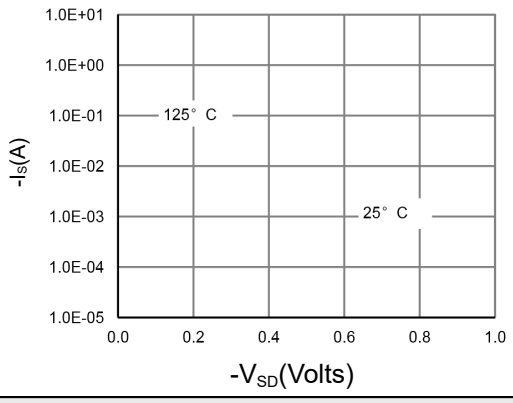


Figure 6: Body-Diode Characteristics(Note E)

7.2Typical characteristic

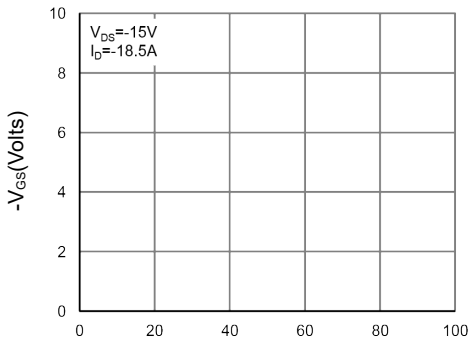


Figure 7: Gate-Charge Characteristics

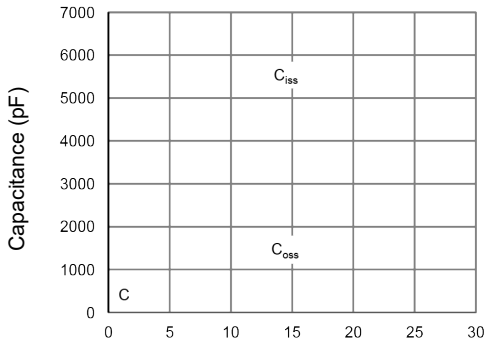


Figure 8: Capacitance Characteristics

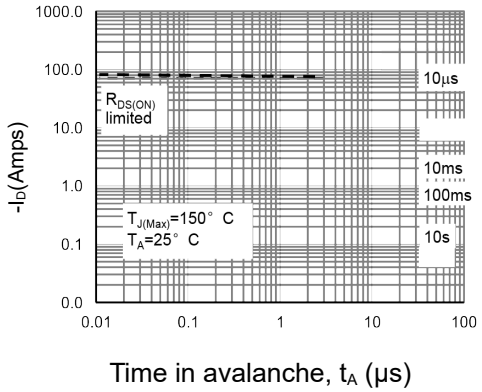


Figure 9: Single Pulse Avalanche capability (Note C)

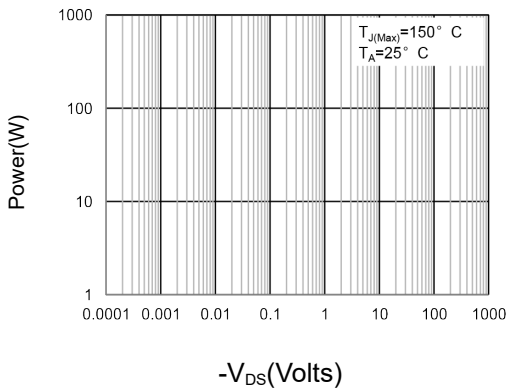


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

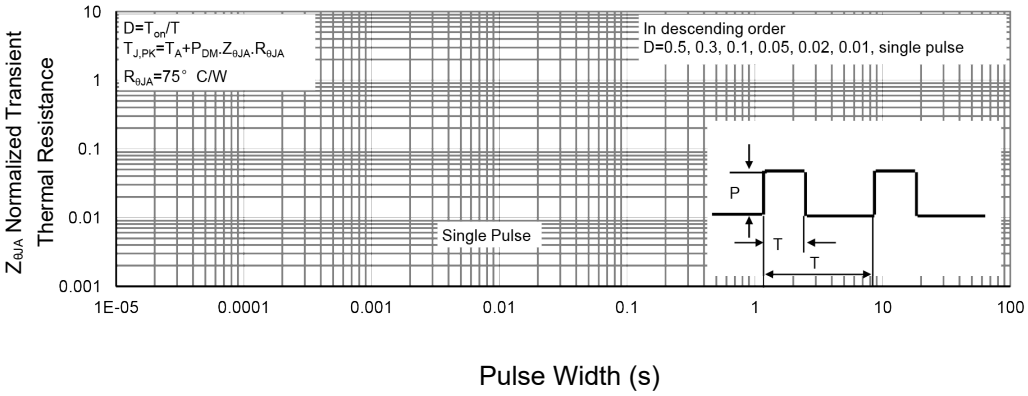
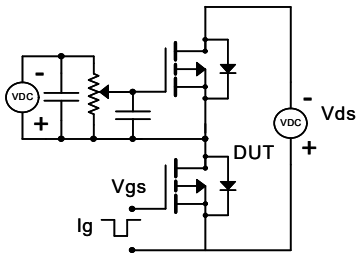
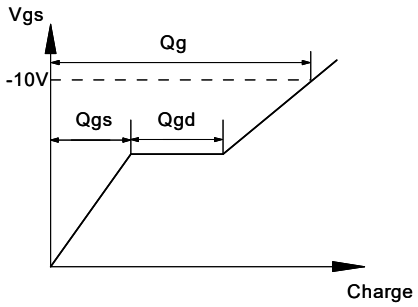


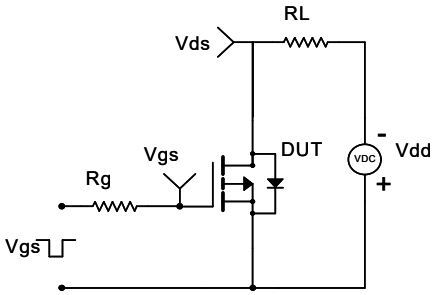
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

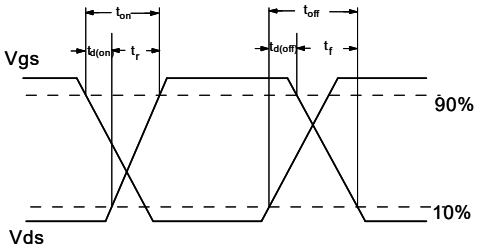
Gate Charge Test Circuit & Waveform



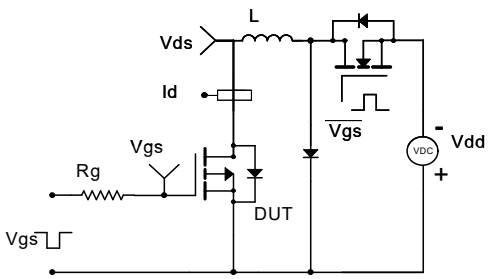


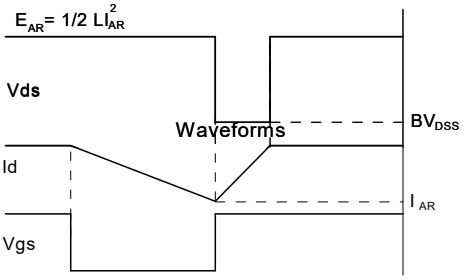
Resistive Switching Test Circuit & Waveforms



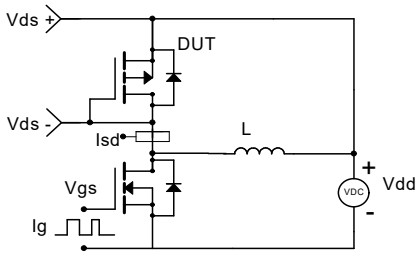


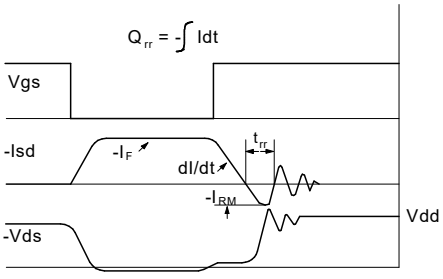
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



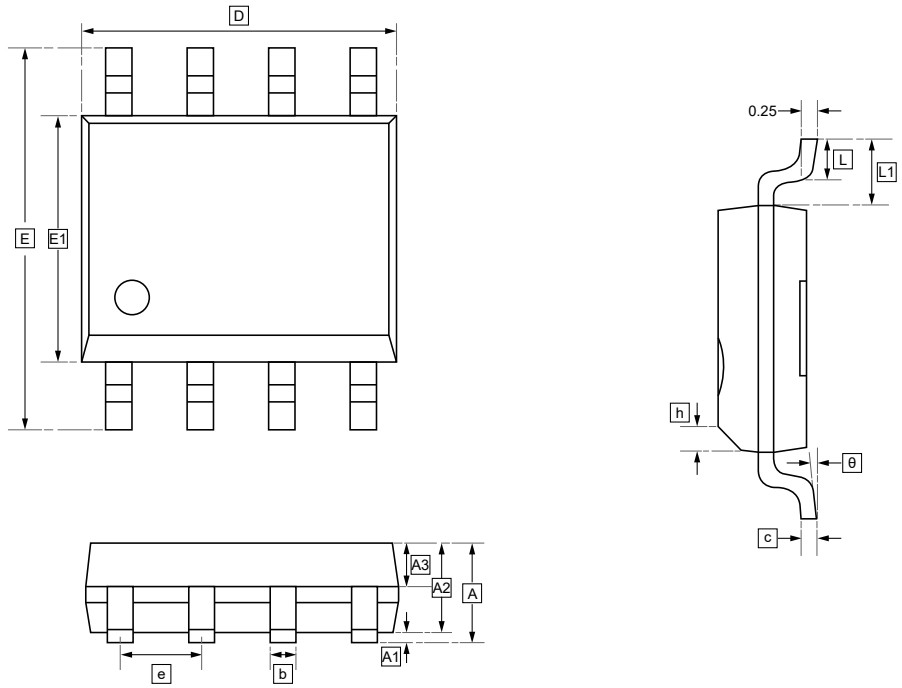


Diode Recovery Test Circuit & Waveforms





8.SOP-8 Package Outline Dimensions

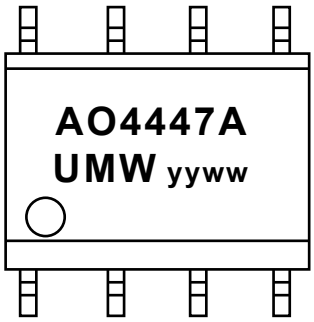


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4447A	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.