1.Description

The UMW LMV721A (single), LMV722A (dual) and UMW LMV724A (quad) are low noise, low voltage, and micro power operational amplifiers. With an excellent bandwidth of 10MHz, a slew rate of 9V/μs and a quiescent current of 1000μA per amplifier at 5V, the UMW LMV72xA family can be designed into a wide range of applications.

The UMW LMV72xA op-amps are designed to provide optimal performance in low voltage and low noise systems. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5mV. These parts provide rail-to-rail output swing into heavy loads. The UMW LMV72xA family is specified for single or dual power supplies of +2.5V to +5.5V. All models are specified over the extended industrial temperature range of −40°C to +125°C.

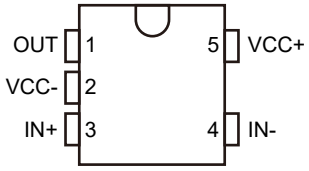
2.Features

- High Slew Rate: 9V/μs
- Wide Bandwidth: 10MHz
- Low Power: 1000μA per Amplifier Supply Current
- Settling Time to 0.1% with 2V Step: 0.25 μs
- Low Noise: 20 nV/ Hz@10kHz
- Low Offset Voltage: 3.5 mV Maximum
- Unit Gain Stable
- Rail-to-Rail Input and Output
- Input Voltage Range: -0.1V to +5.1V at 5V Supply
- Operating Power Supply: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +125°C

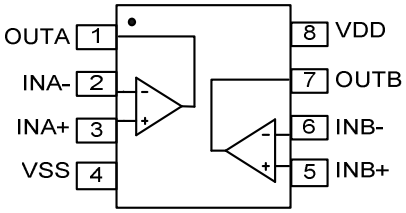
3.Application

- Photodiode Amplification
- Sensor Interfaces
- Audio Outputs
- Active Filters
- Driving A/D Converters
- Portable Equipment & Battery-Powered Instrumentation

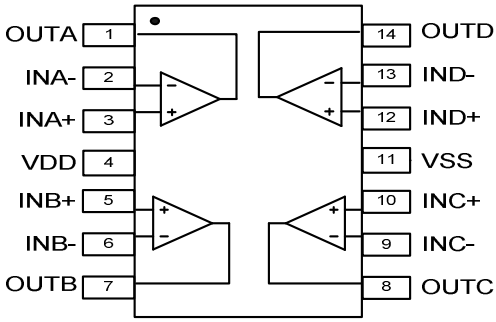
4.Pinning information



LMV721
SOT23-5/SC70-5



LMV722
SOP-8/TSSOP-8/MSOP-8



LMV724
SOP-14/TSSOP-14

Symbol	Description
-IN	Negative (inverting) input
+IN	Positive (noninverting) input
-INA, -INB -INC, IND	Inverting Input of the Amplifier. The Voltage range can go from (V_{S-} – 0.1V) to (V_{S+} + 0.1V)
+INA, +INB +INC, +IND	Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN
+VS	Positive Power Supply. The voltage is from 2.5V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is between 2.5V and 5.5V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground
-VS	Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 2.5V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible
OUT	Output
OUTA, OUTB OUTC, OUTD	Amplifier Output

5.Absolute Maximum Ratings (T_A=25°C)

Parameter	Symbol	Value	Unit
Supply Voltage, V_{S+} to V_{S-}	V_{S+},V_{S-}	7.0	V
Common-Mode Input Voltage	V_{CM}	V_{S-} –0.3 to V_{S+} +0.3	V
Electrostatic Discharge Voltage	ESD	HBM ± 4000	V
		CDM ± 1000	V
Junction Temperature	T_J	160	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C(T_J)
Lead Temperature Range(Soldering 10 sec)	T_{JL}	260	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Input terminals are diode-clamped to the power-supply rails.
3. Provided device does not exceed maximum junction temperature (T_J) at any time.

6.1 Electrical Characteristics (T_A=25°C)

(V_S=5.0V ,T_A=+25°C, V_{CM}=V_S/2 ,V_O=V_S/2, R_L=10kΩ connected to V_S/2, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Input offset voltage	V_{OS}		-3.5	±0.8	3.5	mV
		B Version	-0.9	±0.4	0.9	mV
		C Version	-0.35	±0.1	0.35	mV
Offset voltage drift	V_{OS}TC			3		μV/°C
Input bias current	I_B			260		nA
Over temperature						
Input ofiset current	I_{OS}			25		nA
Common-mode voltage range	V_{CM}		V_{S-}-0.1		V_{S+}+0.1	V
Common-mode rejection ratio	CMRR	V_{CM}=0.05V to 3.5V	70	84		dB
Over temperature				80		dB
		V_{CM}=V_{S-}–0.1 to V_{S+}+0.1V	60	76		dB
Open-loop voltage gain	A_{VOL}	R_L=10kΩ, V_O=0.1 to 4.9V	90	102		dB
Over temperature				90		dB
		R_L=600Ω, V_O=0.2 to 4.8V	80	89		dB
Over temperature				80		dB
Input resistance	R_{IN}			100		GΩ
Input capacitance	C_{IN}	Differential		2		pF
		Common mode		3.5		pF

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Characteristics						
High output voltage swing	V_{OH}	R_L=600Ω		V_{S+}-100		mV
		R_L=10kΩ		V_{S+}-8		mV
Low output voltage swing	V_{OL}	R_L=600Ω		100		mV
		R_L=10kΩ		8		mV
Closed-loop output impedance	Z_{OUT}	f=200kHz, G=+1		0.8		Ω
Open-loop output impedance		f=1MHz, I_O=0		3		Ω
Short-circuit current	I_{SC}	Source current through 10Ω		40		mA
		Sink current through 10Ω		40		mA

6.2 Electrical Characteristics (T_A=25°C)

(V_S=5.0V ,T_A=+25°C, V_{CM}=V_S/2 ,V_O=V_S/2, R_L=10kΩ connected to V_S/2, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Dynamic Performance						
Gain bandwidth product	GBW	f=1kHz		10		MHz
Phase margin	Φ_M	C_L=100pF		60		°
Slew rate	SR	G=+1, C_L=100pF, V_O=1.5V to 3.5V		9		V/μs
Full power bandwidth	BW_P	<1% distortion		400		kHz
Settling time	t_s	To 0.1%, G=+1, 2V step		0.25		μs
		To 0.01%, G=+1, 2V step		0.28		μs
Overload recovery time	t_{OR}	V_{IN} * Gain > V_S		0.5		μs
Noise Performance						
Input voltage noise	V_N	f=0.1 to 10Hz		12		μV_{P-P}
Input voltage noise density	e_n	f=10kHz		20		nV/√Hz
Input current noise density	I_n	f=10kHz		5		fA/√Hz
Power Supply						
Operating supply voltage	V_S		2.5		5.5	V
Power supply rejection ratio	PSRR	V_S=2.7V to 5.5V	70	95		dB
Over temperature		V_{CM}<V_{S+} +0.5V		80		dB
Quiescent current (per amplifier)	I_Q			1000	1300	μA
Over temperature				1200	1600	μA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Characteristics						
Operating temperature range	T_A		-40		125	°C
Package thermal resistance	θ_{JA}	SC70-5		333		°C/W
		SOT23-5		190		°C/W
		SOP-8		125		°C/W
		TSSOP-8		153		°C/W
		MSOP-8		216		°C/W
		TSSOP-14		112		°C/W
		SOP-14		115		°C/W

7.1 Typical Characteristic

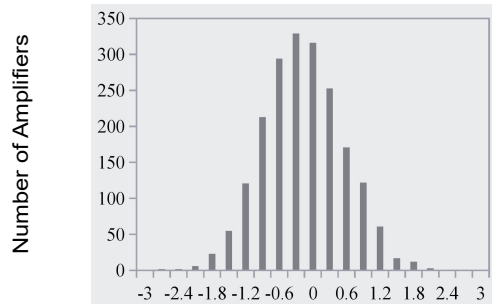


Figure 1: Input Offset Voltage Production

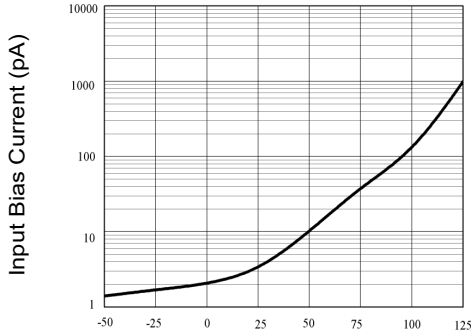


Figure 2: Input Bias Current as a Function of Temperature

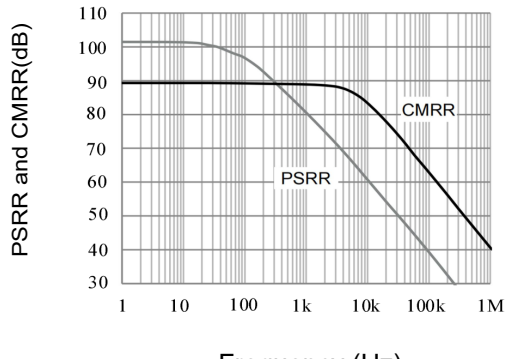


Figure 3: Power Supply and Common-mode Rejection Ratio as a Function of Frequency

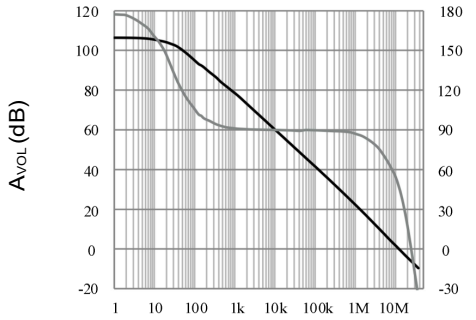


Figure 4: Open-loop Gain and Phase as a function of Frequency

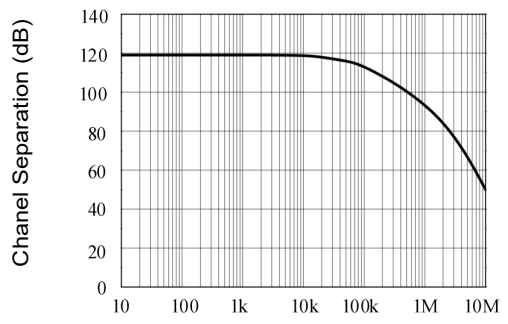


Figure 5: Channel Separation as a function of Frequency

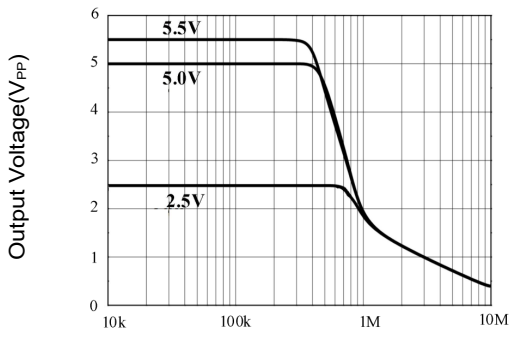


Figure 6: Maximum Output Voltage as a function of Frequency

7.2 Typical Characteristic

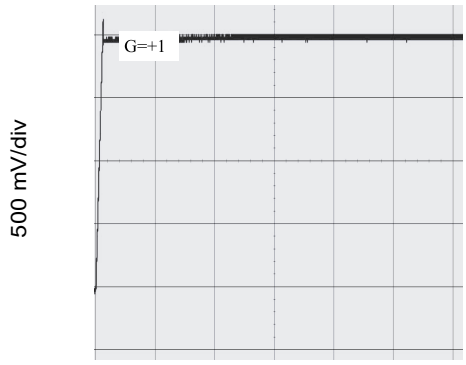


Figure 7: Large-Signal Step Response at 2.7V

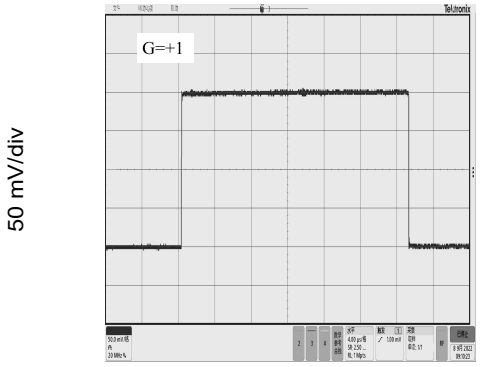


Figure 8: Small-Signal Step Response at 2.7V

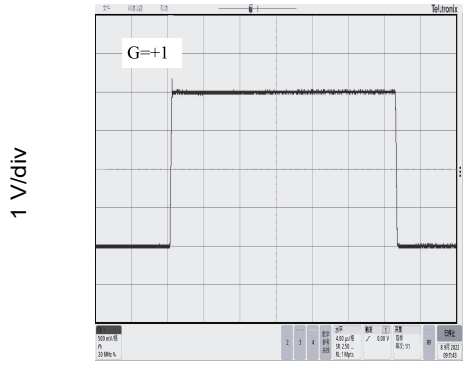


Figure 9: Large-Signal Step Response at 5V

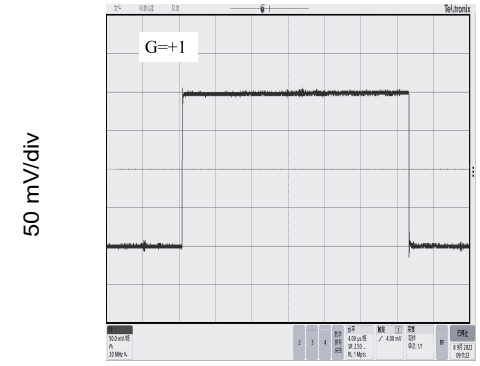


Figure 10: Small-Signal Step Response at 5V

8.Application Notes

Low Input Bias Current

The LMV72xA family is a CMOS op-amp family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 1012Ω. A 5V difference would cause 5pA of current to flow, which is greater than the LMV72xA’s input bias current at +25°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the op-amp’s –IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 11 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

a) Connect the non-inverting pin (+IN) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (-IN). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (+IN). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_S/2 or ground).

b) Connect the inverting pin (-IN) to the input with a wire that does not touch the PCB surface.

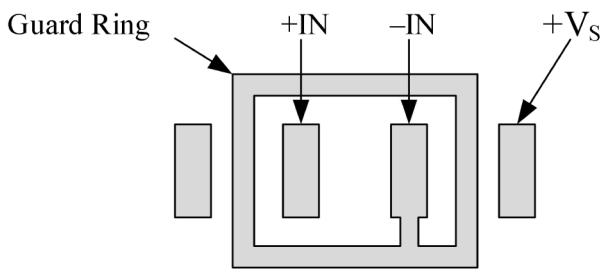


Figure 11: Use a Guard Ring around Sensitive Pins

Ground Sensing And Rail To Rail

The input common-mode voltage range of the LMV72xA series extends 300mV beyond the supply rails. This is achieved with a complementary input stage—a N-channel input differential pair in parallel with a P-channel differential pair. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op-amp. Unlike some other op-amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 12. Since the input common-mode range extends from (V_{S-} −0.1V) to (V_{S+} + 0.1V), the LMV72xA op-amps can easily perform 'true ground' sensing.

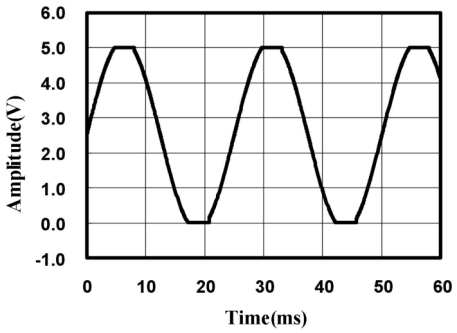


Figure 12: No Phase Inversion with Inputs Greater Than the Power-Supply Voltage

A topology of class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (e.g. 100kΩ), the output voltage can typically swing to within 5mV from the supply rails. With moderate resistive loads (e.g. 10kΩ), the output can typically swing to within 10mV from the supply rails and maintain high open-loop gain.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

Capacitive Load And Stability

The LMV72xA can directly drive 1nF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading.Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 13. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

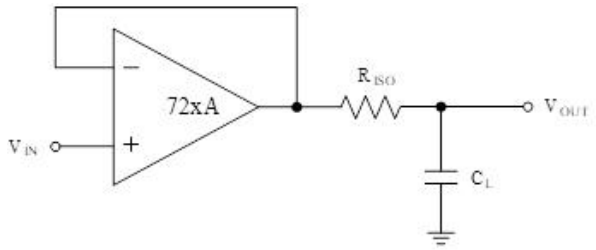


Figure 13: Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 14. It provides DC accuracy as well as AC stability. The RF provides the DC accuracy by connecting the inverting signal with the output. The C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

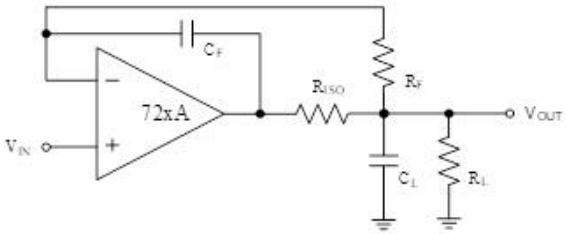


Figure 14: Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power Supply Layout And Bypass

The LMV72xA family operates from either a single +2.5V to +5.5V supply or dual ±1.25V to ±2.25V supplies. For single-supply operation, bypass the power supply V_S with a ceramic capacitor (i.e. 0.01μF to 0.1μF) which should be placed close (within 2mm for good high frequency performance) to the VS pin. For dual-supply operation both the V_{S+} and the V_{S-} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. A bulk capacitor (i.e. 2.2 μF or larger tantalum capacitor) within 100mm to provide large, slow currents and better performance. This bulk capacitor can be shared with other analog parts. Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op-amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible. For the op-amp, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

Grounding

A ground plane layer is important for the LMV72xA circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input To Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

9.Typical Application Circuits

Differential Amplifier

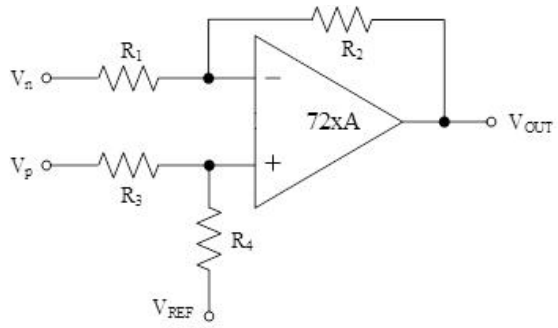
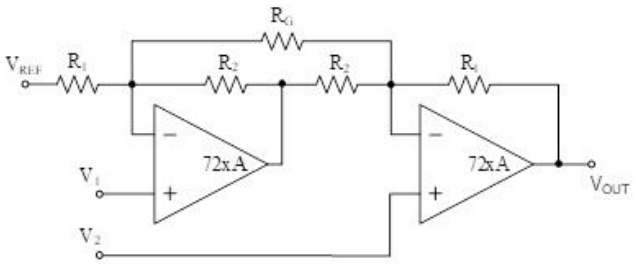


Figure 15: Differential Amplifier

The circuit shown in Figure 15 performs the difference function. If the resistors ratios are equal $R_4/R_3 = R_2/R_1$, then:

$$V_{OUT} = (V_p – V_n) \times R_2/R_1 + V_{REF}$$

Instrumentation Amplifier



$$V_{OUT}=(V_1-V_2)(1+\frac{R_1}{R_2}+\frac{2R_1}{R_G})+V_{REF}$$

Figure 16: Instrumentation Amplifier

The LMV72XA family is well suited for conditioning sensor signals in battery-powered applications. Figure 16 shows a two op-amp instrumentation amplifier, using the LMV72xA op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, the V_{REF} is typically $V_S/2$.

Buffered Chemical Sensors

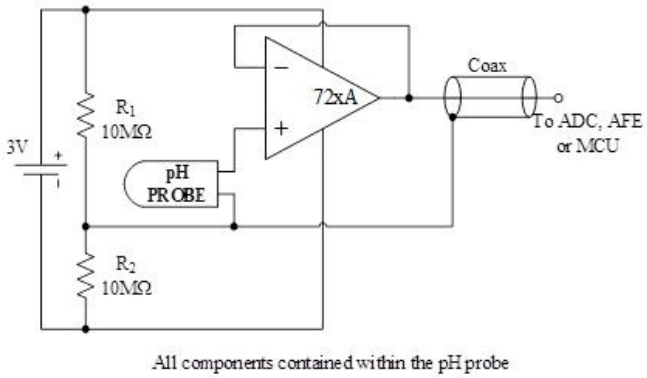


Figure 17: Buffered pH Probe

The LMV72xA family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 6 eliminates expansive low-leakage cables that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. An LMV72xA op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

Shunt-Based Current Sensing Amplifier

The current sensing amplification shown in Figure 7 has a slew rate of 2πfVPP for the output of sine wave signal, and has a slew rate of 2fVPP for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10kHz to 20kHz, and one cycle time is 100μs for a 10kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 8 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t_{SR}) due to the op-amp's slew rate, and the measurement settling time (t_{SET}). If the minimum duty cycle of the PWM is defined at 5%, and the t_{SR} is required at 20% of a total time window for a phase current monitoring, in case of a 3.3V motor control system (3.3V MCU with 12-bit ADC), the op-amp's slew rate should be more than:

$$3.3V / (100\mu s \times 5\% \times 20\%) = 3.3\ V/\mu s$$

At the same time, the op-amp's bandwidth should be much greater than the PWM frequency, like 10 time at least.

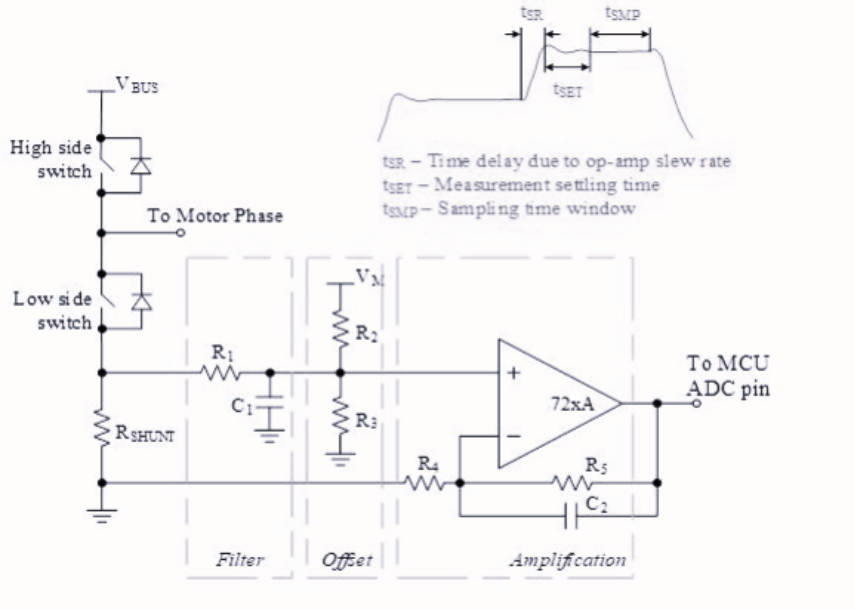
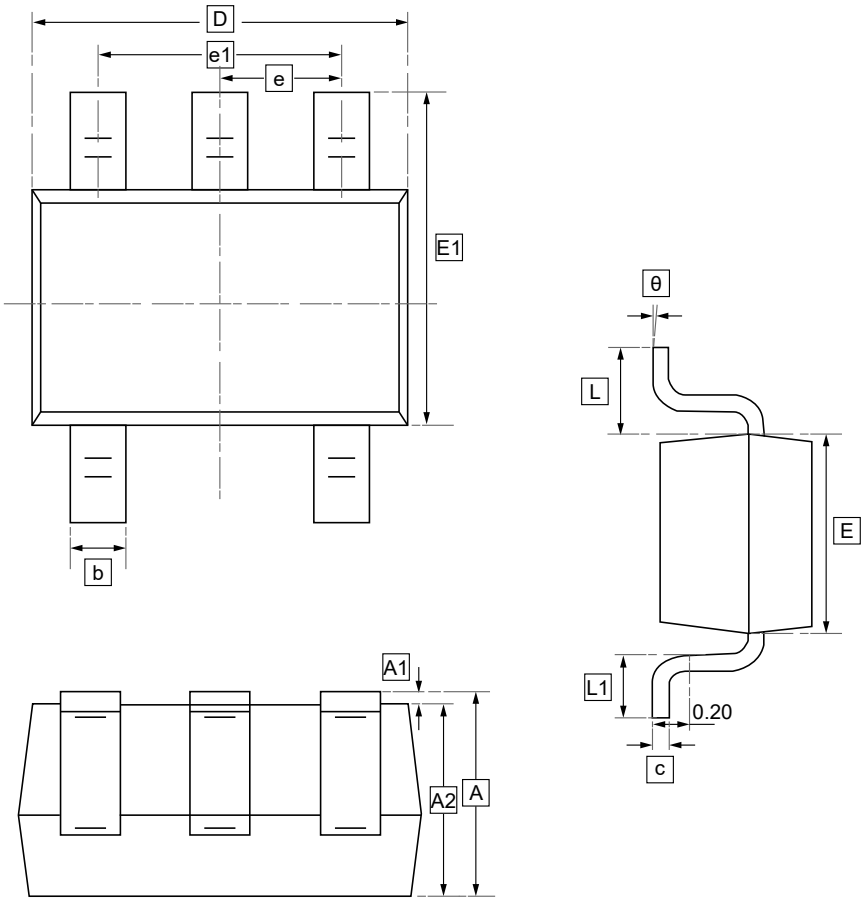


Figure 18: Current Shunt Monitor Circuit

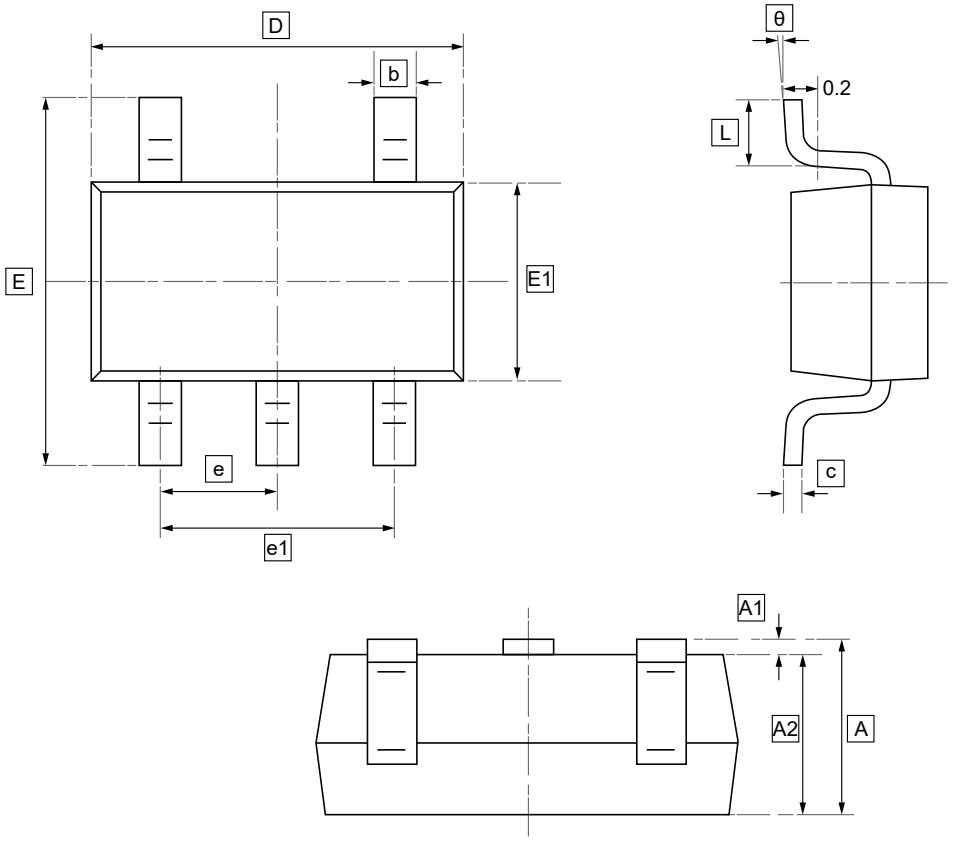
10.1 SC70-5(SOT353) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	2.05	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

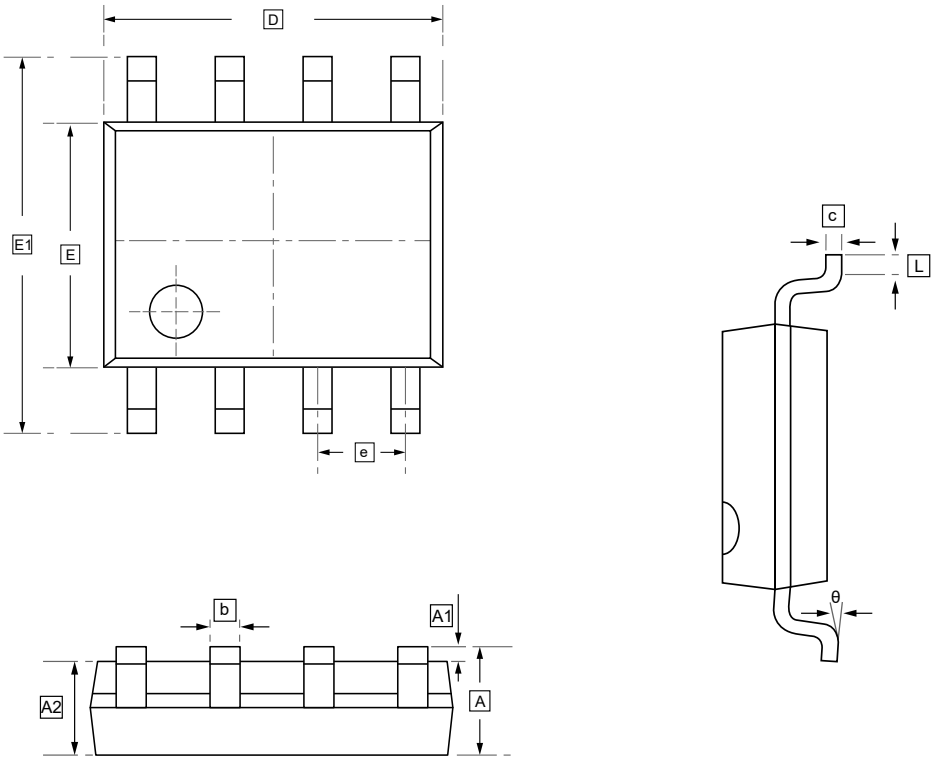
10.2 SOT-23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

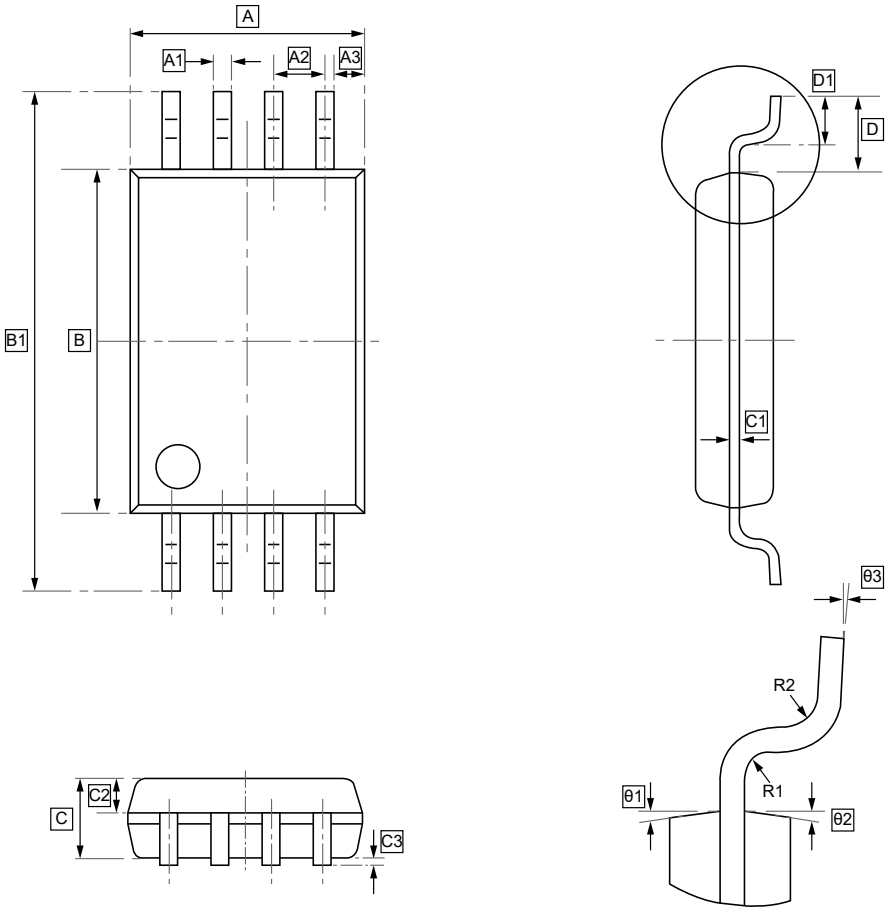
10.3 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

10.4 TSSOP-8 Package Outline Dimensions

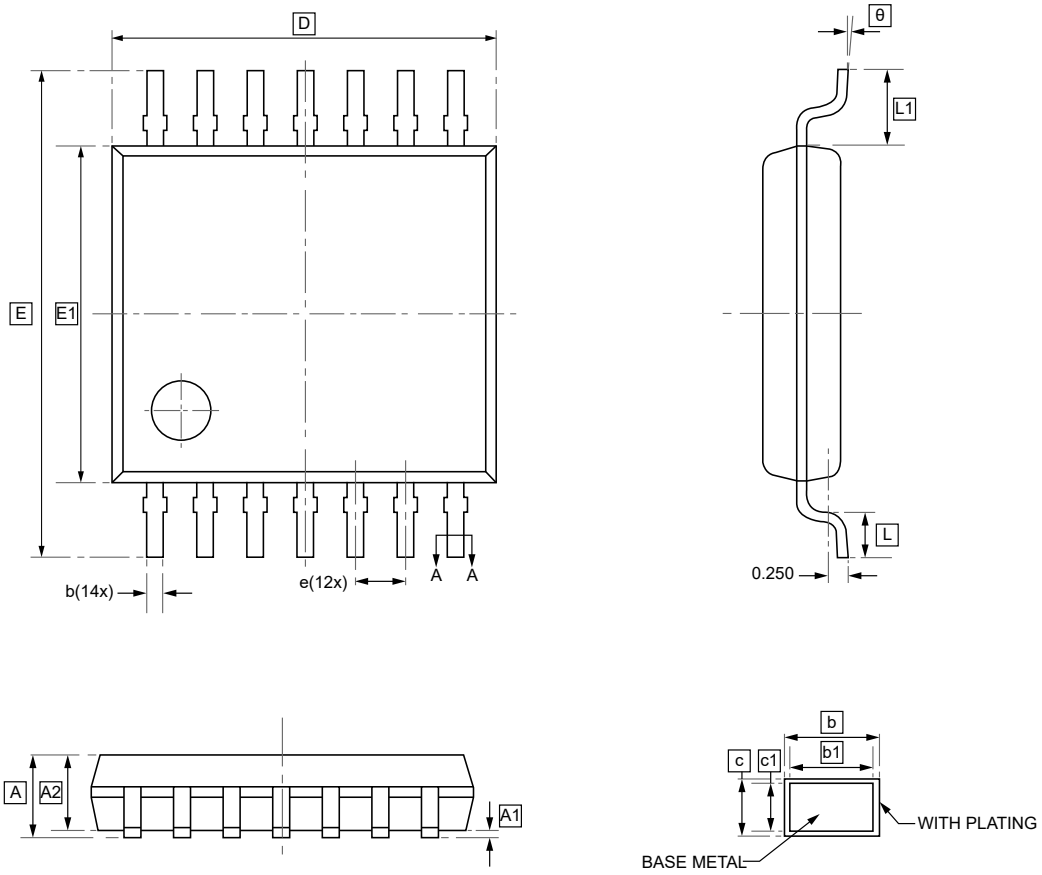


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	C2	C3	D	D1
Min	2.90	0.20	0.65	0.36	4.30	6.30	0.95	0.127	0.39	0.05	1.00	0.50
Max	3.10	0.30	TYP	0.46	4.50	6.50	1.05	TYP	0.49	0.15	REF	0.70

Symbol	R1	R2	θ1	θ2	θ3
Min	0.15	0.15	12°	12°	0°
Max	TYP	TYP	TYP4	TYP4	7°

10.5 TSSOP-14 Package Outline Dimensions

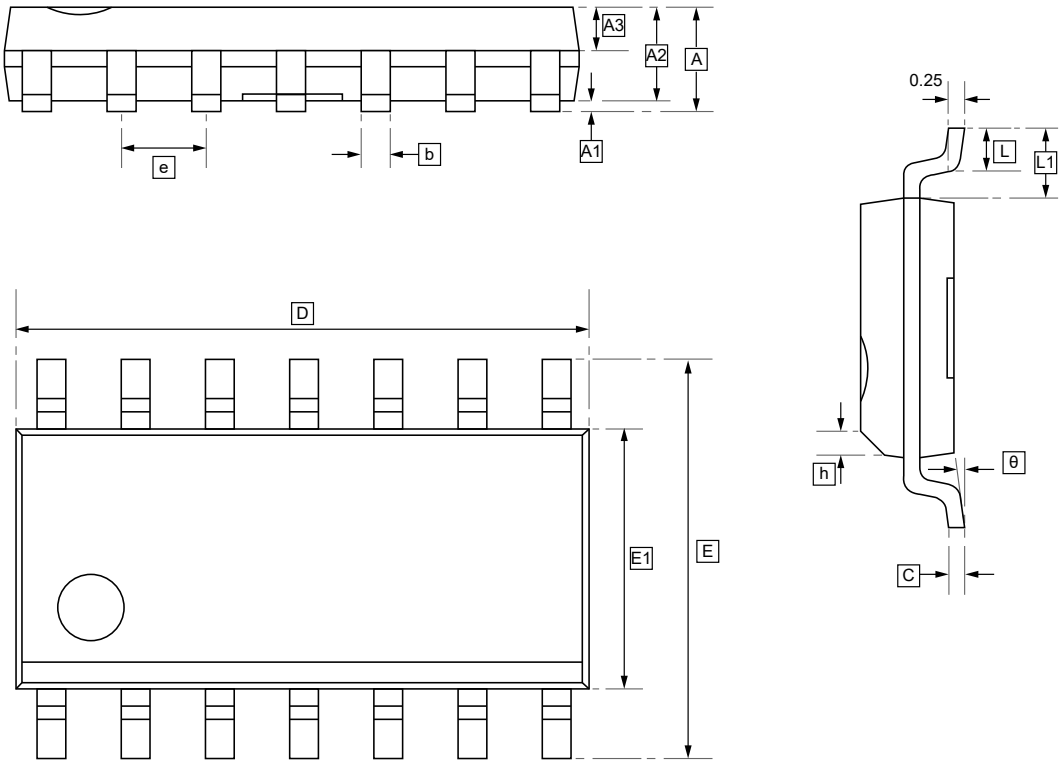


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	c1	D	E	E1	e	L1
Min	-	0.05	0.90	0.20	0.19	0.13	0.120	4.90	6.20	4.30	0.65	0.85
Max	1.20	0.15	1.05	0.28	0.25	0.17	0.14	5.10	6.60	4.50	BSC	1.15

Symbol	L	θ
Min	0.45	0°
Max	0.75	8°

10.6 SOP-14 Package Outline Dimensions

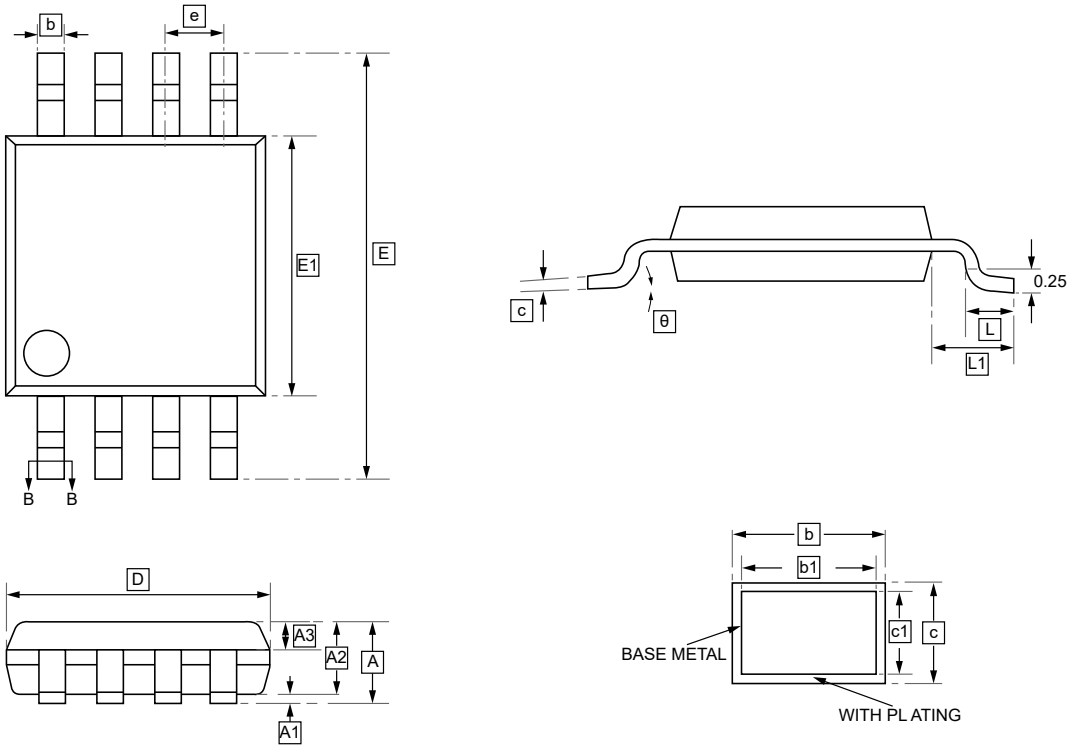


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	C	D	E	E1	e	h	L
Min	-	0.05	1.35	0.65	0.203	0.17	8.45	5.80	3.80	1.24	0.25	0.40
Max	1.75	0.25	1.55	0.75	0.305	0.25	8.85	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

10.7 MSOP-8 Package Outline Dimensions



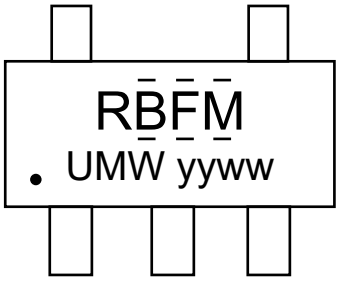
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	b1	c	c1	D	E	E1	e
Min	-	0.05	0.75	0.30	0.28	0.27	0.15	0.14	2.90	4.70	2.90	0.65
Max	1.10	0.15	0.95	0.40	0.36	0.33	0.19	0.16	3.10	5.10	3.10	BSC

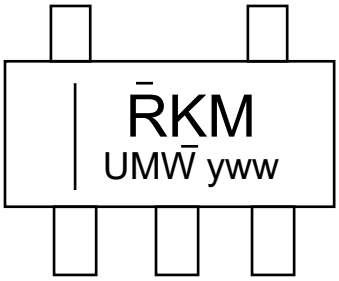
Symbol	L	L1	θ
Min	0.40	0.95	0°
Max	0.70	REF	8°

11.Ordering information

SOT23-5

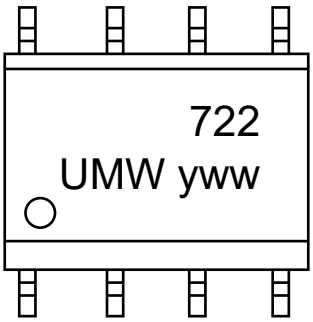


SC70-5

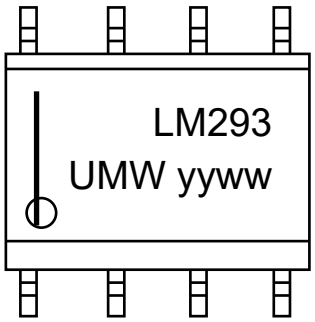


TSSOP-14

TSSOP-8



SOP-8



y: Year Code
yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW LMV721IDCKR	RKM	SC70-5	3000	Tape and reel
UMW LMV721IDBVR	RBFM	SOT23-5	3000	Tape and reel
UMW LMV722IDR	LMV722	SOP-8	2500	Tape and reel
UMW LMV722MT	722	TSSOP-8	4000	Tape and reel
UMW LMV722MM	722	MSOP-8	4000	Tape and reel
UMW LMV724M	LMV724	SOP-14	2500	Tape and reel
UMW LMV724MT	LMV724	TSSOP-14	4000	Tape and reel

12.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.