

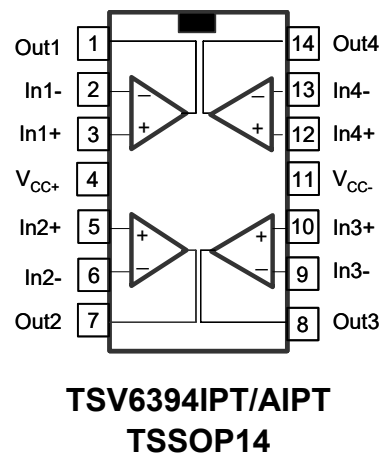
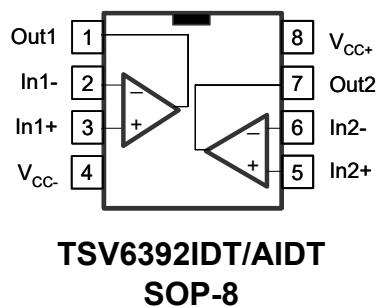
1.Description

The UMW TSV639x series of dual and quad operational amplifiers (op amps) offers low voltage operation and rail-to-rail input and output. For applications configured with gain, UMW TSV639x series offers an excellent speed/power consumption ratio, 2.4 MHz gain bandwidth product while consuming only 60 μ A at 5 V. The devices also feature an ultra-low input bias current and have a shutdown mode (UMW TSV6393, UMW TSV6395). These features make the TSV639x family ideal for sensor interfaces, battery supplied and portable applications, as well as active filtering.

3.Applications

- Battery-powered applications
- Portable devices
- Signal conditioning

4.Pinning information



2.Features

- Rail-to-rail input and output
- Low power consumption: 60 μ A typ at 5V
- Low supply voltage: 1.5 – 5.5V
- Gain bandwidth product: 2.4 MHz typ, stable
- for gain equal or above -3 or 4
- Low-power shutdown mode: 5 nA typ
- Low offset voltage: 800 μ V max (A version)
- Low input bias current: 1 pA typ
- EMI hardened operational amplifiers
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40°C to 125°C

- Active filtering
- Medical instrumentation



5. Absolute Maximum Ratings

Parameter		Symbol	Value	Units
Supply voltage ⁽¹⁾		V _{CC}	6	V
Differential input voltage ⁽²⁾		V _{id}	±V _{CC}	V
Input voltage ⁽³⁾		V _{in}	(V _{CC-})-0.2 to (V _{CC+})+0.2	V
Input current ⁽⁴⁾		I _{in}	10	mA
Shutdown voltage ⁽³⁾		$\overline{\text{SHDN}}$	(V _{CC-})-0.2 to (V _{CC+})+0.2	V
Storage temperature		T _{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient ⁽⁵⁾⁽⁶⁾	SOP-8	R _{thja}	125	°C/W
	TSSOP-14		100	°C/W
Maximum junction temperature		T _J	150	°C
HBM: human body model ⁽⁷⁾		ESD	4	kV
MM: machine model ⁽⁸⁾			300	V
CDM: charged device model ⁽⁹⁾			1.5	kV
Latch-up immunity			200	mA

Notes:

- (1) All voltage values, except differential voltage, are with respect to network ground terminal.
- (2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- (3) $V_{CC} - V_{in}$ must not exceed 6 V, V_{in} must not exceed 6 V.
- (4) Input current must be limited by a resistor in series with the inputs.
- (5) Short-circuits can cause excessive heating and destructive dissipation.
- (6) R_{th} are typical values.
- (7) Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- (8) Machine mode: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
- (9) Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.



6. Operating conditions

Parameter	Symbol	Rating	Units
Supply voltage	V_{CC}	1.5 to 5.5	V
Common mode input voltage range	V_{icm}	$(V_{CC-})-0.1$ to $(V_{CC+})+0.1$	V
Operating free air temperature range	T_{oper}	40 to +125	°C



7.1 DC Electrical Characteristics

(V_{CC+})=1.8V with (V_{CC-})=0V, $V_{icm}=V_{CC}/2$, $T_{amb}=25^{\circ}\text{C}$, and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset voltage	V _{io}	UMW TSV639x			3	mV
		UMW TSV639xA			0.8	mV
		T _{min} <T _{op} <T _{max} , UMW TSV639x			4.5	mV
		T _{min} <T _{op} <T _{max} , UMW TSV639xA			2	mV
Input offset voltage drift	DV _{io}			2		μV/°C
Input offset current, V _{out} =V _{CC} /2	I _{io}	T _{min} <T _{op} <T _{max}		1	10 ⁽¹⁾	pA
				1	100	pA
Input bias current, V _{out} =V _{CC} /2	I _{ib}	T _{min} <T _{op} <T _{max}		1	10 ⁽¹⁾	pA
				1	100	pA
Common mode rejection ratio, 20 log (ΔV _{ic} /ΔV _{io})	CMR	0V to 1.8V, V _{out} =0.9V	53	74		dB
		T _{min} <T _{op} <T _{max}	51			dB
Large signal voltage gain	A _{vd}	R _L =10kΩ, V _{out} =0.5V to 1.3V	85	95		dB
		T _{min} <T _{op} <T _{max}	80			dB
High-level output voltage (V _{OH} =V _{CC} -V _{OUT})	V _{OH}	R _L =10kΩ		5	35	mV
		T _{min} <T _{op} <T _{max}			50	mV
Low-level output voltage	V _{OL}	R _L =10kΩ		4	35	mV
		T _{min} <T _{op} <T _{max}			50	mV
Isink	I _{OUT}	V _{out} =1.8V	6	12		mA
		T _{min} <T _{op} <T _{max}	4			mA
Isource		V _{out} =0V	6	10		mA
		T _{min} <T _{op} <T _{max}	4			mA
Supply current (per operator)	I _{CC}	No load, V _{out} =V _{CC} /2	40	50	60	μA
		T _{min} <T _{op} <T _{max}			62	μA



Parameter	Symbol	Conditions	Min	Typ	Max	Units
AC performance						
Gain bandwidth product	GBP	$R_L=10k\Omega$, $C_L=100pF$		2		MHz
Minimum gain for stability	Gain	Phase margin=60°, $R_f=10k\Omega$, $R_L=10k\Omega$, $C_L=20pF$		4		V/V
				-3		V/V
Slew rate	SR	$R_L=10k\Omega$, $C_L=100pF$ $V_{out}=0.5V$ to $1.3V$		0.7		V/ μs
Equivalent input noise voltage	e_n	$f=1kHz$		60		nV/ $\sqrt{Hz}$
		$f=10kHz$		33		nV/ $\sqrt{Hz}$

1. Guaranteed by design.

7.2 DC Electrical Characteristics

Shutdown characteristics $V_{CC}=1.8V$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current in shutdown mode (all operators)	I_{CC}	$\overline{SHDN}=V_{CC-}$		2.5	50	nA
		$T_{min}<T_{op}<85^\circ C$			200	nA
		$T_{min}<T_{op}<125^\circ C$			1.5	μA
Amplifier turn-on time	t_{on}	$R_L=2k\Omega$, $V_{out}=V_{CC-}$ to $V_{CC-} + 0.2V$		200		ns
Amplifier turn-off time	t_{off}	$R_L=2k\Omega$, $V_{out}=V_{CC+} - 0.5V$ to $V_{CC+} - 0.7V$		20		ns
$\overline{SHDN}$ logic high	V_{IH}		1.35			V
$\overline{SHDN}$ logic low	V_{IL}				0.6	V
$\overline{SHDN}$ current high	I_{IH}	$\overline{SHDN}=V_{CC+}$		10		pA
$\overline{SHDN}$ current low	I_{IL}	$\overline{SHDN}=V_{CC-}$		10		pA
Output leakage in shutdown mode	I_{OLeak}	$\overline{SHDN}=V_{CC-}$		50		pA
		$T_{min}<T_{op}<125^\circ C$		1		nA



7.3 DC Electrical Characteristics

(V_{CC+})=3.3V with (V_{CC-})=0V, $V_{icm}=V_{CC}/2$, $T_{amb}=25^{\circ}\text{C}$, and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset voltage	V _{io}	UMW TSV639x			3	mV
		UMW TSV639xA			0.8	mV
		T _{min} <T _{op} <T _{max} , UMW TSV639x			4.5	mV
		T _{min} <T _{op} <T _{max} , UMW TSV639xA			2	mV
Input offset voltage drift	DV _{io}			2		μV/°C
Input offset current	I _{io}	T _{min} <T _{op} <T _{max}		1	10 ⁽¹⁾	pA
				1	100	pA
Input bias current	I _{ib}	T _{min} <T _{op} <T _{max}		1	10 ⁽¹⁾	pA
				1	100	pA
Common mode rejection ratio, 20 log (ΔV _{ic} /ΔV _{io})	CMR	0V to 3.3V, V _{out} =1.65V	57	79		dB
		T _{min} <T _{op} <T _{max}	53			dB
Large signal voltage gain	A _{vd}	R _L =10kΩ, V _{out} =0.5V to 2.8V	88	98		dB
		T _{min} <T _{op} <T _{max}	83			dB
High-level output voltage (V _{OH} =V _{CC} -V _{OUT})	V _{OH}	R _L =10kΩ		6	35	mV
		T _{min} <T _{op} <T _{max}			50	mV
Low-level output voltage	V _{OL}	R _L =10kΩ		7	35	mV
		T _{min} <T _{op} <T _{max}			50	mV
Isink	I _{OUT}	V _O =3.3V	23	45		mA
		T _{min} <T _{op} <T _{max}	20			mA
Isource		V _O =0V	23	38		mA
		T _{min} <T _{op} <T _{max}	20			mA
Supply current (per operator)	I _{CC}	No load, V _{out} =1.75V	43	55	64	μA
		T _{min} <T _{op} <T _{max}			66	μA



Parameter	Symbol	Conditions	Min	Typ	Max	Units
AC performance						
Gain bandwidth product	GBP	$R_L=10k\Omega$, $C_L=100pF$		2.2		MHz
Minimum gain for stability	Gain	Phase margin=60°, $R_f=10k\Omega$, $R_L=10k\Omega$, $C_L=20pF$		4		V/V
				-3		V/V
Slew rate	SR	$R_L=10k\Omega$, $C_L=100pF$ $V_{out}=0.5V$ to $2.8V$		0.9		V/ μs

1. Guaranteed by design.



7.4 DC Electrical Characteristics

(V_{CC+})=5V with (V_{CC-})=0V, $V_{icm}=V_{CC}/2$, $T_{amb}=25^{\circ}\text{C}$, and R_L connected to $V_{CC}/2$ (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset voltage	V_{io}	UMW TSV639x			3	mV
		UMW TSV639xA			0.8	mV
		$T_{min}<T_{op}<T_{max}$, UMW TSV639x			4.5	mV
		$T_{min}<T_{op}<T_{max}$, UMW TSV639xA			2	mV
Input offset voltage drift	DV_{io}			2		$\mu\text{V}/^{\circ}\text{C}$
Input offset current, $V_{out}=V_{CC}/2$	I_{io}	$T_{min}<T_{op}<T_{max}$		1	$10^{(1)}$	pA
				1	100	pA
Input bias current, $V_{out}=V_{CC}/2$	I_{ib}	$T_{min}<T_{op}<T_{max}$		1	$10^{(1)}$	pA
				1	100	pA
Common mode rejection ratio, $20 \log (\Delta V_{io}/\Delta V_{io})$	CMR	0V to 5V, $V_{out}=2.5\text{V}$	60	80		dB
		$T_{min}<T_{op}<T_{max}$	55			dB
Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	SVR	$V_{CC}=1.8$ to 5V	75	93		dB
		$T_{min}<T_{op}<T_{max}$	73			dB
Large signal voltage gain	A_{vd}	$R_L=10\text{k}\Omega$, $V_{out}=0.5\text{V}$ to 4.5V	89	98		dB
		$T_{min}<T_{op}<T_{max}$	84			dB
EMI rejection ratio $\text{EMIRR}=-20 \log (V_{RFpeak}/\Delta V_{io})$	EMIRR	$V_{RF}=100\text{mV}_{rms}$, $f=400\text{MHz}$		61		dB
		$V_{RF}=100\text{mV}_{rms}$, $f=900\text{MHz}$		85		dB
		$V_{RF}=100\text{mV}_{rms}$, $f=1800\text{MHz}$		92		dB
		$V_{RF}=100\text{mV}_{rms}$, $f=2400\text{MHz}$		83		dB
High level output voltage ($V_{OH}=V_{CC}-V_{OUT}$)	V_{OH}	$R_L=10\text{k}\Omega$		7	35	mV
		$T_{min}<T_{op}<T_{max}$			50	mV
Low level output voltage	V_{OL}	$R_L=10\text{k}\Omega$		6	35	mV
		$T_{min}<T_{op}<T_{max}$			50	mV



Parameter	Symbol	Conditions	Min	Typ	Max	Units
I_{sink}	I_{OUT}	$V_{\text{O}}=5\text{V}$	40	65		mA
		$T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$	35			mA
I_{source}		$V_{\text{O}}=0\text{V}$	40	72		mA
		$T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$	35			mA
Supply current (per operator)	I_{CC}	No load, $V_{\text{out}}=2.5\text{V}$	50	60	69	μA
		$T_{\text{min}} < T_{\text{op}} < T_{\text{max}}$			72	μA
AC performance						
Gain bandwidth product	GBP	$R_{\text{L}}=10\text{k}\Omega$, $C_{\text{L}}=100\text{pF}$		2.4		MHz
Minimum gain for stability	Gain	Phase margin=60°, $R_{\text{f}}=10\text{k}\Omega$, $R_{\text{L}}=10\text{k}\Omega$, $C_{\text{L}}=20\text{pF}$, $T_{\text{op}}=25^{\circ}\text{C}$		4		V/V
				-3		V/V
Slew rate	SR	$R_{\text{L}}=10\text{k}\Omega$, $C_{\text{L}}=100\text{pF}$ $V_{\text{out}}=0.5\text{V}$ to 2.8V		1.1		V/ μs
Equivalent input noise voltage	e_{n}	$f=1\text{kHz}$		60		nV/ $\sqrt{\text{Hz}}$
		$f=10\text{kHz}$		33		nV/ $\sqrt{\text{Hz}}$
Total harmonic distortion + noise	THD+N	$V_{\text{CC}}=5\text{V}$, $f_{\text{in}}=1\text{kHz}$, $A_{\text{CL}}=-10$, $R_{\text{L}}=100\text{k}\Omega$ $V_{\text{icm}}=V_{\text{CC}}/2$, $\text{BW}=22\text{kHz}$, $V_{\text{out}}=1V_{\text{rms}}$		0.015		%

1. Guaranteed by design.



7.5 DC Electrical Characteristics

Shutdown characteristics $V_{CC}=5V$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current in shutdown mode (all operators)	I_{CC}	$\overline{SHDN}=V_{IL}$		5	50	nA
		$T_{min}<T_{op}<85^{\circ}C$			200	nA
		$T_{min}<T_{op}<125^{\circ}C$			1.5	μA
Amplifier turn-on time	t_{on}	$R_L=2k\Omega$, $V_{out}=V_{CC-}$ to $V_{CC-} + 0.2V$		200		ns
Amplifier turn-off time	t_{off}	$R_L=2k\Omega$, $V_{out}=V_{CC+} -0.5V$ to $V_{CC+} -0.7V$		20		ns
$\overline{SHDN}$ logic high	V_{IH}		2			V
$\overline{SHDN}$ logic low	V_{IL}				0.8	V
$\overline{SHDN}$ current high	I_{IH}	$\overline{SHDN}=V_{CC+}$		10		pA
$\overline{SHDN}$ current low	I_{IL}	$\overline{SHDN}=V_{CC-}$		10		pA
Output leakage in shutdown mode	I_{OLeak}	$\overline{SHDN}=V_{CC-}$		50		pA
		$T_{min}<T_{op}<125^{\circ}C$		1		nA



8.1 Typical characteristic

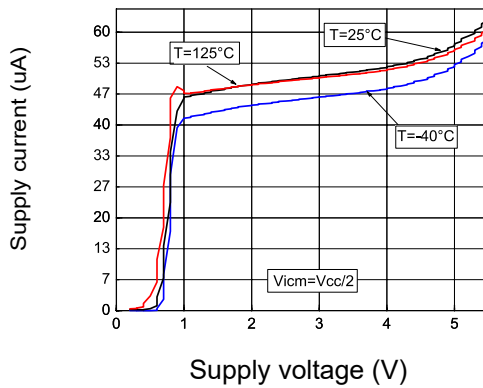


Figure 1: Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

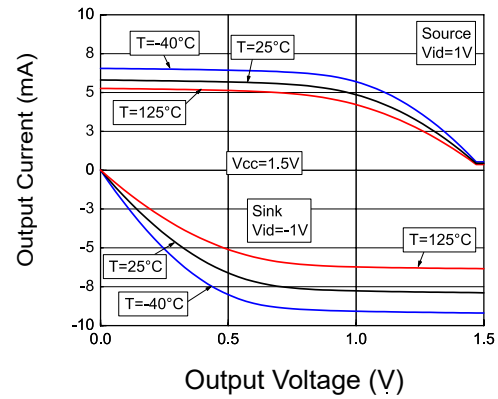


Figure 2: Output current vs. output voltage at $V_{CC} = 1.5V$

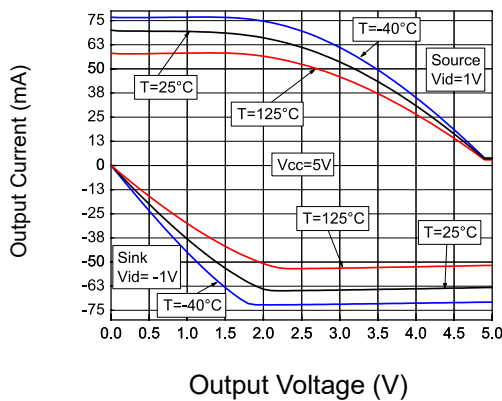


Figure 3: Output current vs. output voltage at $V_{CC} = 5V$

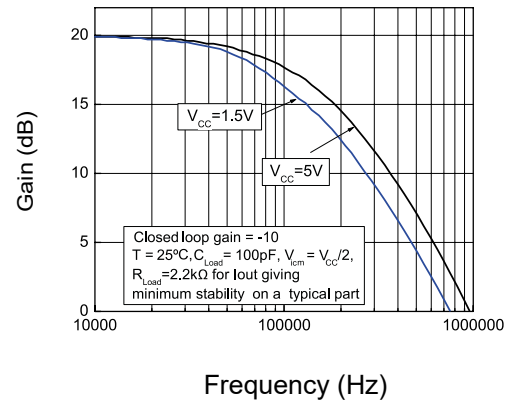


Figure 4: Peaking at closed loop gain = -10 at $V_{CC} = 1.5V$ and $V_{CC} = 5V$

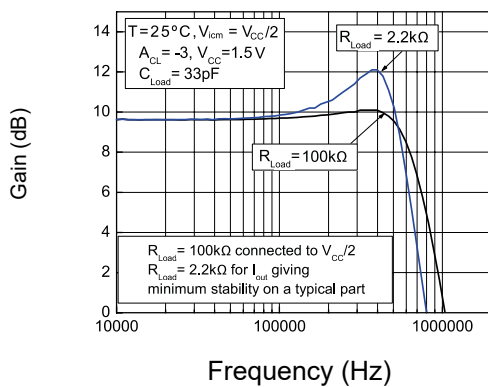


Figure 5: Peaking at closed loop gain = -3, $V_{CC} = 1.5V$

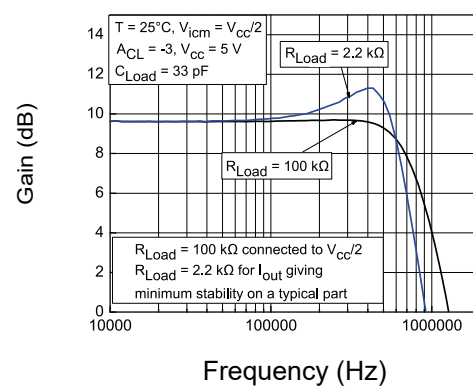


Figure 6: Peaking at closed loop gain = -3, $V_{CC} = 5V$



8.2 Typical characteristic

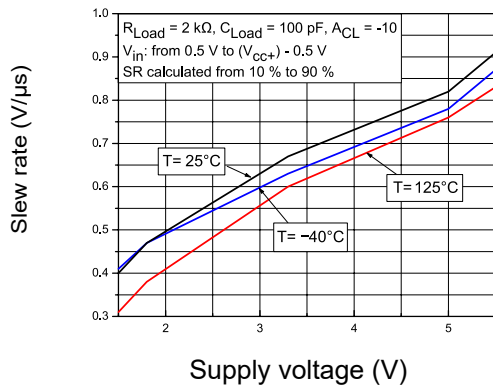


Figure 7: Positive slew rate vs. supply voltage in closed loop

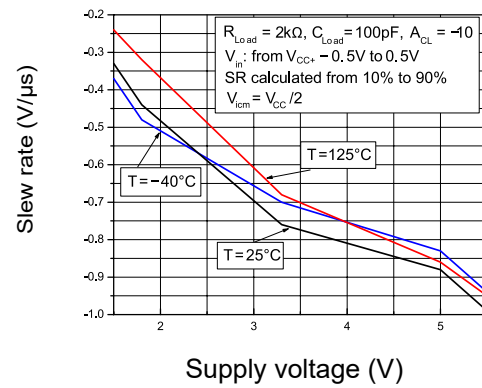


Figure 8: Negative slew rate vs. supply voltage in closed loop

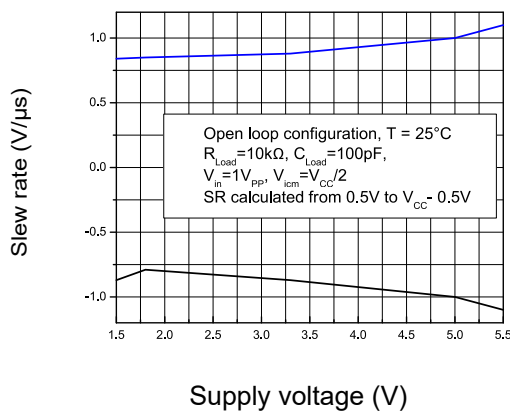


Figure 9: Slew rate vs. supply voltage in open loop

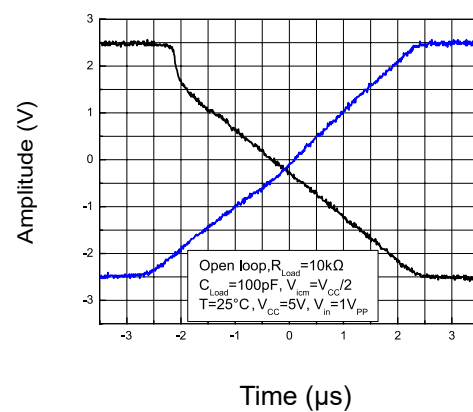


Figure 10: Slew rate timing in open loop

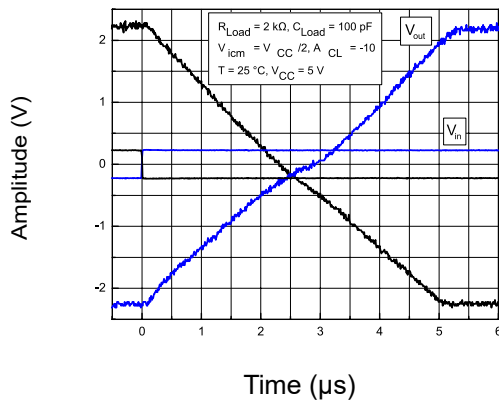


Figure 11: Slew rate timing in closed loop

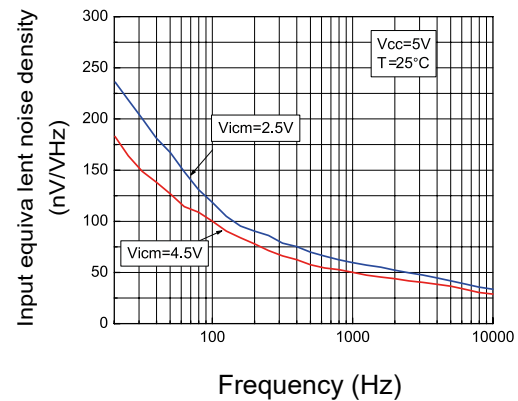


Figure 12: Noise vs. frequency



8.3 Typical characteristic

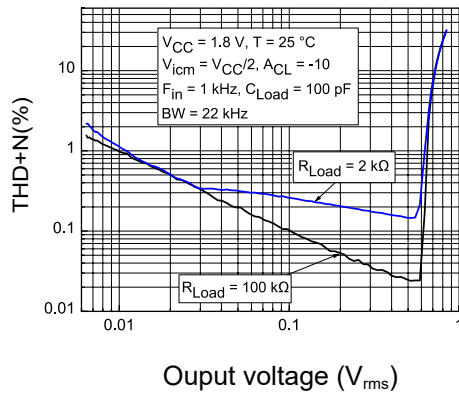


Figure 13: Distortion + noise vs. output voltage at $V_{CC}=1.8\text{V}$

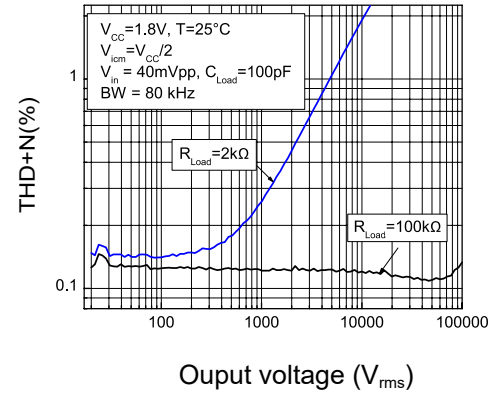


Figure 14: Distortion and noise vs. frequency at $V_{CC}=1.8\text{V}$

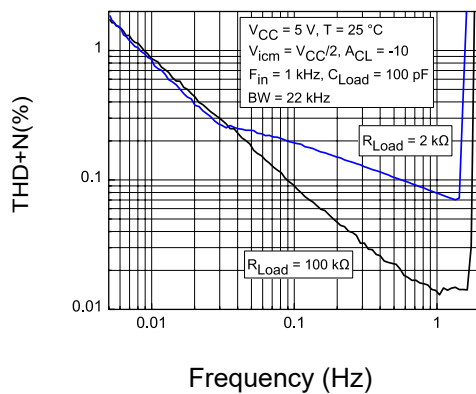


Figure 15: Distortion + noise vs. output voltage at $V_{CC}=5\text{V}$

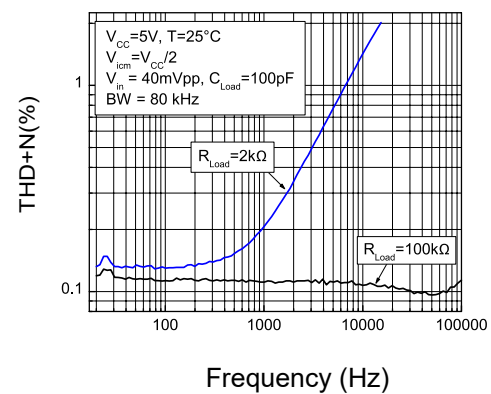


Figure 16: Distortion + noise vs. frequency at $V_{CC}=5\text{V}$

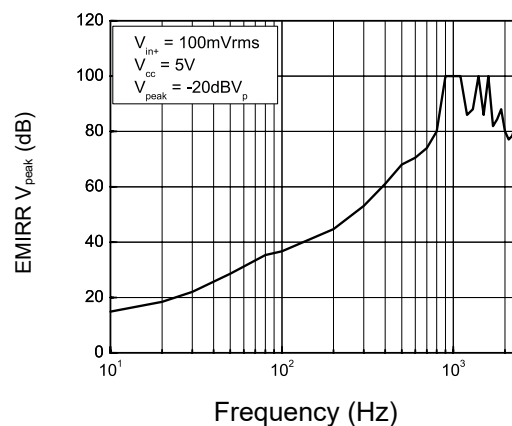


Figure 17: EMIRR vs. frequency at $V_{CC}=5\text{V}$, $T=25^\circ\text{C}$



8.4 Typical characteristic

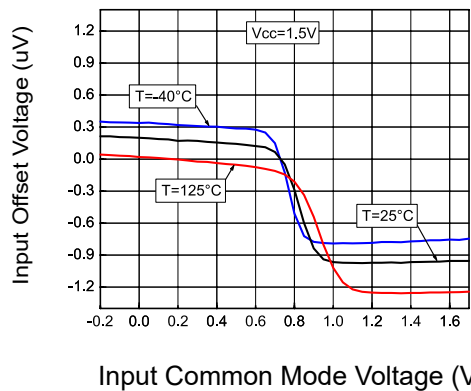


Figure 18: Input offset voltage vs input common mode at $V_{CC}=1.5V$

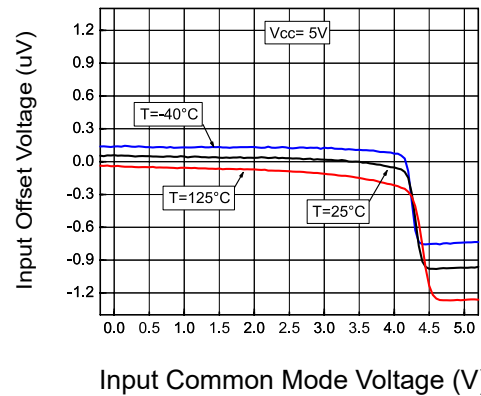


Figure 19: Input offset voltage vs input common mode at $V_{CC}=5V$

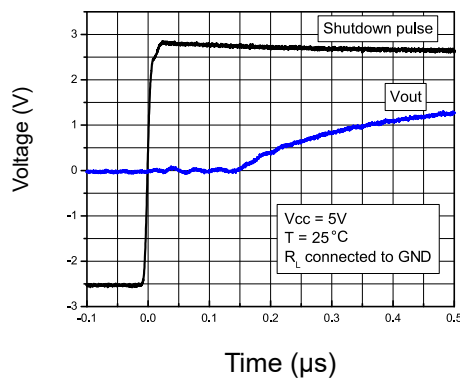


Figure 20: Turn-on time, $V_{CC}=5V$, V_{out} pulled down, $T=25^{\circ}C$

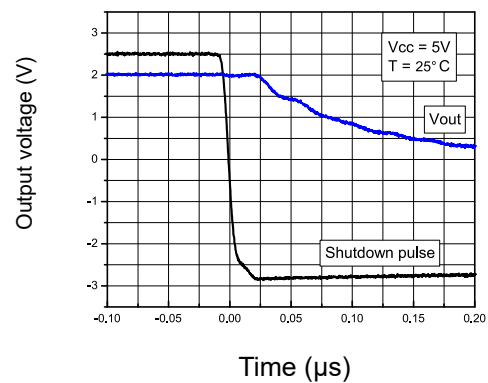


Figure 21: Turn-off time, $V_{CC}=5V$, V_{out} pulled down, $T=25^{\circ}C$

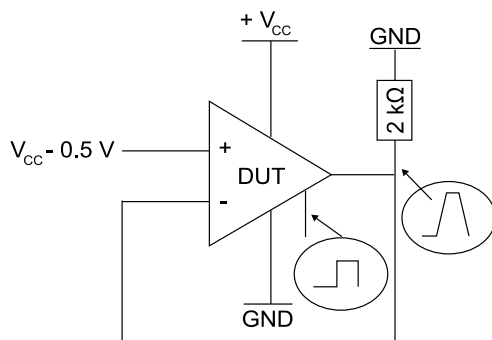


Figure 21: Test configuration for turn-on time (V_{out} pulled down)

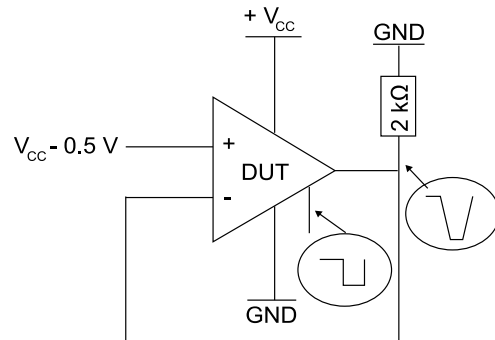
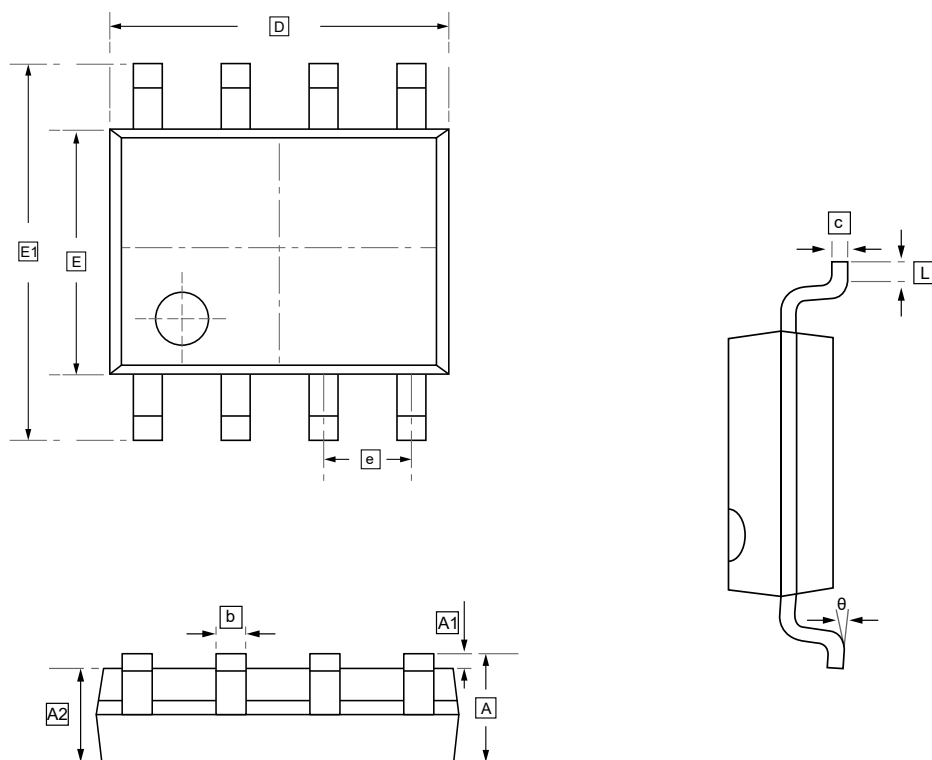


Figure 21: Test configuration for turn-off time (V_{out} pulled down)



9.1 SOP-8 Package Outline Dimensions

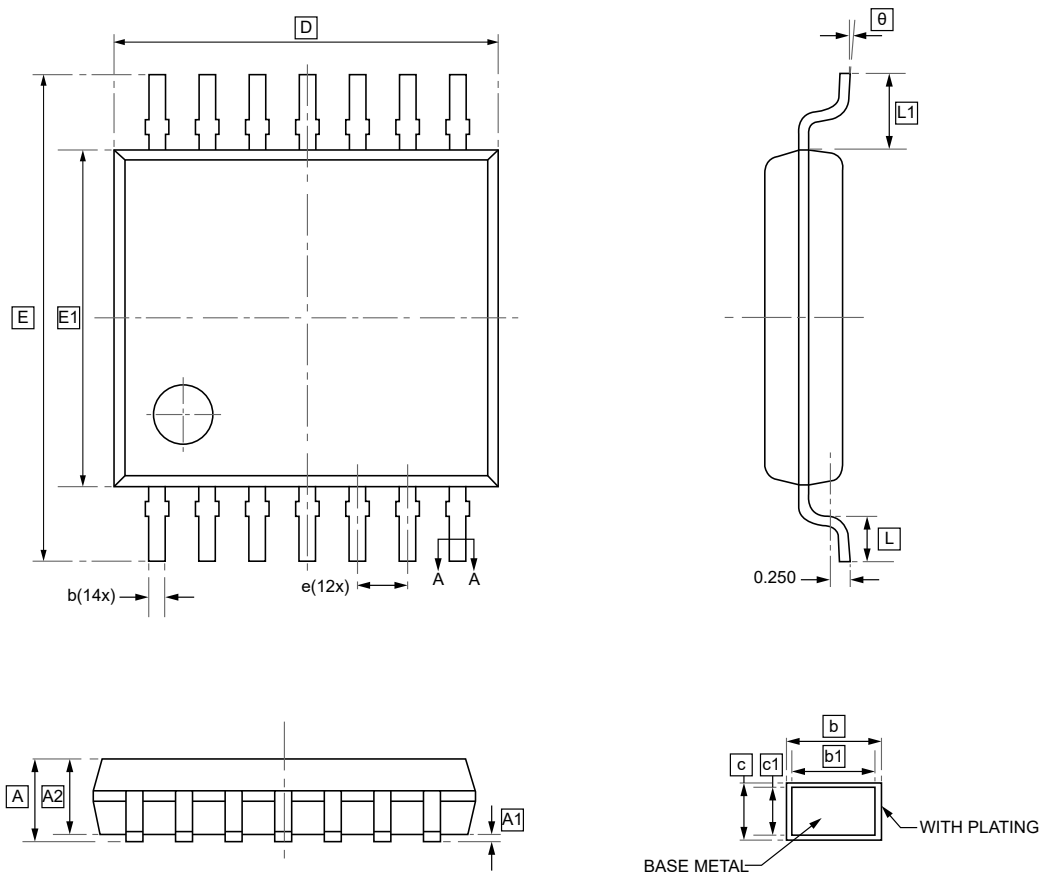


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°



9.2 TSSOP-14 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

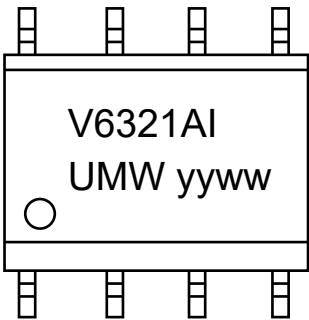
Symbol	A	A1	A2	b	b1	c	c1	D	E	E1	e	L1
Min	-	0.05	0.90	0.20	0.19	0.13	0.120	4.90	6.20	4.30	0.65	0.85
Max	1.20	0.15	1.05	0.28	0.25	0.17	0.14	5.10	6.60	4.50	BSC	1.15

Symbol	L	θ
Min	0.45	0°
Max	0.75	8°

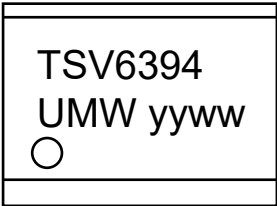


10.Ordering information

SOP-8



TSSOP-14



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW TSV6392AIDT	V632AI	SOP-8	2500	Tape and reel
UMW TSV6392IDT	V6392I	SOP-8	2500	Tape and reel
UMW TSV6394IPT	TSV6394	TSSOP-14	4000	Tape and reel
UMW TSV6394AIPT	TSV6394	TSSOP-14	4000	Tape and reel



11.Disclaimer

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