UMW OPA4388

Precision, Zero-Drift, Zero-Crossover, True Rail-To-Rail Input and Output Operational Amplifiers

1.Description

The OPA4388 series of precision operational amplifiers are ultra-low noise, fast settling, zero-drift, zero-crossover devices that achieve rail-to-rail input and output operation. These features and excellent AC performance are combined with a dropout of only 0.25μV.The combination of adjustable voltage and 0.005μV/°C temperature drift makes the OPA4388 an ideal choice for driving high-precision analog-to-digital converters (ADCs) or buffering high-resolution digital-to-analog converters (DACs). The design provides excellent performance when driving analog-to-digital converters (ADCs) without sacrificing linearity.

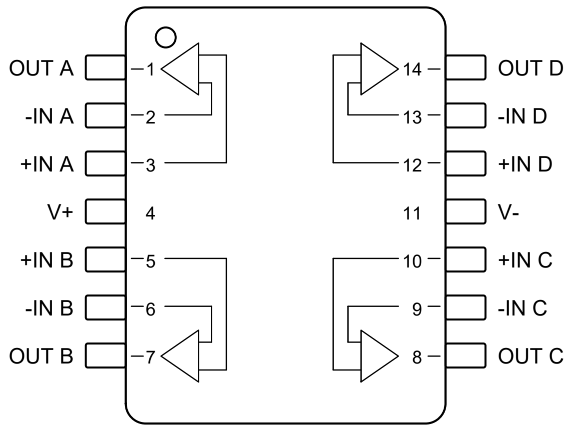
2.Features

- Ultra-Low Offset Voltage: ±0.25μV
- Zero Drift: ±0.005μV°C
- Zero Crossover: 140dB CMRR True RRIO
- Low Noise: 7.0nV√Hz (at 1kHz)
- No 1f Noise: 140nV$_{PP}$ (0.1Hz to 10Hz)
- Fast Settling: 2μs (1V, 0.01%)
- Gain Bandwidth: 10MHz
- Single Supply: 2.5V to 5.5V
- Dual power supply: ±1.25V to ±2.75V
- True Rail-to-Rail Input and Output
- EMI RFI Filter Input

3.Applications

- Commercial Network and Server PSU
- Laptop Power Adapter Designs
- Weighing Scales
- Lab and Field Instruments
- Battery Testing
- Electronic Thermometers
- Temperature Transmitters

4.Pinning Information



SOP-14 (D) and TSSOP-14 (PW) Packages, Top View

Pin Functions: OPA4388

Name	SOP-14/TSSOP-14	I/O	Description
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
-IN C	9	I	Inverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

5.Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter			Min	Max	Units
Supply voltage	V_S=(V+) - (V-)	Single-supply		6	V
		Dual-supply		±3	V
Signal input pins	Voltage	Common-mode	(V-) - 0.5	(V+) + 0.5	V
		Differential		(V+) - (V-) + 0.2	V
	Current			±10	mA
Output short circuit (2)			Continuous	Continuous	
Temperature	Operating, T_A		-55	150	°C
	Junction, T_J			150	°C
	Storage, T_{STG}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

6.ESD Ratings

		Value	Units
Electrostatic Discharge, $V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

7.Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Min	Max	Units
Supply voltage, V_S=(V+) - (V-)	Single-supply	2.5	5.5	V
	Dual-supply	±1.25	±2.75	V
Specified temperature		-40	125	°C

8.Thermal Information

Thermal Metric (1)	Symbol	(SOP) 14 Pins	(TSSOP) 14 Pins	Units
Junction-to-ambient thermal resistance	$R_{θJA}$	86.4	109.6	°C/W
Junction-to-case (top) thermal resistance	$R_{θJC(top)}$	46.3	27.4	°C/W
Junction-to-board thermal resistance	$R_{θJB}$	41	56.1	°C/W
Junction-to-top characterization parameter	$ψ_{JT}$	11.3	1.5	°C/W
Junction-to-board characterization parameter	$ψ_{JB}$	40.7	54.9	°C/W
Junction-to-case(bottom)thermal resistance	$R_{θJC(bot)}$	N/A	N/A	°C/W

9.Electrical Characteristics (V_S=±1.25 V to ±2.75 V (V_S=2.5 to 5.5V)

at T_A=25°C, V_{CM}=V_{OUT}=V_S/2, and R_{LOAD}=10kΩ connected to V_S/2 (unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input offset voltage	V_{OS}	V_S=5.5V			±2.25	±8	μV
		T_A=-40°C to 125°C, V_S=5.5V				±10.5	μV
Input offset voltage drift	dV_{OS}/dT	T_A=-40°C to 125°C, V_S=5.5V			±0.005	±0.05	μV/°C
Power-supply rejection ratio	PSRR	T_A=-40°C to 125°C			±1.25	±3.5	μV/V
Input bias current	I_B	R_{IN}=100kΩ			±30	±500	pA
			T_A=0°C to 85°C			±600	pA
			T_A=-40°C to 125°C			±800	pA
Input offset current	I_{OS}	R_{IN}=100kΩ				±1000	pA
			T_A=0°C to 85°C			±1100	pA
			T_A=-40°C to 125°C			±1100	pA
Input voltage noise	E_N	f=0.1Hz to 10Hz			0.14		μV_{PP}
		f=10Hz			7		μV_{PP}
Input voltage noise density	e_N	f=100Hz			7		nV/√Hz
		f=1kHz			7		nV/√Hz
		f=10kHz			7		nV/√Hz
Input current noise density	I_N	f=1kHz			100		fA/√Hz
Common-mode voltage range	V_{CM}	(V-)-0.1V<V_{CM}<(V+)+0.1V		(V-)-0.1		(V+)+0.1	V
		V_S=±1.25V		102	110		V
Common-mode rejection ratio	CMRR	(V-)<V_{CM}<(V+)+0.1V, T_A=-40°C to 125°C	V_S=±2.75V	124	140		dB
			V_S=±1.25V	102	107		dB
Differential input impedance	z_{id}	(V-)-0.05V<V_{CM}<(V+)+0.1V, T_A=-40°C to 125°C, V_S=±2.75V		124	140		MΩ||pF
					100||2		MΩ||pF
Common-mode input impedance	z_{ic}				60||4.5		TΩ||pF

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Open-loop voltage gain	A_{OL}	(V-)+0.15V<V_O<(V+)-0.15V, R_{LOAD}=10kΩ		126	148		dB
		(V-)+0.15V<V_O<(V+)-0.15V, R_{LOAD}=10kΩ V_S=5.5V, T_A=-40°C to +125°C		120	126		dB
		(V-)+0.25V<V_O<(V+)-0.25V, R_{LOAD}=2kΩ		126	148		dB
		(V-)+0.3V<V_O<(V+)-0.3V, R_{LOAD}=2kΩ V_S=5.5V, T_A=-40°C to +125°C		120	126		dB
Unity-gain bandwidth	GBW				10		MHz
Slew rate	SR	G=1, 4-V step			5		V/μs
Total harmonic distortion+noise	THD+N	G=1, f=1kHz, V_O=1V_{RMS}			0.0005		
Settling time	t_S	To 0.1%	V_S=±2.5V, G=1, 1-V step		0.75		μs
		To 0.01%	V_S=±2.5V, G=1, 1-V step		2		μs
Overload recovery time	t_{OR}	V_{IN}×G=V_S			10		μs
Voltage output swing from rail	V_O	Positive rail	No load		1	15	mV
			R_{LOAD}=10kΩ		5	20	mV
			R_{LOAD}=2kΩ		20	50	mV
		Negative rail	No load		5	15	mV
			R_{LOAD}=10kΩ		10	20	mV
			R_{LOAD}=2kΩ		40	60	mV
		T_A=-40°C to +125°C, both rails R_{LOAD}=10kΩ			10	25	mV
Short-circuit current	I_{SC}	V_S=5.5V			±60		mA
		V_S=2.5V			±30		mA
Capacitive load drive	C_{LOAD}	See Figure 26					
Open-loop output impedance	Z_O	f=1MHz, I_O=0A, see Figure 25			100		Ω
Quiescent current per amplifier	I_Q	V_S=±1.25V (V_S=2.5V)	I_O=0A		1.7	2.4	mA
			T_A=-40°C to +125°C,I_O=0A		1.7	2.4	mA
		V_S=±2.75V (V_S=5.5V)	I_O=0A		1.9	2.6	mA
			T_A=-40°C to +125°C,I_O=0A		1.9	2.6	mA

10.1 Typical Characteristic

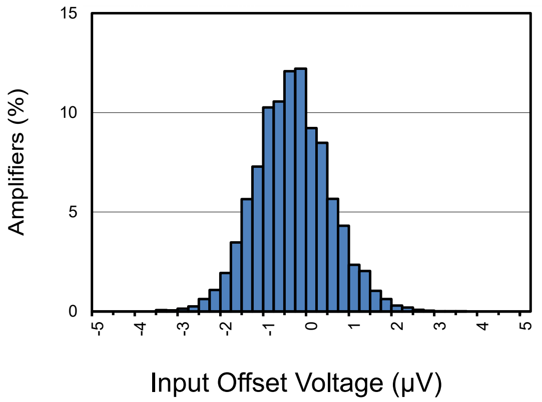


Figure 1: Offset Voltage Production Distribution

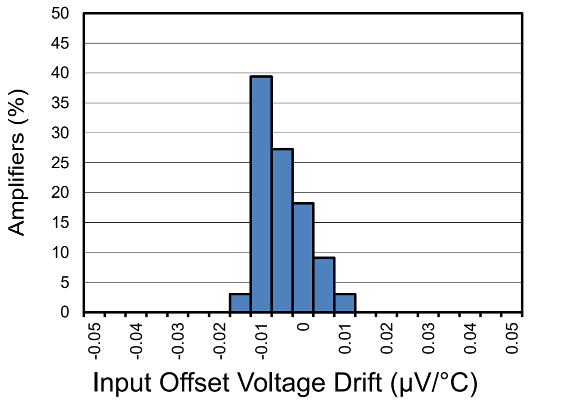


Figure 2: Offset Voltage Drift Distribution From -40°C to +125°C

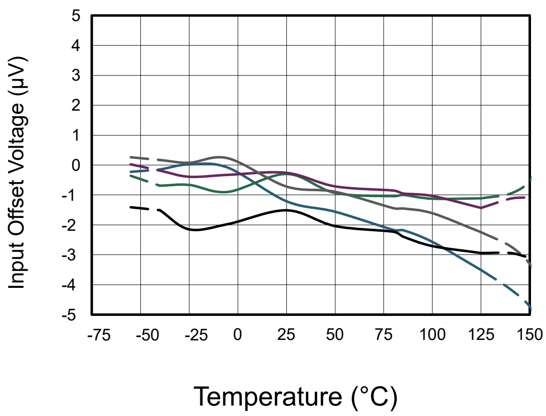


Figure 3: Offset Voltage vs Temperature

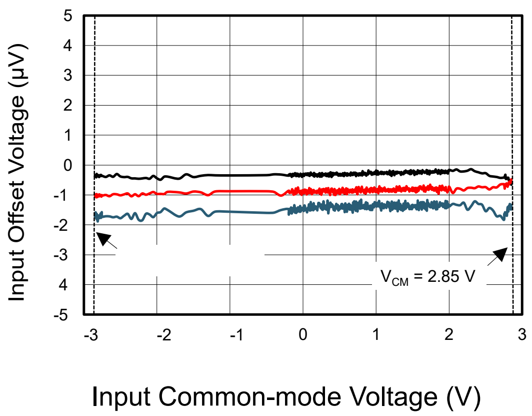


Figure 4: Offset Voltage vs Common-Mode Voltage

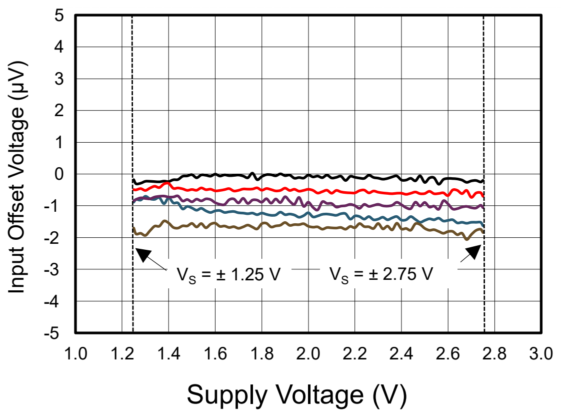


Figure 5: Offset Voltage vs Supply Voltage

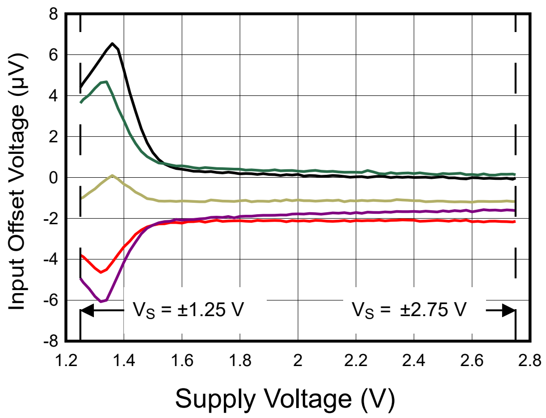


Figure 6: Offset Voltage vs Supply Voltage: OPA4388

10.2 Typical Characteristic

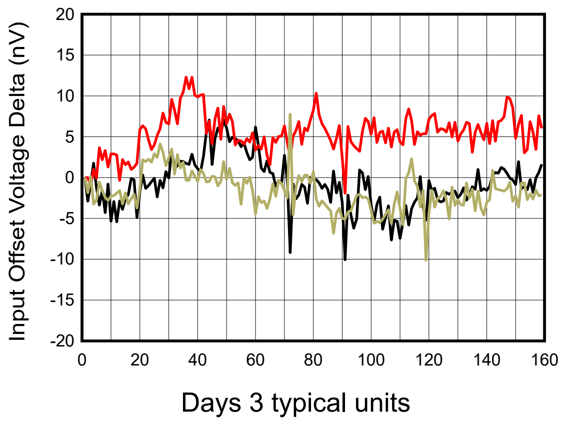


Figure 7: Offset Voltage Long Term Drift

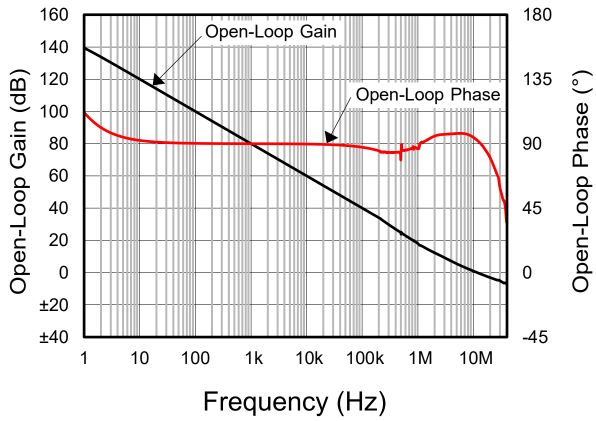


Figure 8: Open-Loop Gain and Phase vs Frequency

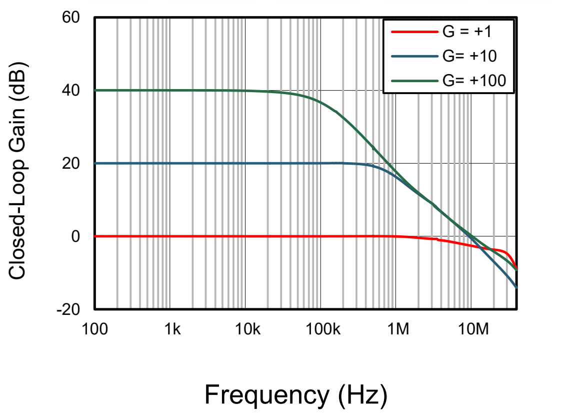


Figure 9: Closed-Loop Gain and Phase vs Frequency

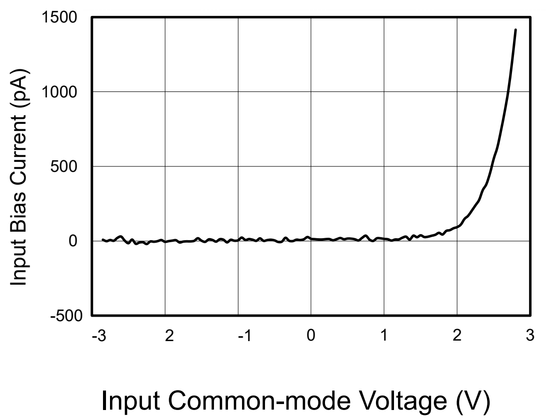


Figure 10: Input Bias Current vs Common-Mode Voltage

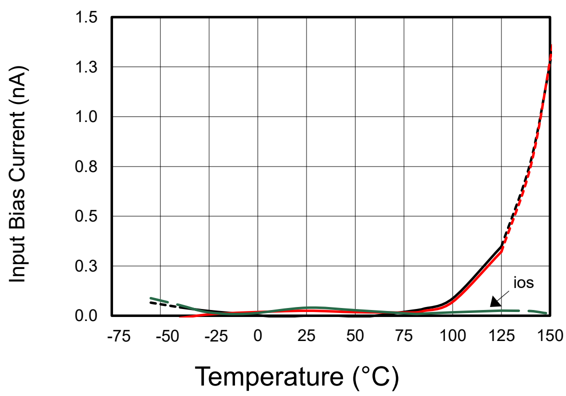


Figure 11: Input Bias Current vs Temperature

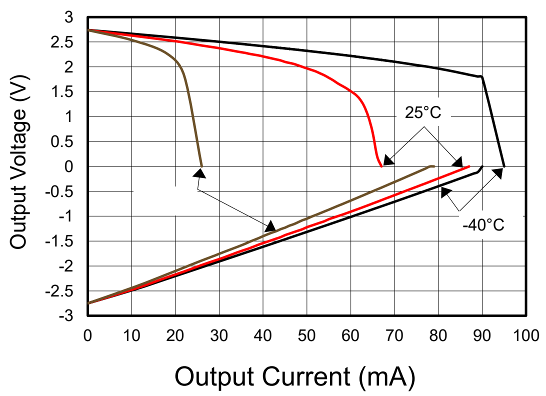


Figure 12: Output Voltage Swing vs Output Current (Maximum Supply)

10.3 Typical Characteristic

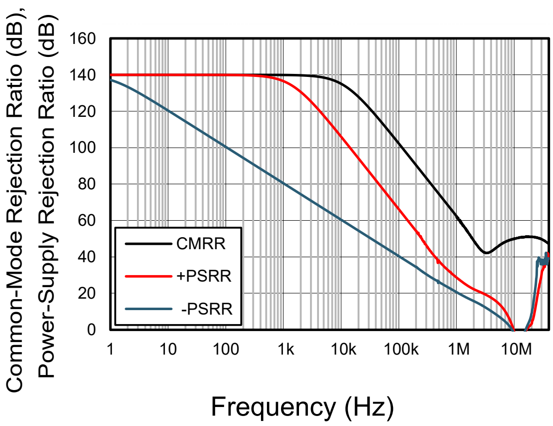


Figure 13: CMRR and PSRR vs Frequency

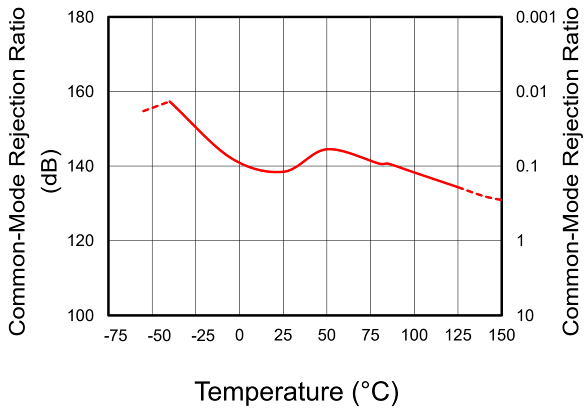


Figure 14: CMRR vs Temperature

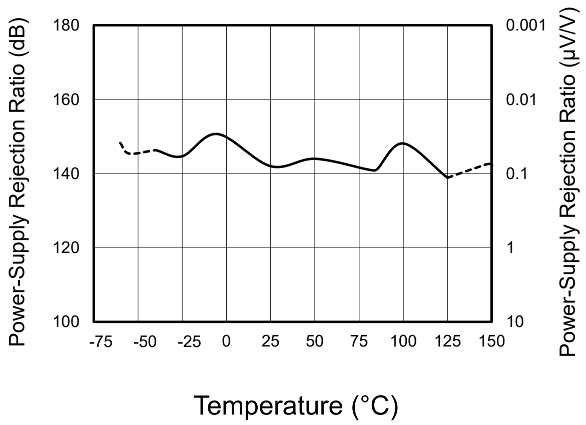


Figure 15: PSRR vs Temperature

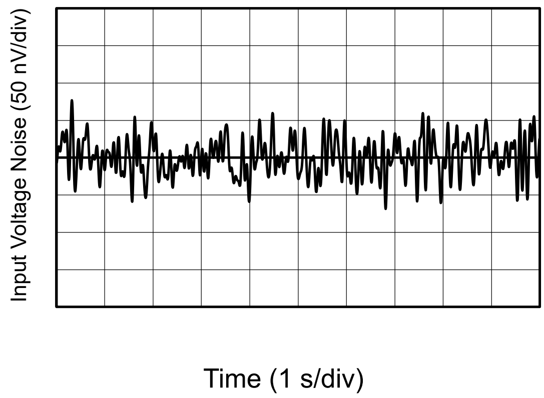


Figure 16: 0.1-Hz to 10-Hz Noise

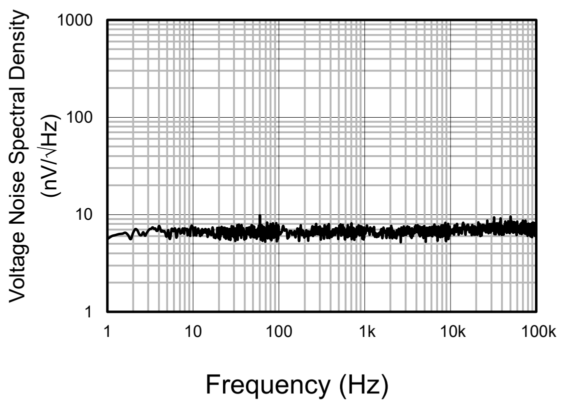


Figure 17: Input Voltage Noise Spectral Density vs Frequency

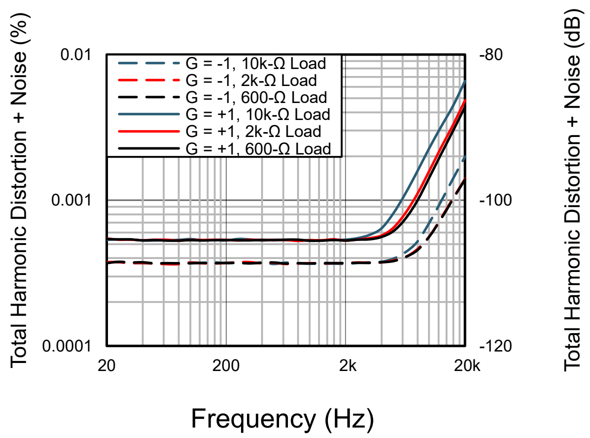


Figure 18: THD+N Ratio vs Frequency

10.4 Typical Characteristic

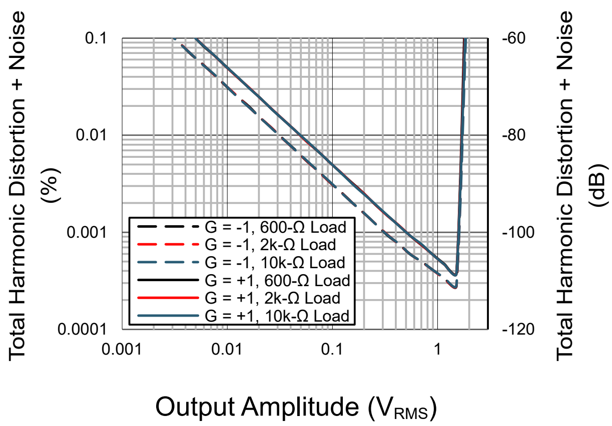


Figure 19: THD+N vs Output Amplitude

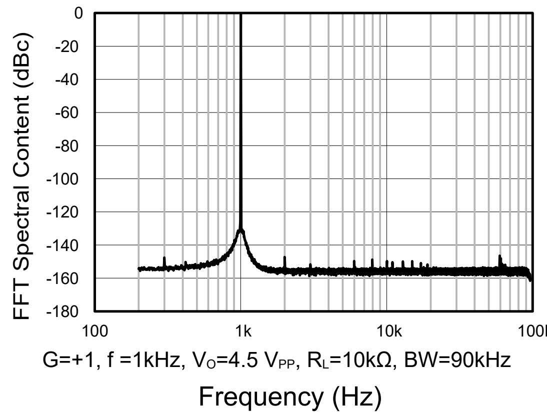


Figure 20: Spectral Content (With 10-kΩ Load)

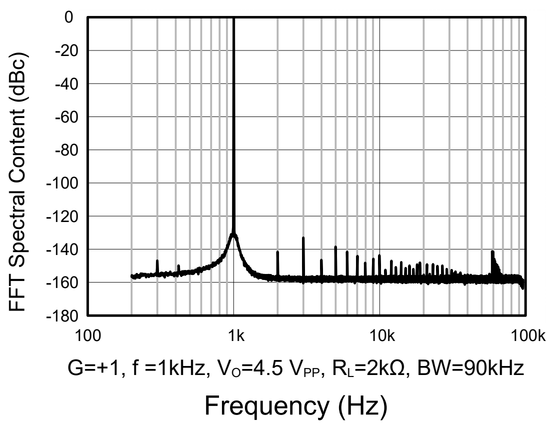


Figure 21: Spectral Content (With 2-kΩ Load)

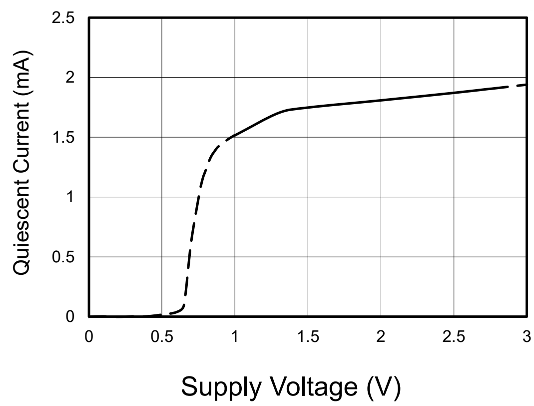


Figure 22: Quiescent Current vs Supply Voltage

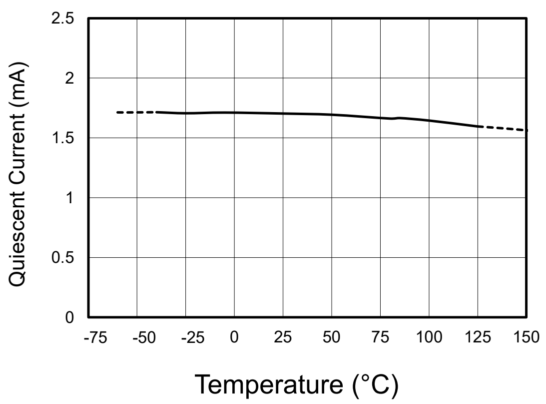


Figure 23: Quiescent Current vs Temperature

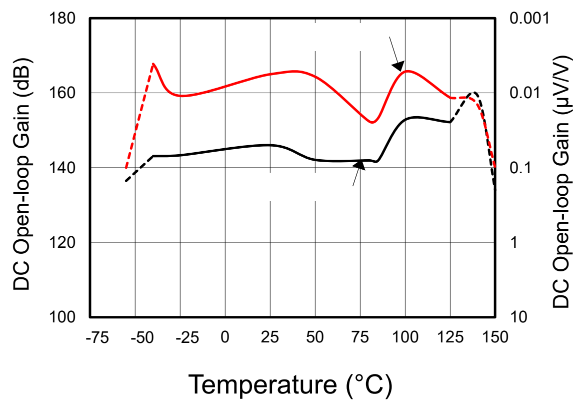


Figure 24: Open-Loop Gain vs Temperature

10.5 Typical Characteristic

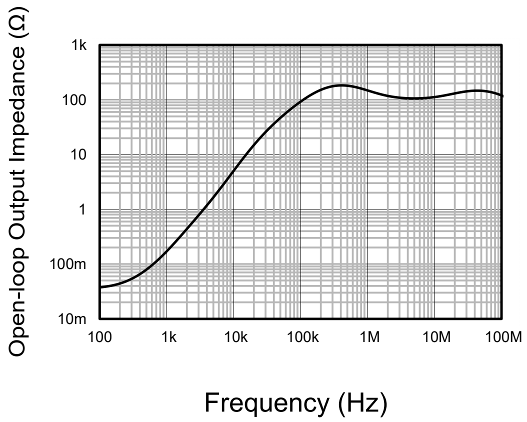


Figure 25: Open-Loop Output Impedance vs Frequency

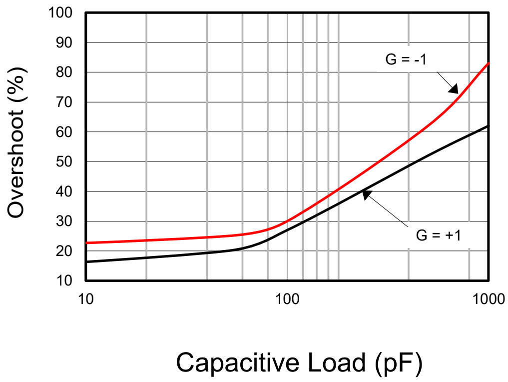


Figure 26: Small-Signal Overshoot vs Capacitive Load (10-mV Step)

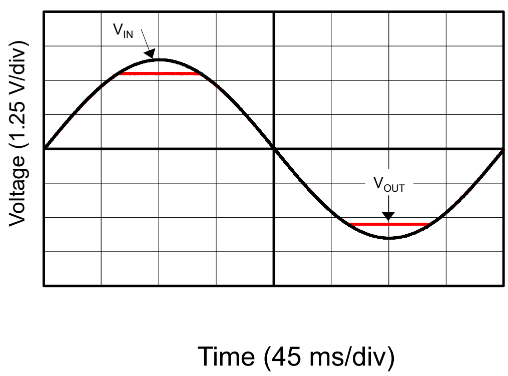


Figure 27: No Phase Reversal

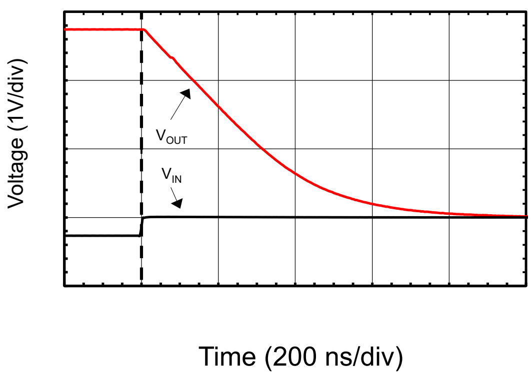


Figure 28: Positive Overload Recovery

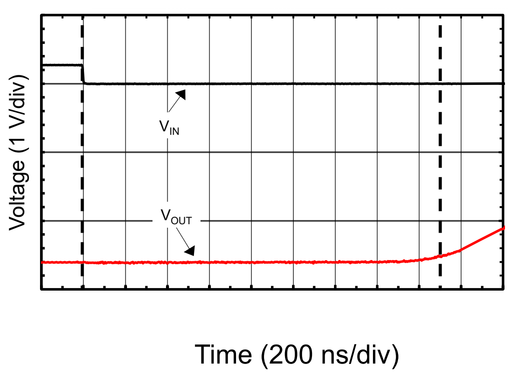


Figure 29: Negative Overload Recovery

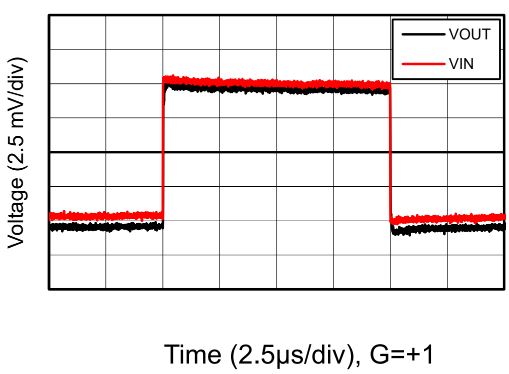


Figure 30: Small-Signal Step Response (10-mV Step)

10.6 Typical Characteristic

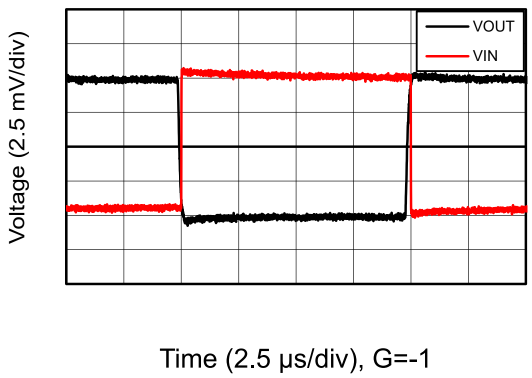


Figure 31: Small-Signal Step Response (10-mV Step)

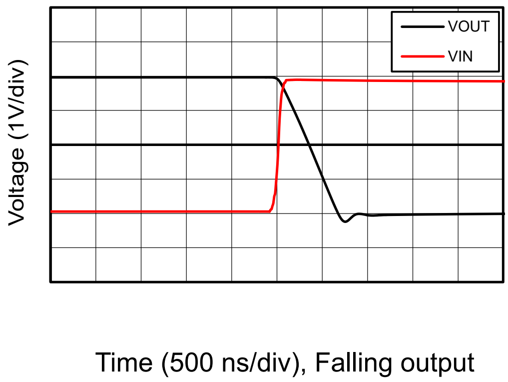


Figure 32: Large-Signal Step Response (4-V Step

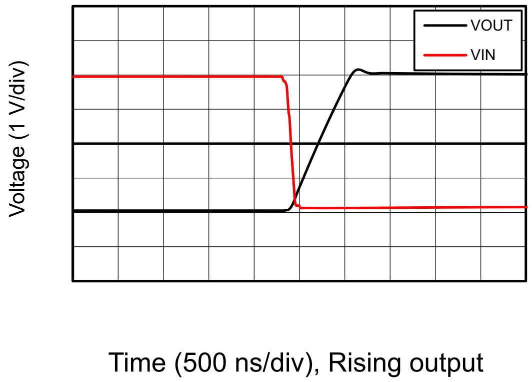


Figure 33: Large-Signal Step Response (4-V Step)

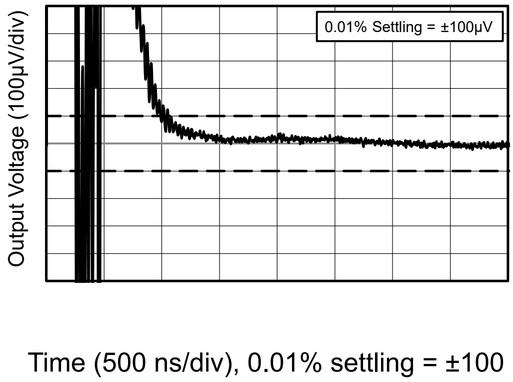


Figure 34: Settling Time (1-V Positive Step)

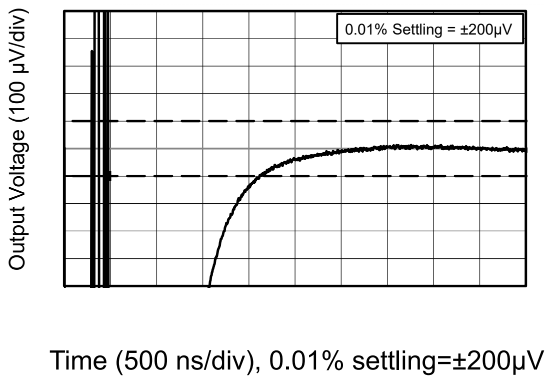


Figure 35: Settling Time (1-V Negative Step)

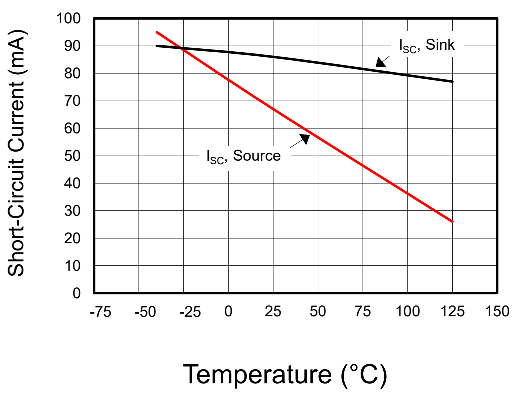


Figure 36: Short-Circuit Current vs Temperature

10.7 Typical Characteristic

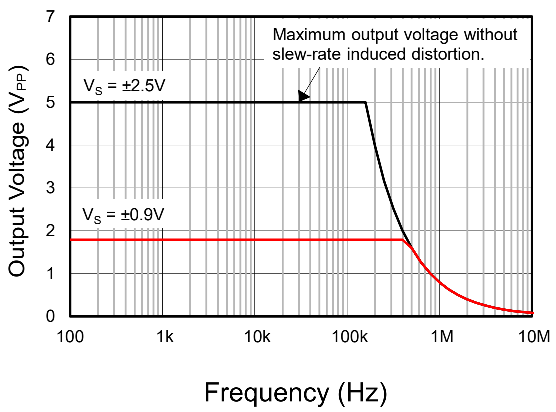


Figure 37: Maximum Output Voltage vs Frequency

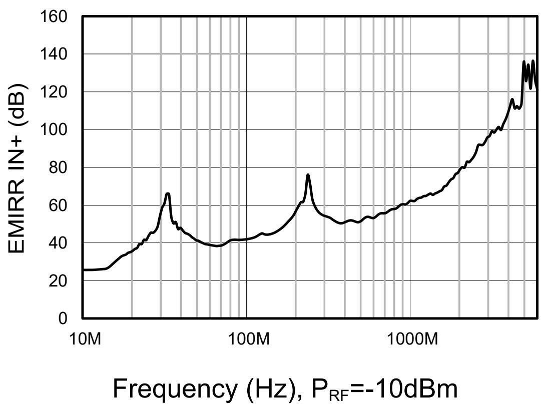
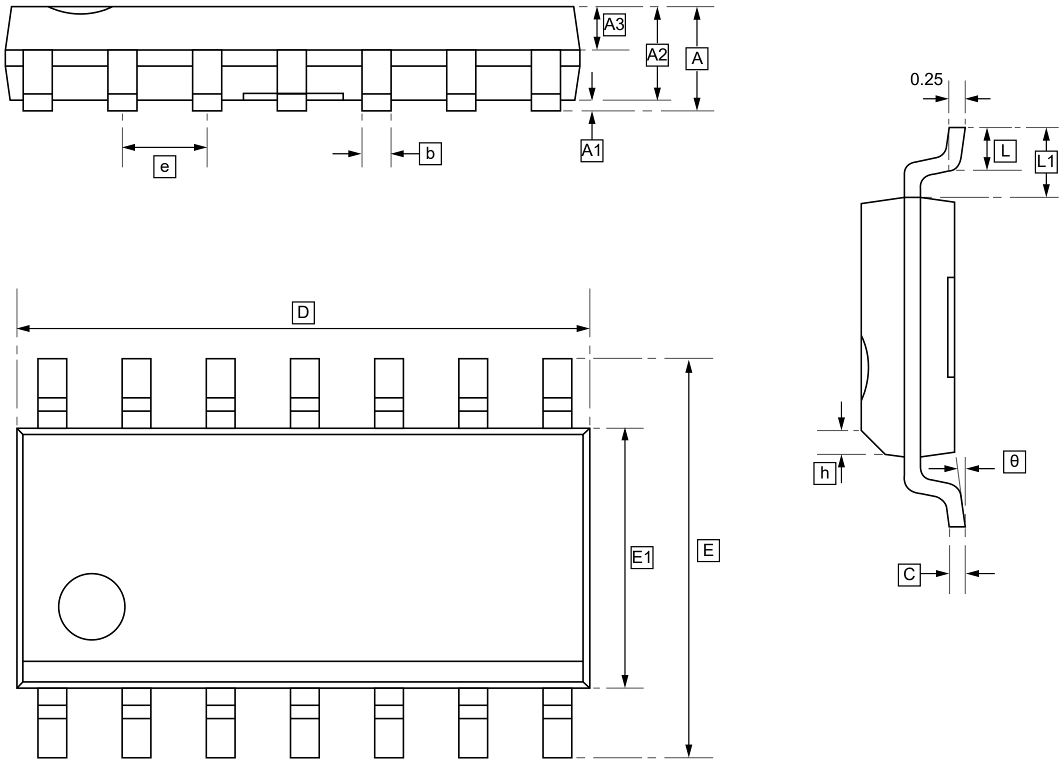


Figure 38: EMIRR vs Frequency

11.1 SOP-14 Package Outline Dimensions

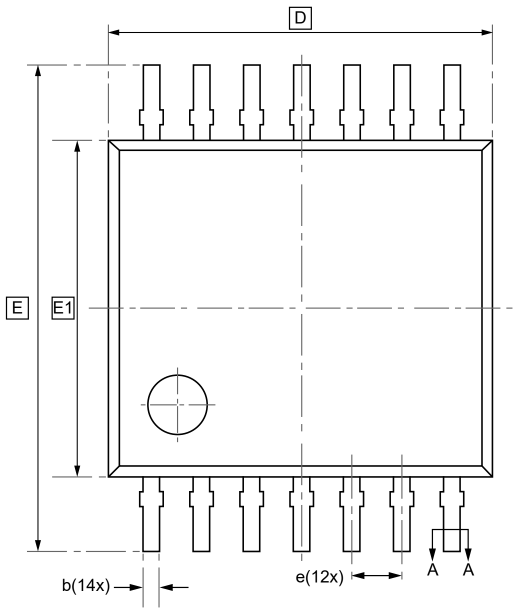


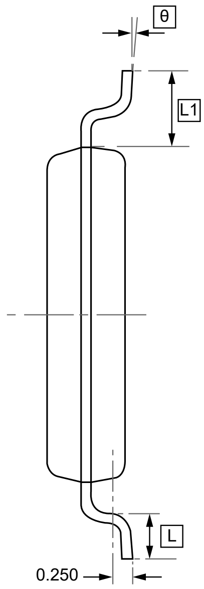
DIMENSIONS (mm are the original dimensions)

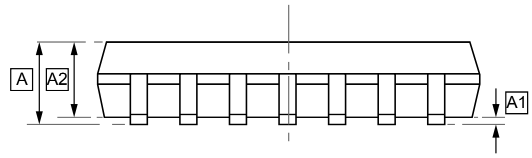
Symbol	A	A1	A2	A3	b	C	D	E	E1	e	h	L
Min	-	0.05	1.35	0.65	0.203	0.17	8.45	5.80	3.80	1.24	0.25	0.40
Max	1.75	0.25	1.55	0.75	0.305	0.25	8.85	6.20	4.00	1.30	0.50	0.80

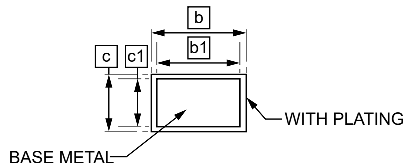
Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

11.2 TSSOP-14 Package Outline Dimensions







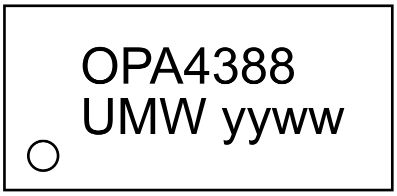


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	c1	D	E	E1	e	L1
Min	-	0.05	0.90	0.20	0.19	0.13	0.120	4.90	6.20	4.30	0.65	0.85
Max	1.20	0.15	1.05	0.28	0.25	0.17	0.14	5.10	6.60	4.50	BSC	1.15

Symbol	L	θ
Min	0.45	0°
Max	0.75	8°

12.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW OPA4388IPWR	OPA4388	TSSOP-14	4000	Tape and reel
UMW OPA4388IDR	OPA4388	SOP-14	2500	Tape and reel
UMW OPA4388ID	OPA4388	SOP-14	2500	Tape and reel

13.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.