



Description

The NVMFS5C673NLWFAFT1G uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 60V$ $I_D = 65A$

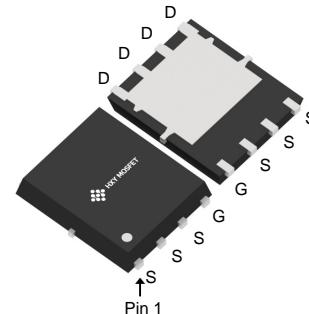
$R_{DS(ON)} < 11m\Omega$ $V_{GS} = 10V$

Application

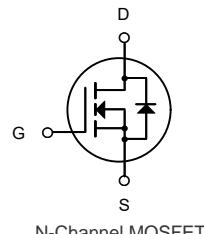
Battery protection

Load switch

Uninterruptible power supply



DFN5X6-8L
(TDSON-8-EP(5.1x5.9))



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NVMFS5C673NLWFAFT1G	DFN5X6-8L (TDSON-8-EP(5.1x5.9))	HXY MOSFET	5000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	65	A
$I_D @ T_c=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	49	A
I_{DM}	Pulsed Drain Current ²	180	A
EAS	Single Pulse Avalanche Energy ³	56	mJ
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	89	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	°C/W



Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<hr/>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=60\text{V}$, $V_{\text{GS}}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}= \pm 20\text{V}$	-	-	± 100	nA
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=250\mu\text{A}$	1.0	1.6	2.5	V
$R_{\text{DS}(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	-	8	11	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=10\text{A}$	-	14	20	
C_{iss}	Input Capacitance	$V_{\text{DS}}=25\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1.0\text{MHz}$	-	930	-	pF
C_{oss}	Output Capacitance		-	370	-	pF
C_{rss}	Reverse Transfer Capacitance		-	20	-	pF
Q_g	Total Gate Charge	$V_{\text{DS}}=30\text{V}$, $I_D=20\text{A}$, $V_{\text{GS}}=10\text{V}$	-	19	-	nC
Q_{gs}	Gate-Source Charge		-	4.8	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	4.5	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DD}}=30\text{V}$, $I_D=20\text{A}$, $R_G=1.6\Omega$, $V_{\text{GS}}=10\text{V}$	-	4.9	-	ns
t_r	Turn-on Rise Time		-	31	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time		-	23	-	ns
t_f	Turn-off Fall Time		-	8.7	-	ns
I_s	Maximum Continuous Drain to Source Diode Forward Current		-	-	65	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	240	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{\text{GS}}=0\text{V}$, $I_s=30\text{A}$	-	-	1.4	V
t_{rr}	Body Diode Reverse Recovery Time	$T_J=25^\circ\text{C}$, $I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	34	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	14	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{\text{DD}}=30\text{V}$, $V_{\text{G}}=10\text{V}$, $R_{\text{G}}=25\Omega$, $L=0.5\text{mH}$, $I_{\text{AS}}=12\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$



Typical Performance Characteristics

Figure 1: Output Characteristics

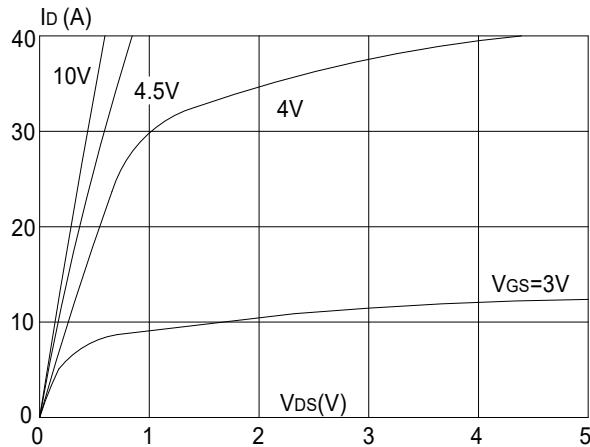


Figure 2: Typical Transfer Characteristics

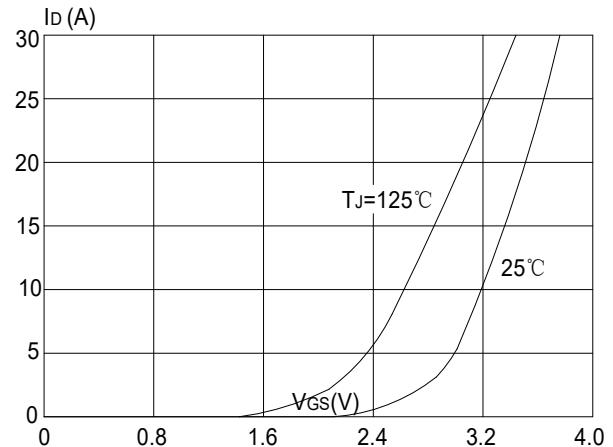


Figure 3: On-resistance vs. Drain Current

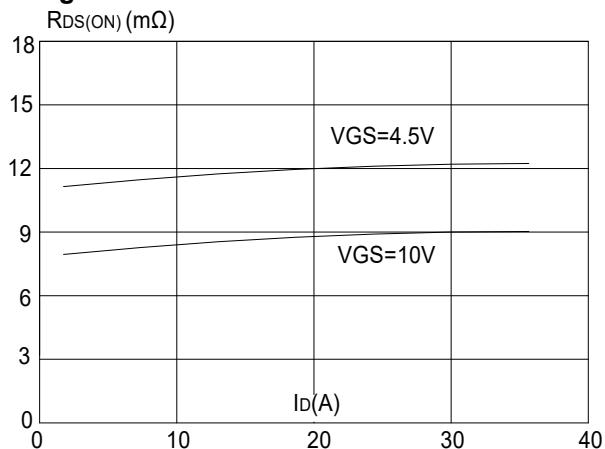


Figure 4: Body Diode Characteristics

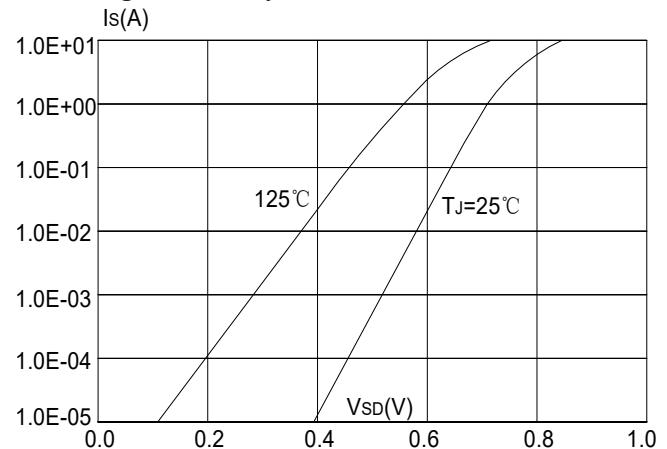


Figure 5: Gate Charge Characteristics

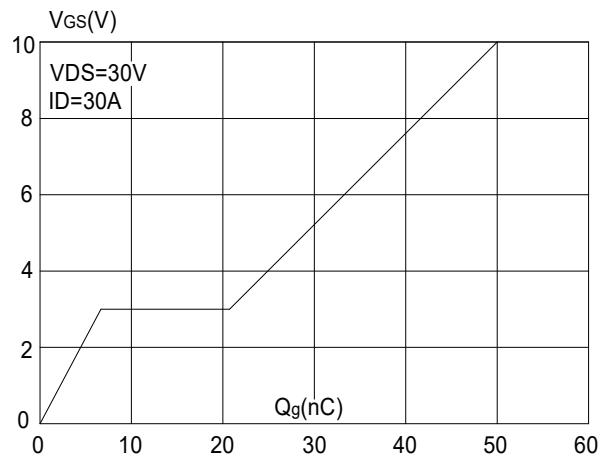


Figure 6: Capacitance Characteristics

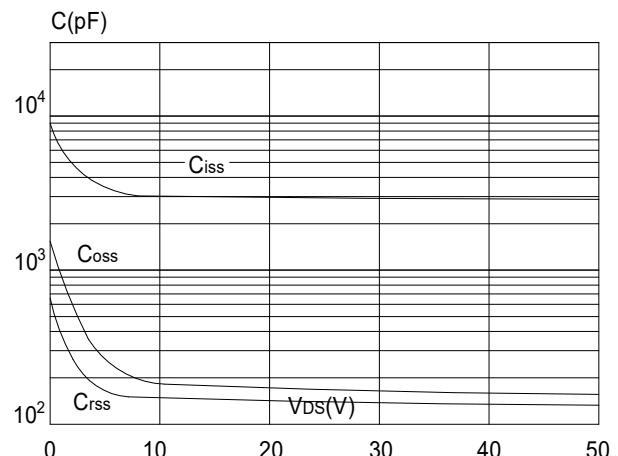




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

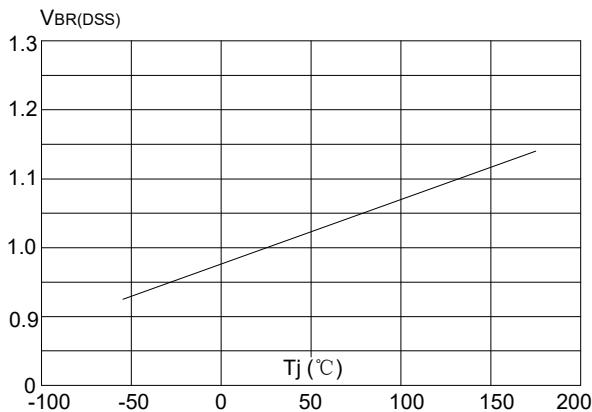


Figure 8: Normalized on Resistance vs. Junction Temperature

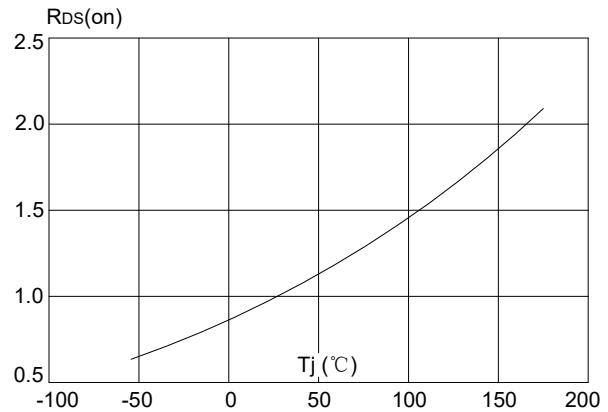


Figure 9: Maximum Safe Operating Area

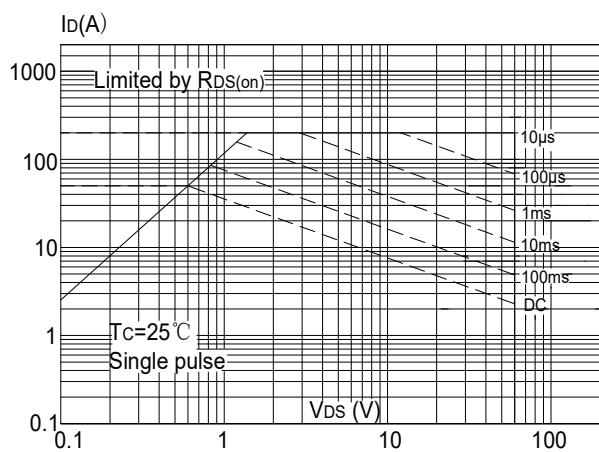


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

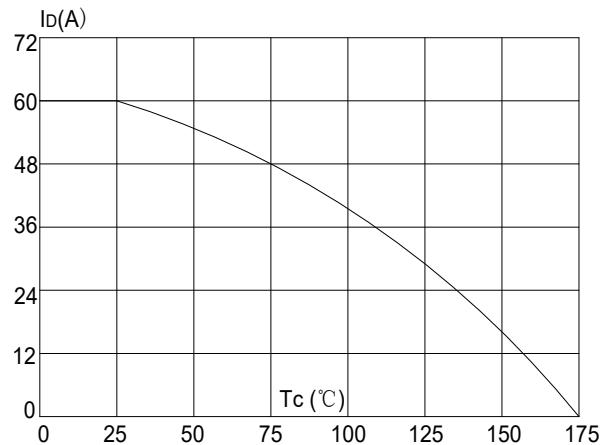
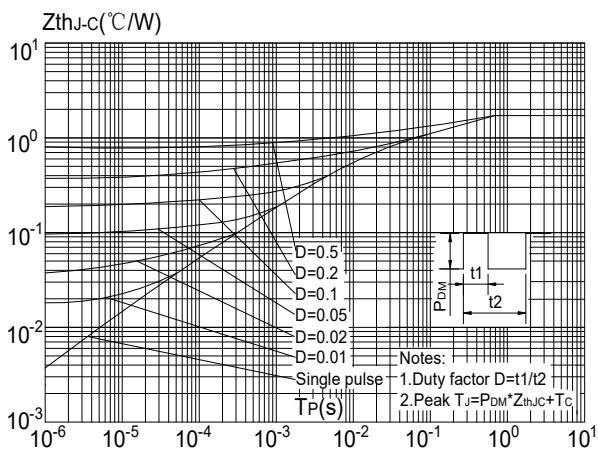
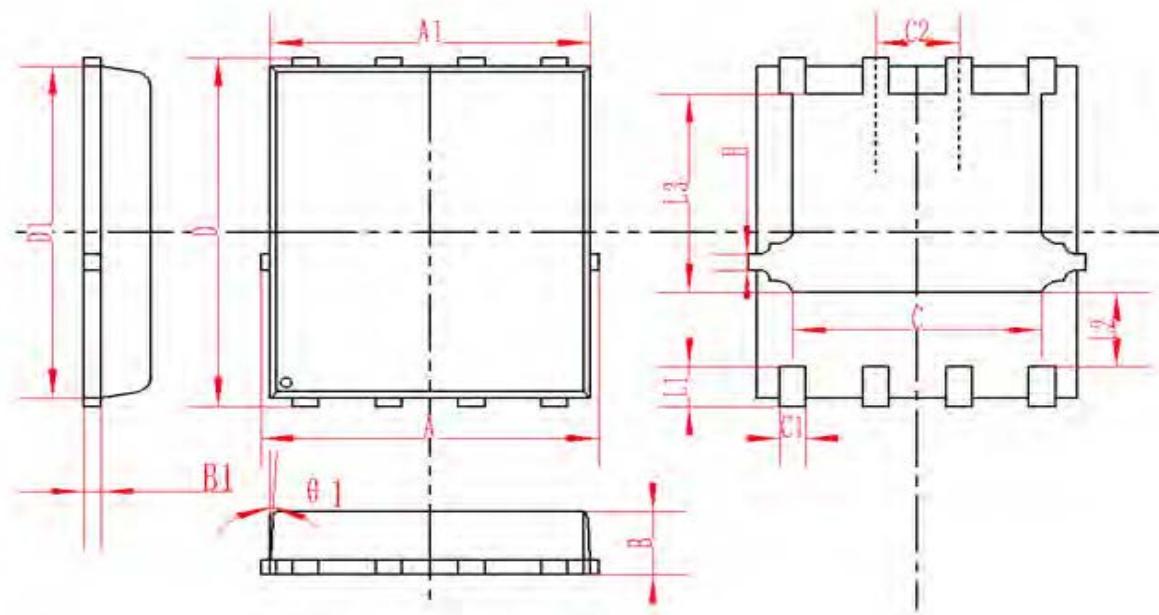


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case





DFN5X6-8L(TDS0N-8-EP(5.1x5.9)) Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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