



## Description

The NVMFS5C450NAFT1G uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

## General Features

$V_{DS} = 40V$   $I_D = 130A$

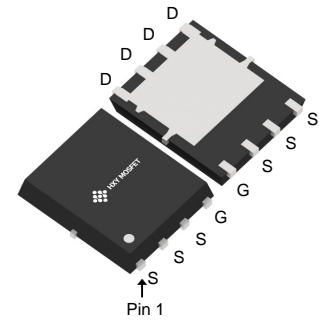
$R_{DS(ON)} < 3.5m\Omega$   $V_{GS}=10V$

## Application

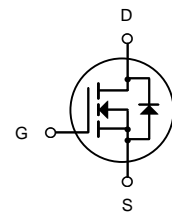
Battery protection

Load switch

Uninterruptible power supply



DFN5X6-8L



N-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NVMFS5C450NAFT1G	DFN5X6-8L	HXY MOSFET	5000

## Absolute Maximum Ratings ( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	130	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	65	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	400	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	150	mJ
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ C$



**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.6	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	2.8	3.5	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	50	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	5584	-	PF
Output Capacitance	C <sub>oss</sub>		-	410	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	338	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, I <sub>D</sub> =20A, R <sub>L</sub> =1Ω V <sub>GS</sub> =10V, R <sub>GEN</sub> =3Ω	-	11	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	15	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	38	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	14	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	64	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	12.4	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	14	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	130	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =30A di/dt = 100A/μs <sup>(Note3)</sup>	-	22		nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	11		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$



## Typical Characteristics

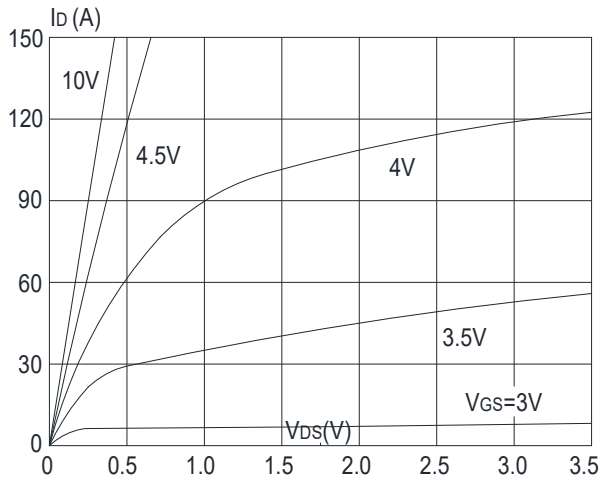


Figure1: Output Characteristics

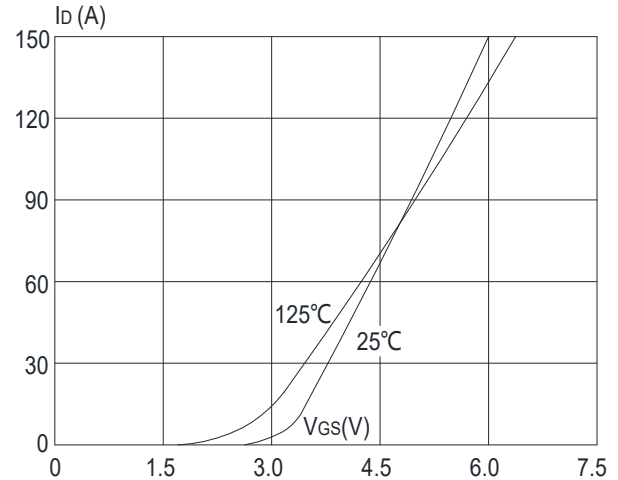


Figure 2: Typical Transfer Characteristics

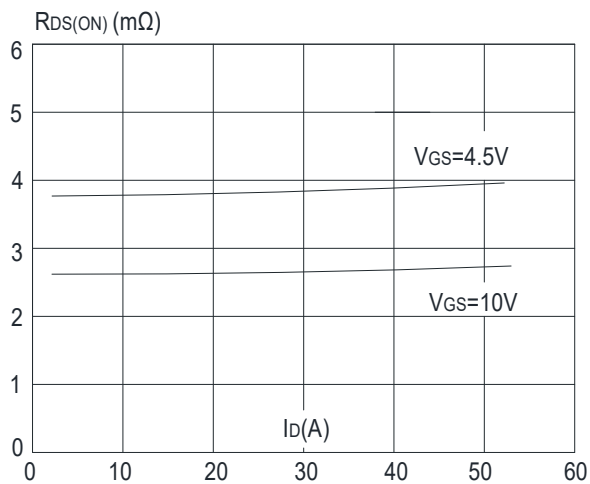


Figure 3: On-resistance vs. Drain Current

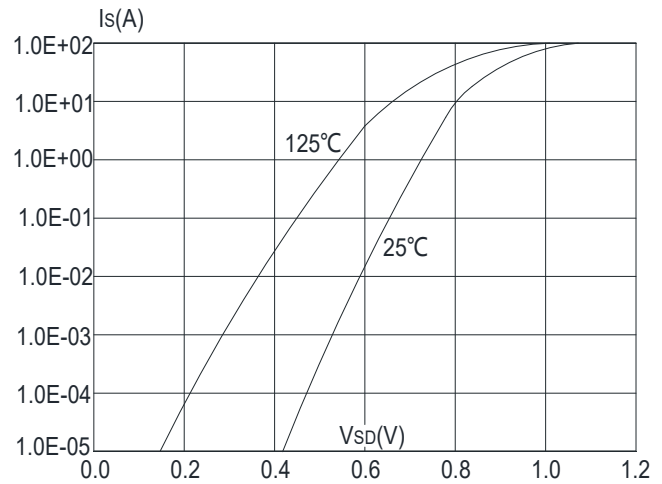


Figure 4: Body Diode Characteristics

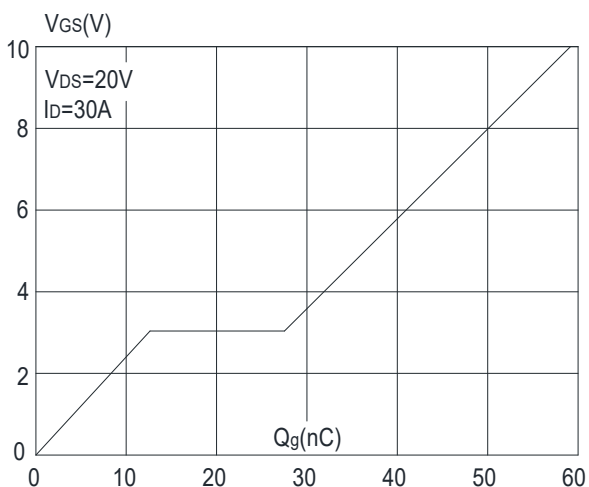


Figure 5: Gate Charge Characteristics

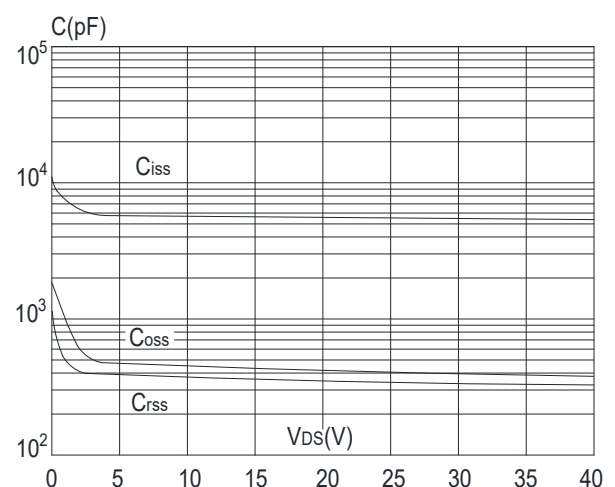
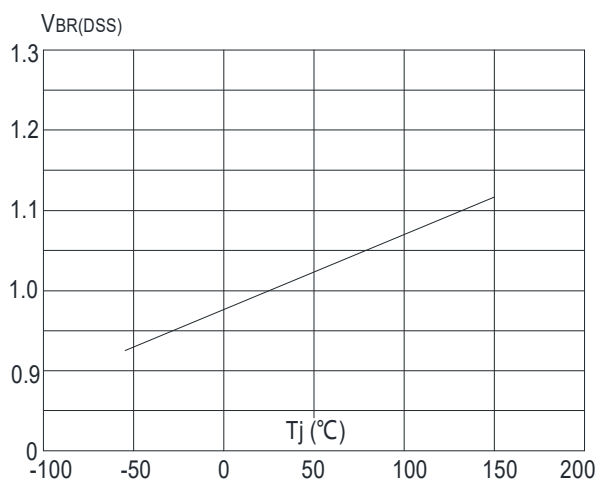
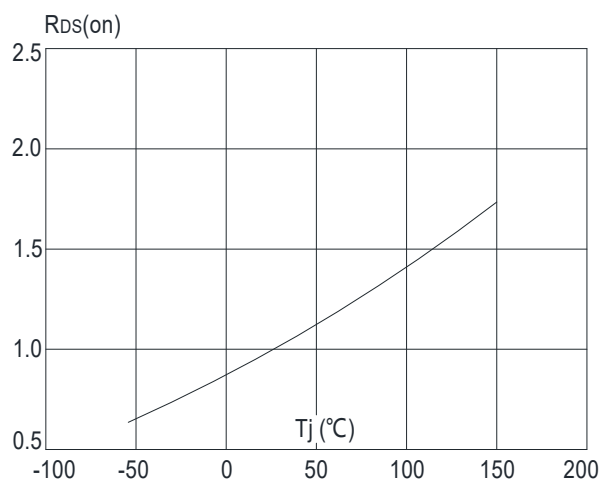


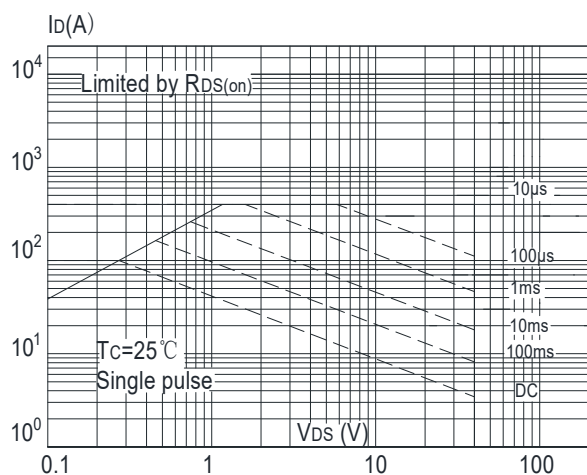
Figure 6: Capacitance Characteristics



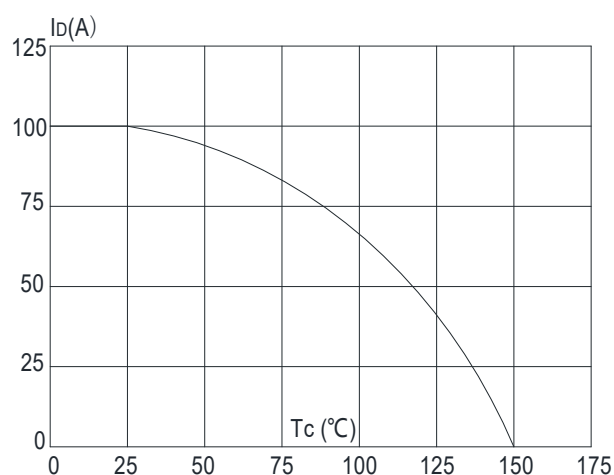
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



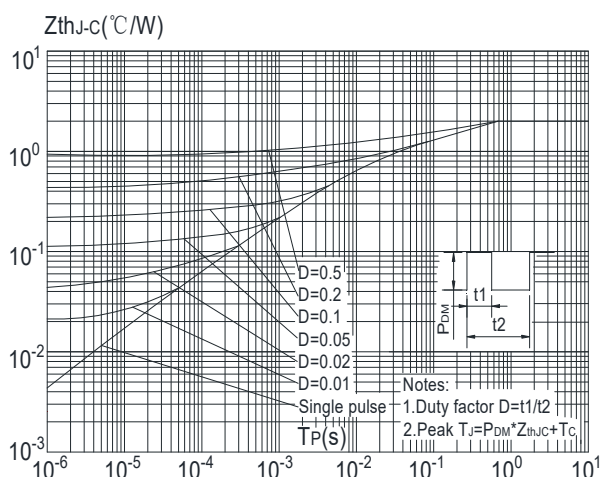
**Figure 8:** Normalized on Resistance vs. Junction Temperature



**Figure 9:** Maximum Safe Operating Area



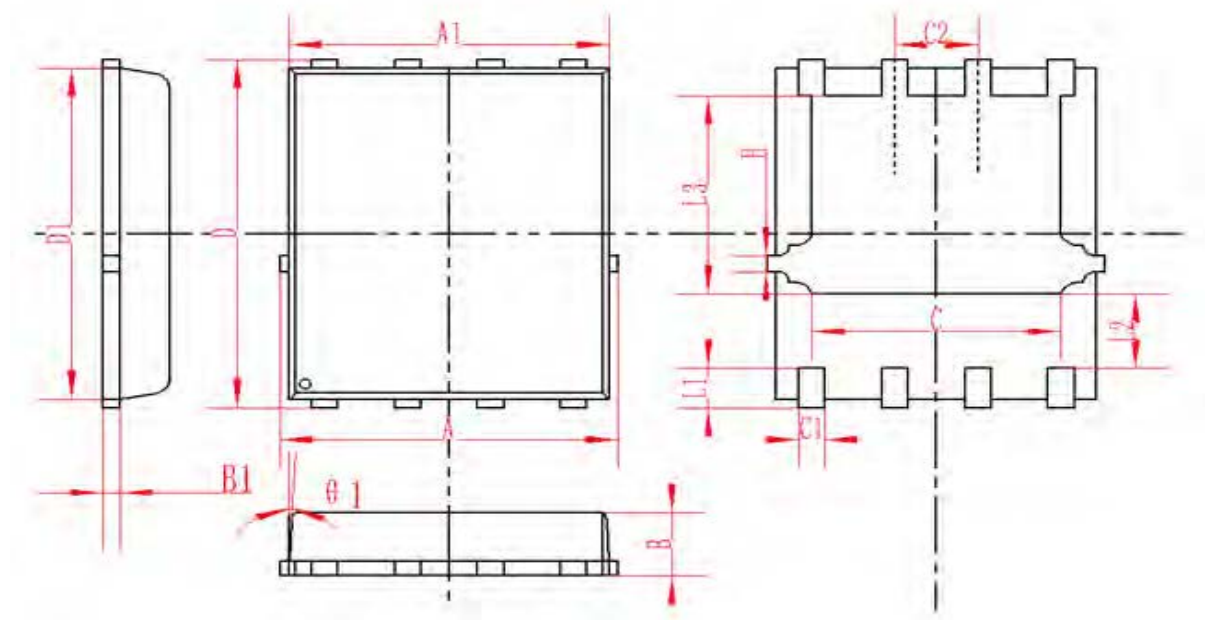
**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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