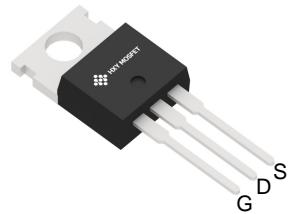




General Description

The PSMN4R8-100PSEQ use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness.



General Features

$V_{DS} = 100V$ $I_D = 120A$

$R_{DS(ON)} < 5.0m\Omega$ @ $V_{GS}=10V$

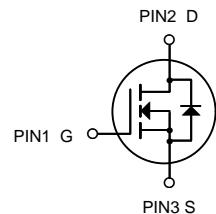
TO-220C

Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
PSMN4R8-100PSEQ	TO-220C	HXY MOSFET	50

Absolute Maximum Ratings at $T_j=25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾	I_D	120	A
Continuous drain current ¹⁾	I_D	81	A
Pulsed drain current ²⁾	I_{DM}	512	A
Power dissipation ⁴⁾	P_D	178	W
Single pulsed avalanche energy ³⁾	EAS	486	mJ
Operation and storage temperature	T_{STG}, T_j	-55 to 150	°C
Thermal resistance, junction-case	$R_{\theta JC}$	0.8	°C/W
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	56	°C/W



Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
△BV _{DSS} /△T _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	---	---	V/°C
R _{Ds(on)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	4.1	5.0	mΩ
		V _{GS} =4.5V, I _D =20A	---	---	---	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2.0	3.0	4.0	V
△V _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =80V, V _{GS} =0V, T _J =100°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =20A	---	35	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.6	---	Ω
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _D =20A	---	69	---	nC
Q _{gs}	Gate-Source Charge		---	24	---	
Q _{gd}	Gate-Drain Charge		---	18.5	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DD} =50V, RG=3Ω, ID=20A	---	18.0	---	ns
T _r	Rise Time		---	23	---	
T _{d(off)}	Turn-Off Delay Time		---	37	---	
T _f	Fall Time		---	15.7	---	
C _{iss}	Input Capacitance	V _{DS} =50V, V _{GS} =0V, f=1MHz	---	4102	---	pF
C _{oss}	Output Capacitance		---	592	---	
C _{rss}	Reverse Transfer Capacitance		---	19.8	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	120	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

1 The data is tested by a surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2 The data is tested by a pulsed pulse width ≤ 300us, Duty Cycle ≤ 2%

3 The EAS data shows Max. Rating AT the test condition As T_J = 25°C, L = 3.0mH, IAS = 18A, VGS = 10V, VDD = 50V; 100% test at L = 0.1mH, IAS = 67A.

4 The power dissipation is limited by 50°C junction temperature

5 The data is theoretically the same as A_D and A_{DM}. In real applications, it should be limited by total power dissipation.



Typical Characteristics

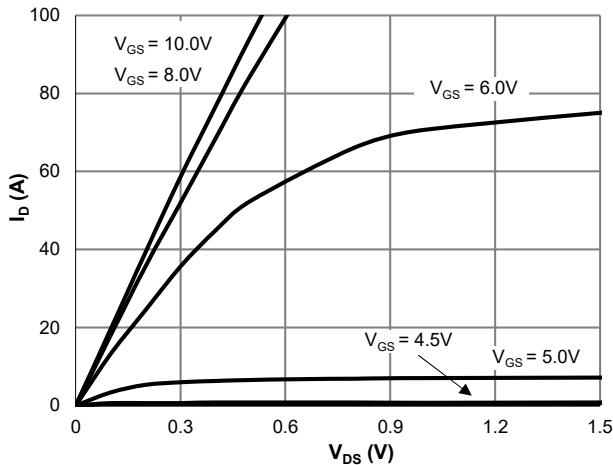


Figure 1: Saturation Characteristics

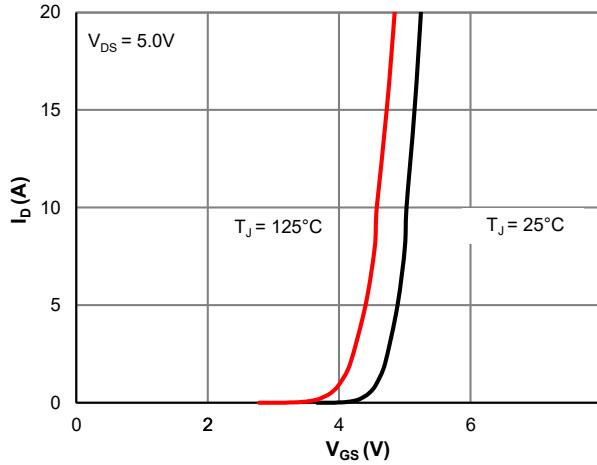


Figure 2: Transfer Characteristics

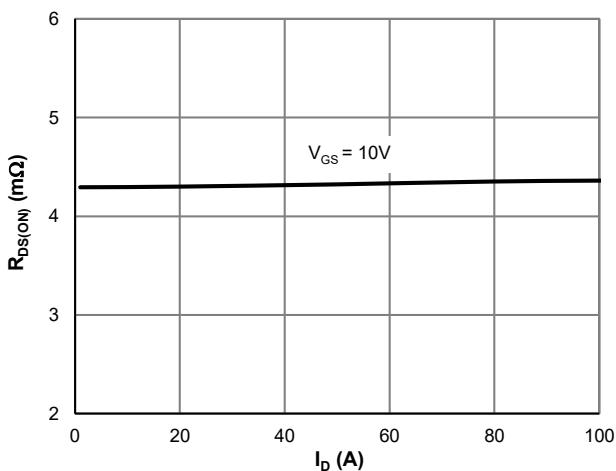


Figure 3: $R_{DS(ON)}$ vs. Drain Current

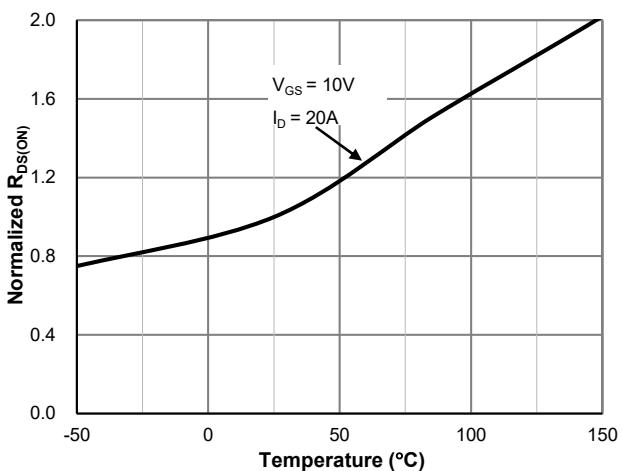


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

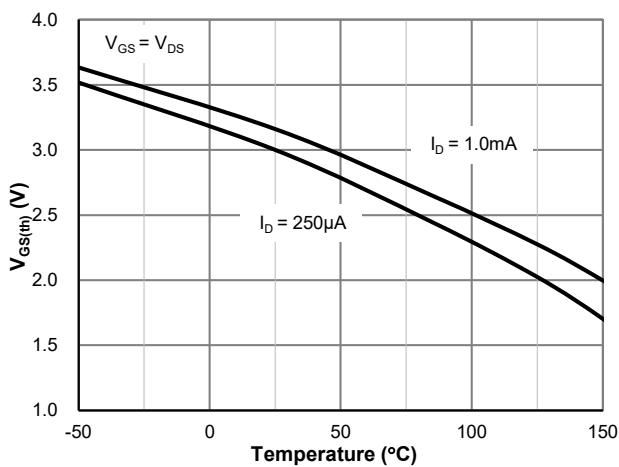


Figure 5: $V_{GS(th)}$ vs. Junction Temperature

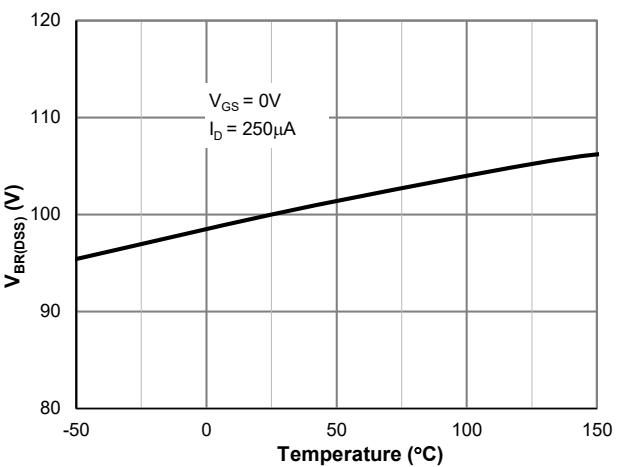


Figure 6: $V_{BR(DSS)}$ vs. Junction Temperature

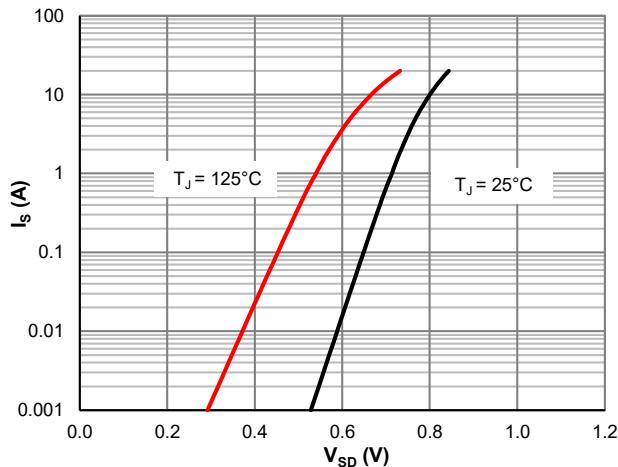


Figure 7: Body-Diode Characteristics

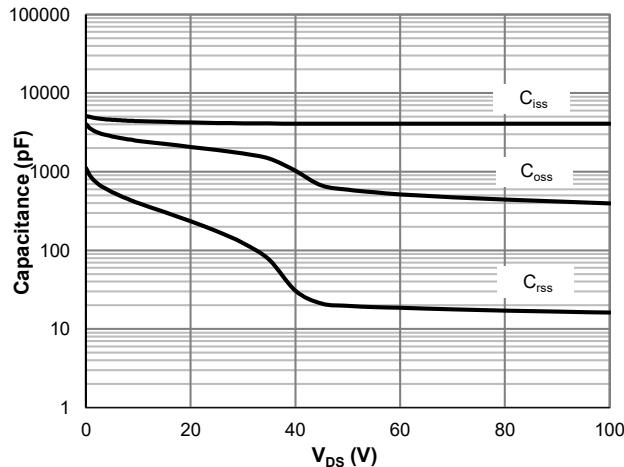


Figure 8: Capacitance Characteristics

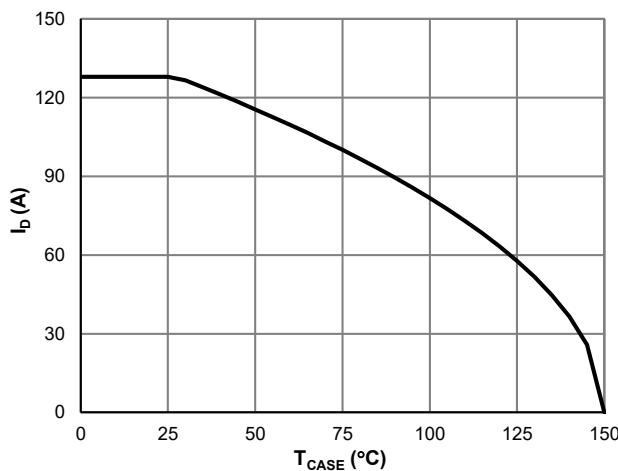


Figure 9: Current De-rating

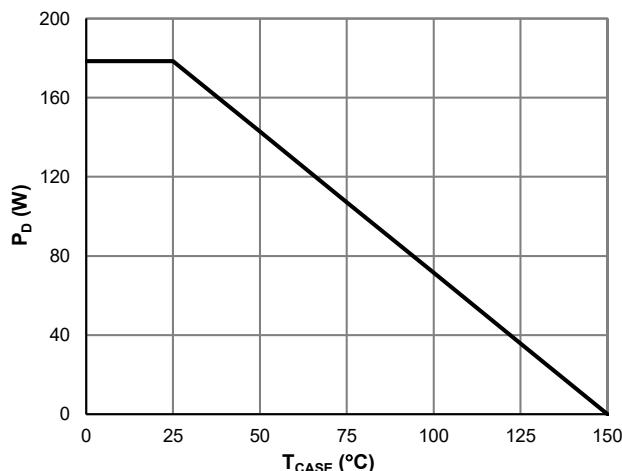


Figure 10: Power De-rating

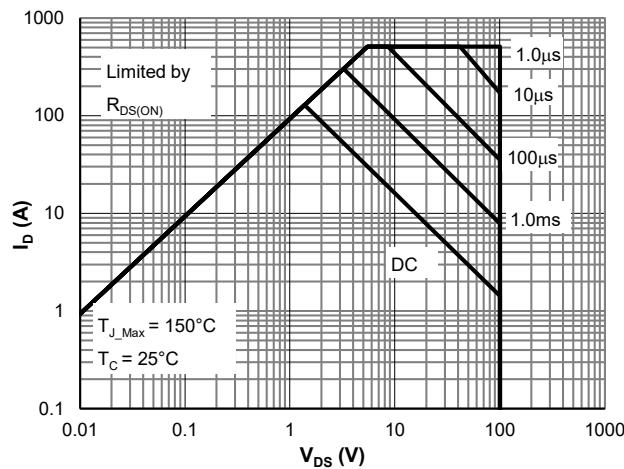


Figure 11: Maximum Safe Operating Area

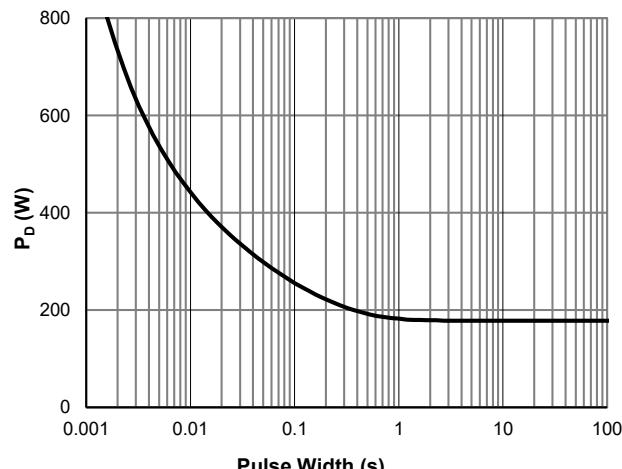


Figure 12: Single Pulse Power Rating, Junction-to-Case

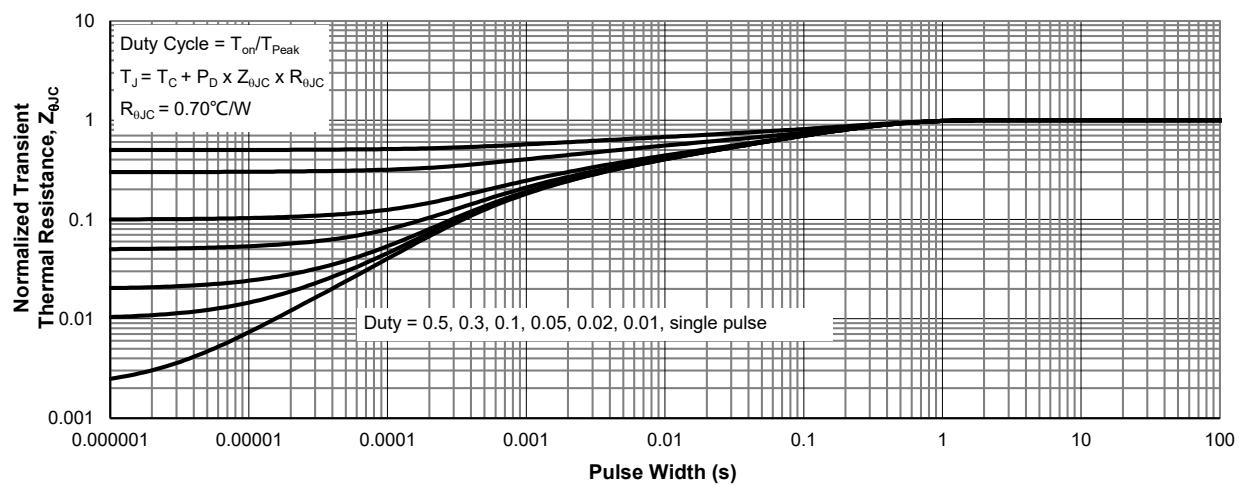
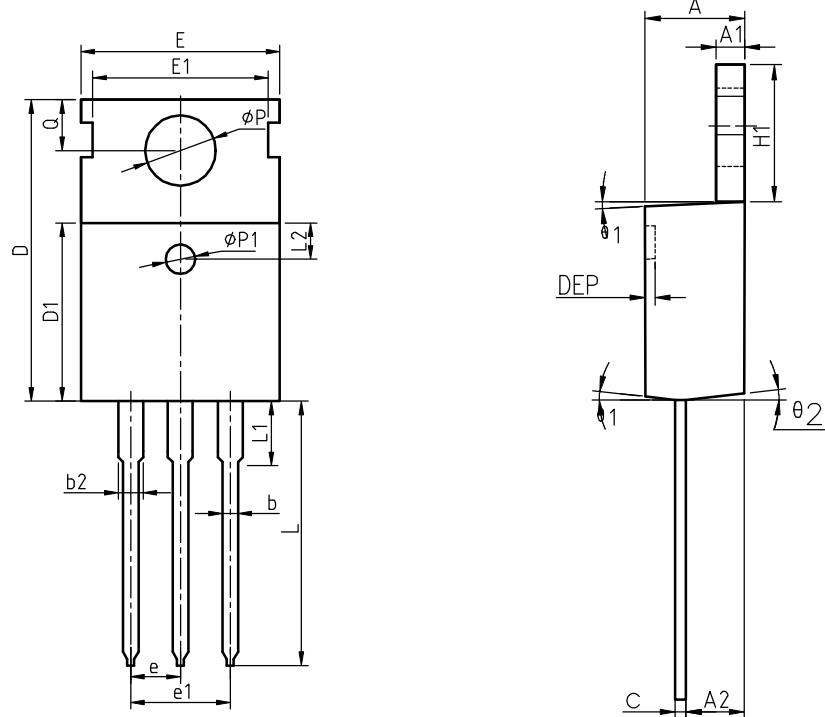


Figure 13: Normalized Maximum Transient Thermal Impedance

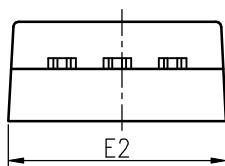


Package Information

TO-220C



COMMON DIMENSIONS



SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°
θ3	1°	3°	5°	1°	3°	5°



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