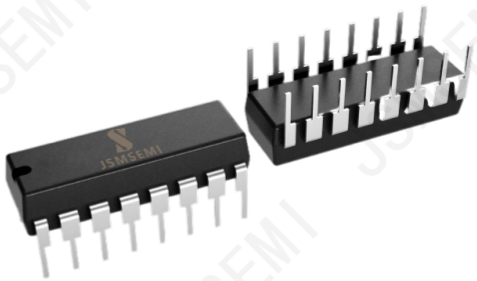
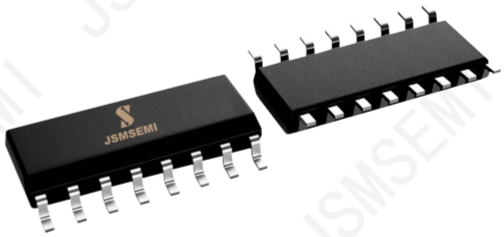
1、General Description

The 4538 is a dual retrig gerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger /retrigger input (nA), an active HIGH trigger/retrigger input (nB), an overriding active LOW direct reset input ($n\overline{CD}$), an output (nQ) and its complement ($n\overline{Q}$), and two pins (nREXT/CEXT, and nCEXT, always connected to ground) forconnecting the external timing components C_{EXT} and R_{EXT}. Typical pulse width variation over the specified temperature range is ±0.2%.

The multivibrator may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10us to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_{EXT} and R_{EXT}. The output pulse width (t_W) is equal to $R_{EXT} \times C_{EXT}$. The linear design techniques in LOCMOS (Local Oxide CMOS) guarantee precise control of the output pulse width. A LOW level at $n\overline{CD}$ terminates the output pulse immediately.

It operates over a recommended V_{DD} power supply range of 3V to 12V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.





Features:

- Wide supply voltage range from 3V to 12V
- Tolerant of slow trigger rise and fall times
- Fully static operation
- 5V and 10V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +125℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information

Order number	Package	Operation Temperature Range	MSL Grade	Ship,Quantity	Green
74HC4538D-JSM	SOP-16	-40 to 125°C	3	T&R,2500	Rohs

2、Block Diagram And Pin Description

2.1、Block Diagram

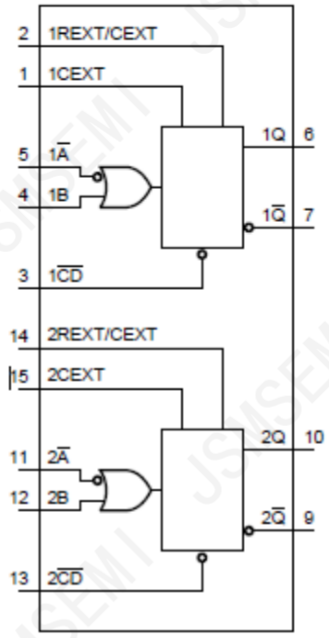


Figure 1. Functional diagram

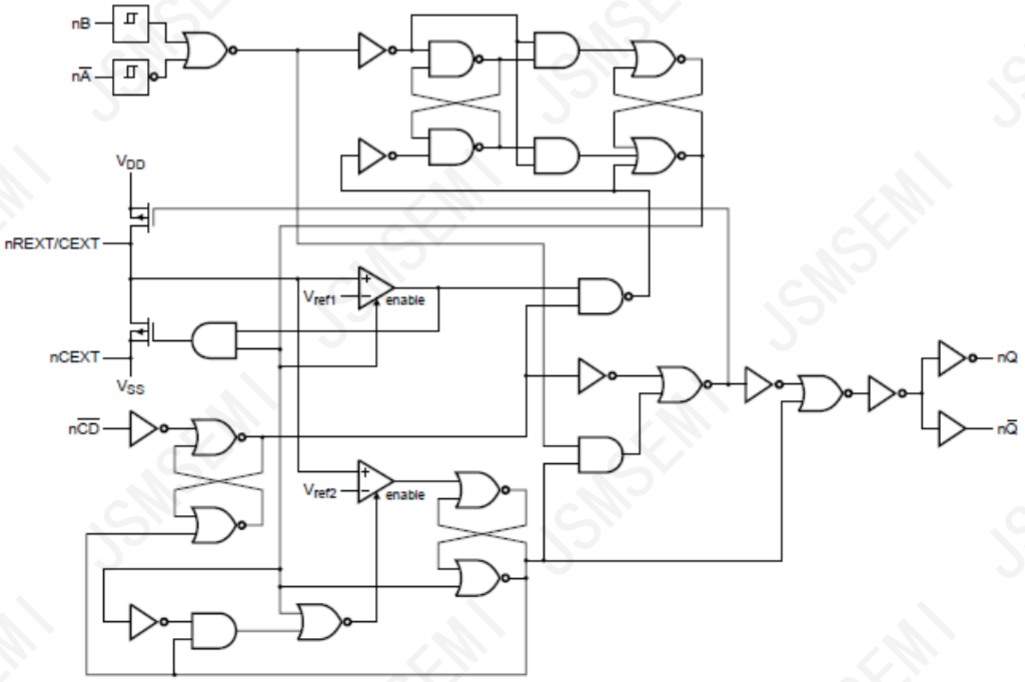
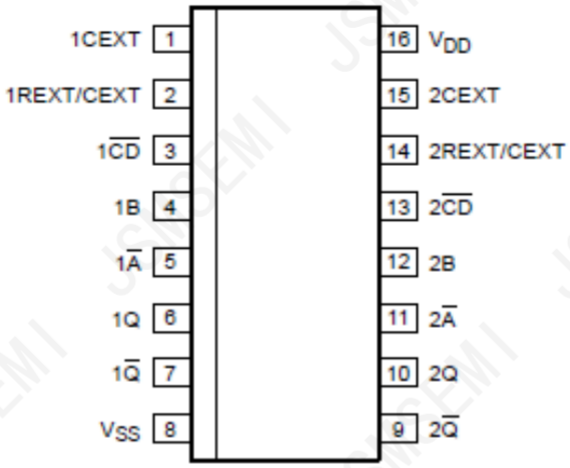


Figure 2. Logic diagram (one multivibrator)

2.2、Pin Configurations



2.3、Pin Description

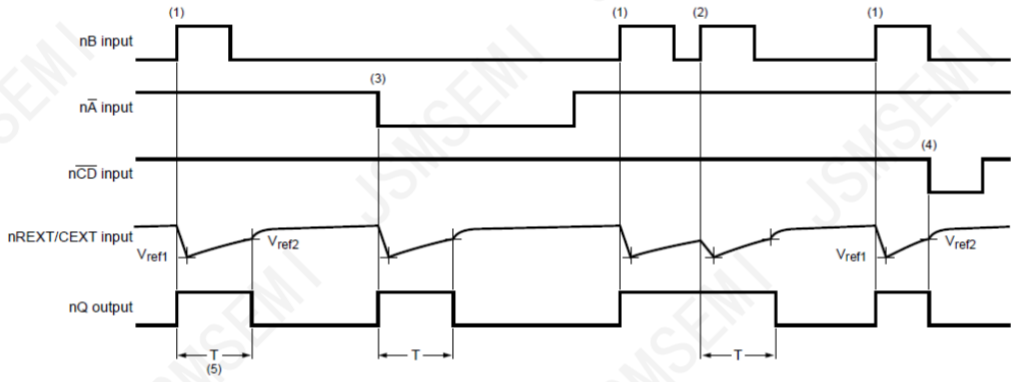
Pin No.	Pin Name	Description
1	1CEXT	external capacitor connection (always connected to ground)
2	1REXT/ CEXT	external capacitor/resistor connection
3	1$\overline{CD}$	direct reset input (active LOW)
4	1B	input (LOW-to-HIGH triggered)
5	1$\overline{A}$	input (HIGH-to-LOW triggered)
6	1Q	output
7	1$\overline{Q}$	complementary output (active LOW)
8	V_{SS}	ground (0V)
9	2$\overline{Q}$	complementary output (active LOW)
10	2Q	output
11	2$\overline{A}$	input (HIGH-to-LOW triggered)
12	2B	input (LOW-to-HIGH triggered)
13	2$\overline{CD}$	clear direct input (active LOW)
14	2REXT/ CEXT	external capacitor/resistor connection
15	2CEXT	external capacitor connection (always connected to ground)
16	V_{DD}	supply voltage

2.4、Function Table

Input			Output	
$n\bar{A}$	nB	$n\bar{C}\bar{D}$	nQ	$n\bar{Q}$
↓	L	H	⊓	⊔
H	↑	H	⊓	⊔
X	X	L	L	H

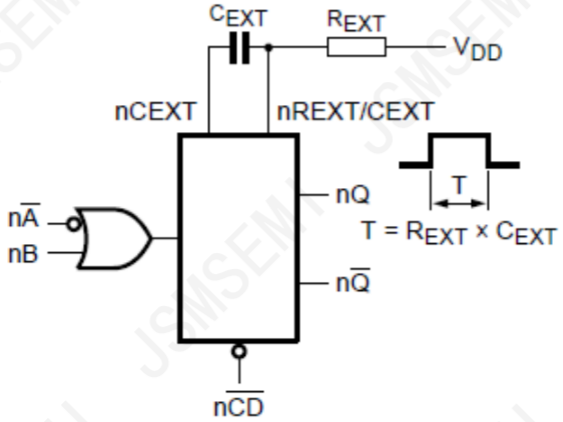
Note:
[1] H=HIGH voltage level; L=LOW voltage level; X=don't care;
[2] ↑=positive-going clock transition; ↓=negative-going transition;
[3] ⊓ =one HIGH level output pulse, with the pule width determined by C_{EXT} and R_{EXT};
[4] ⊔ =one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.

2.4.1、Timing Diagram



(1) Positive edge triggering.
(2) Positive edge re-triggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) T = REXT×CEXT.

2.4.2、Connection Of The External Timing Components REXT And CEXT



3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+14	V
DC input current	I_{IK}	any one input		-	±10	mA
input voltage	V_I	all inputs		-0.5	V_{DD}+0.5	V
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP/TSSOP	260		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	12	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions			T_{amb}=25℃			Unit
		$\|I_O\|$(uA)	V_O(V)	V_{DD}(V)	Min.	Typ.	Max.	
supply current	I_{DD}	active state V_I=V_{SS} or V_{DD}		5	-	55	-	uA
				10	-	150	-	uA
LOW-level output current	I_{OL}	-	0.4	5	0.5	-	-	mA
		-	0.5	10	1.3	-	-	mA
HIGH-level output current	I_{OH}	-	2.5	5	-	-	-1.4	mA
		-	4.6	5	-	-	-0.5	mA
		-	9.5	10	-	-	-1.3	mA
LOW-level output voltage	V_{OL}	<1	-	5	-	-	0.05	V
		<1	-	10	-	-	0.05	V
HIGH-level output voltage	V_{OH}	<1	-	5	4.95	-	-	V
		<1	-	10	9.95	-	-	V
LOW-level input voltage	V_{IL}	<1	-	5	-	-	1.5	V
		<1	-	10	-	-	3	V
HIGH-level input voltage	V_{IH}	<1	-	5	3.5	-	-	V
		<1	-	10	7	-	-	V
input leakage current	I_I	nA̅, nB		12	-	-	±1.0	uA
		nREXT/CEXT		12	-	-	±1.0	uA

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions			T_{amb}=-40℃		T_{amb}=+85℃		T_{amb}=+125℃		Unit
		$\|I_O\|$(uA)	V_O(V)	V_{DD}(V)	Min.	Max.	Min.	Max.	Min.	Max.	
LOW-level output current	I_{OL}	-	0.4	5	0.64	-	0.36	-	0.36	-	mA
		-	0.5	10	1.6	-	0.9	-	0.9	-	mA
HIGH-leve output current	I_{OH}	-	2.5	5	-	-1.7	-	-1.1	-	-1.1	mA
		-	4.6	5	-	-0.64	-	-0.36	-	-0.36	mA
		-	9.5	10	-	-1.6	-	-0.9	-	-0.9	mA
LOW-level output voltage	V_{OL}	<1	-	5	-	0.05	-	0.05	-	0.05	V
		<1	-	10	-	0.05	-	0.05	-	0.05	V
HIGH-leve output voltage	V_{OH}	<1	-	5	4.95	-	4.95	-	4.95	-	V
		<1	-	10	9.95	-	9.95	-	9.95	-	V
LOW-level input voltage	V_{IL}	<1	-	5	-	1.5	-	1.5	-	1.5	V
		<1	-	10	-	3.0	-	3.0	-	3.0	V
HIGH-level input voltage	V_{IH}	<1	-	5	3.5	-	3.5	-	3.5	-	V
		<1	-	10	7.0	-	7.0	-	7.0	-	V
input leakage current	I_I	nA, $\overline{nB}$		12	-	±0.1	-	±1.0	-	±1.0	uA
		nREXT/CEXT		12	-	±1.0	-	±1.0	-	±1.0	uA

3.3.3、AC Characteristics

(T_{amb}=25℃, V_{SS}=0V, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay	t_{PHL}	$n\bar{A}$ or nB to $n\bar{Q}$; see Figure 4	V_{DD}=5V	-	220	440	ns
			V_{DD}=10V	-	85	190	ns
		$n\bar{CD}$ to nQ; see Figure 4	V_{DD}=5V	-	125	250	ns
			V_{DD}=10V	-	55	110	ns
LOW to HIGH propagation delay	t_{PLH}	$n\bar{A}$ or nB to nQ; see Figure 4	V_{DD}=5V	-	200	460	ns
			V_{DD}=10V	-	90	180	ns
		$n\bar{CD}$ to $n\bar{Q}$; see Figure 4	V_{DD}=5V	-	125	250	ns
			V_{DD}=10V	-	55	110	ns
transition time	t_t	see Figure 4	V_{DD}=5V	-	60	120	ns
			V_{DD}=10V	-	30	60	ns
recovery time	t_{rec}	$n\bar{CD}$ to $n\bar{A}$ or nB; see Figure 5	V_{DD}=5V	-	20	40	ns
			V_{DD}=10V	-	10	20	ns
retrigger time	t_{rtrig}	nQ, $n\bar{Q}$ to $n\bar{A}$, nB; see Figure 5	V_{DD}=5V	0	-	-	ns
			V_{DD}=10V	0	-	-	ns
pulse width	t_W	$n\bar{A}$ LOW; minimum width; see Figure 5	V_{DD}=5V	90	45	-	ns
			V_{DD}=10V	30	15	-	ns
		nB HIGH; minimum width; see Figure 5	V_{DD}=5V	50	25	-	ns
			V_{DD}=10V	24	12	-	ns
		$n\bar{CD}$ LOW; minimum width; see Figure 5	V_{DD}=5V	55	25	-	ns
			V_{DD}=10V	25	12	-	ns
		nQ or $n\bar{Q}$; R_{EXT}=100kΩ; C_{EXT}=2nF; see Figure 5	V_{DD}=5V	218	230	242	us
			V_{DD}=10V	213	224	235	us
		nQ or $n\bar{Q}$; R_{EXT}=100kΩ; C_{EXT}=0.1uF; see Figure 5	V_{DD}=5V	10.3	10.8	11.3	ms
			V_{DD}=10V	10.2	10.7	11.2	ms
		nQ or $n\bar{Q}$; R_{EXT}=100kΩ; C_{EXT}=10uF; see Figure 5	V_{DD}=5V	1.01	1.09	1.11	s
			V_{DD}=10V	0.99	1.04	1.09	s
pulse width variation	Δt_W	nQ or $n\bar{Q}$ variation over temperature range; see Figure 6	V_{DD}=5V	-	±0.2	-	%
			V_{DD}=10V	-	±0.2	-	%
		nQ or $n\bar{Q}$ variation over V_{DD} voltage range 5V to 12V; see Figure 7		-	±1.5	-	%
		nQ or $n\bar{Q}$ variation between monostables in the same device; R_{EXT}=100kΩ; C_{EXT}=2nF to 10uF	V_{DD}=5V	-	±1	-	%
			V_{DD}=10V	-	±1	-	%

external timing resistor	R_{EXT}	-	5	-	-	kΩ
external timing capacitor	C_{EXT}	-	2000	-	no limits	pF
input capacitance	C_I	-	-	-	7.5	pF

Note:

[1] t_t is the same as t_{TLH} and t_{THL}.

[2] The maximum permissible resistance R_{EXT}, which holds the specified accuracy of t_W (nQ, $n\overline{Q}$ output), depends on the leakage current of the capacitor C_{EXT} and the leakage current of the 74HC4538D-JSM.

4、Testing Circuit

4.1、AC Testing Circuit

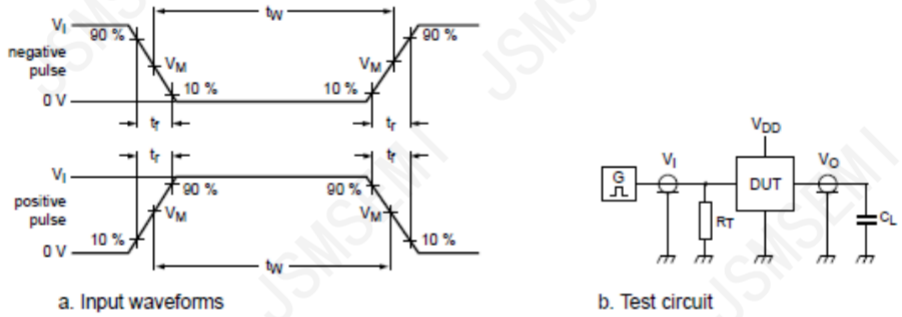


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

4.2、AC Testing Waveforms

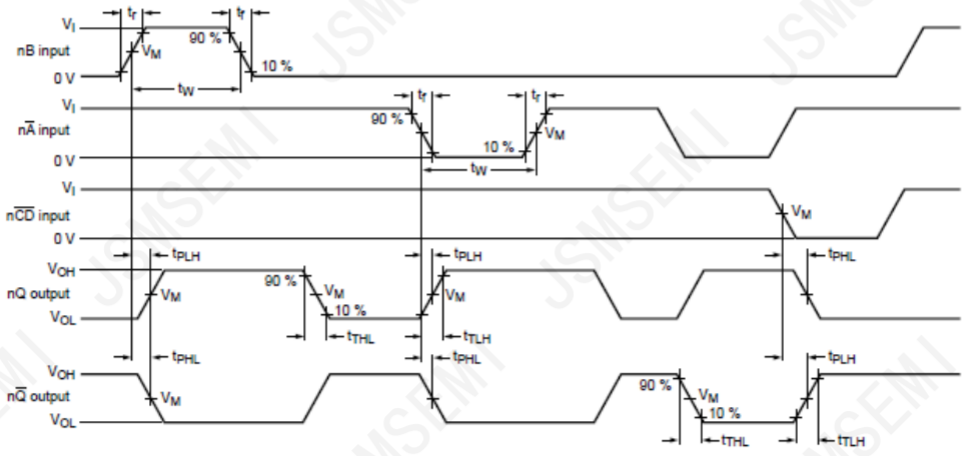


Figure 4. Waveforms showing propagation delays

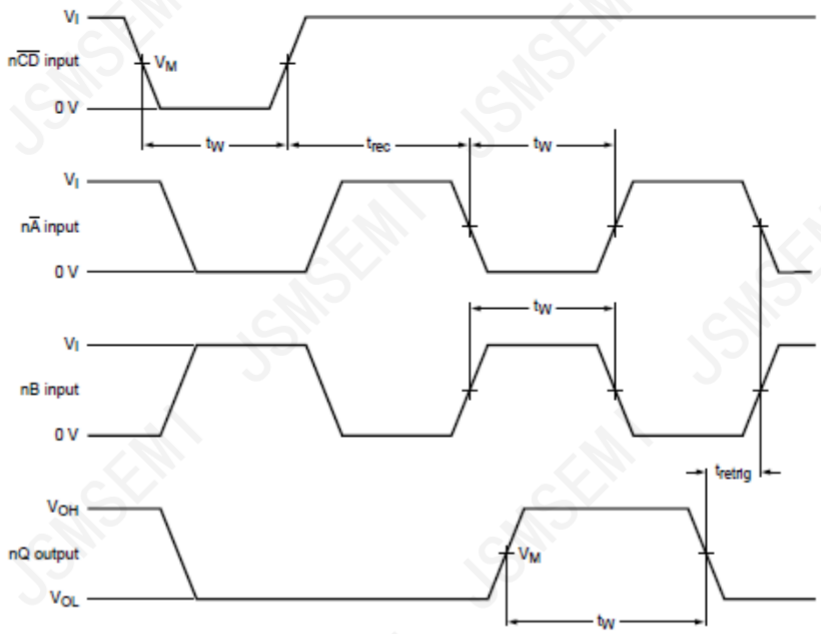
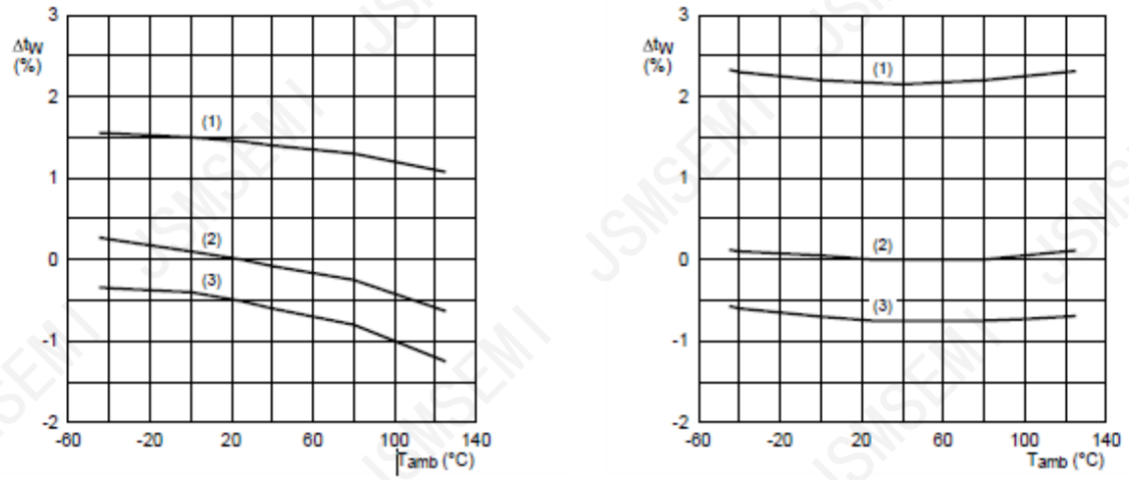


Figure 5. Waveforms showing minimum nCD, nA, nB, and nQ pulse widths, recovery and retrigger times



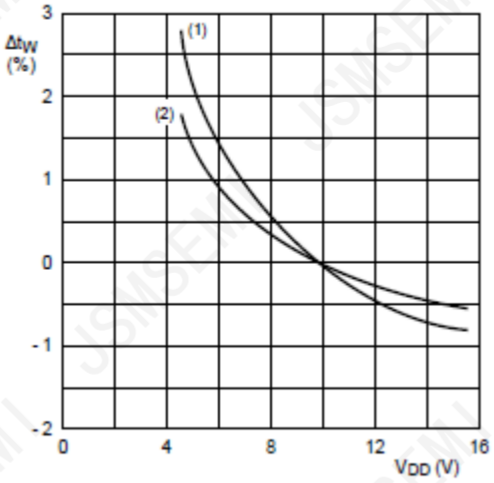
a. R_{EXT} = 100 kΩ; C_{EXT} = 100 nF

(1) V_{DD} = 5 V
(2) V_{DD} = 10 V
(3) V_{DD} = 15 V
Δt_W = 0 % at V_{DD} = 10 V and T_{amb} = 25 °C

b. R_{EXT} = 100 kΩ; C_{EXT} = 2 nF

(1) V_{DD} = 5 V
(2) V_{DD} = 10 V
(3) V_{DD} = 15 V
Δt_W = 0 % at V_{DD} = 10 V and T_{amb} = 25 °C

Figure 6. Typical normalized change in output pulse width as a function of ambient temperature



T_{amb} = 25 °C; Δt_W = 0 % at V_{DD} = 10 V; R_{EXT} = 100 kΩ
(1) C_{EXT} = 2 nF
(2) C_{EXT} = 100 nF

Figure 7. Typical normalized change in output pulse width as a function of the supply voltage

4.3、Measurement Points

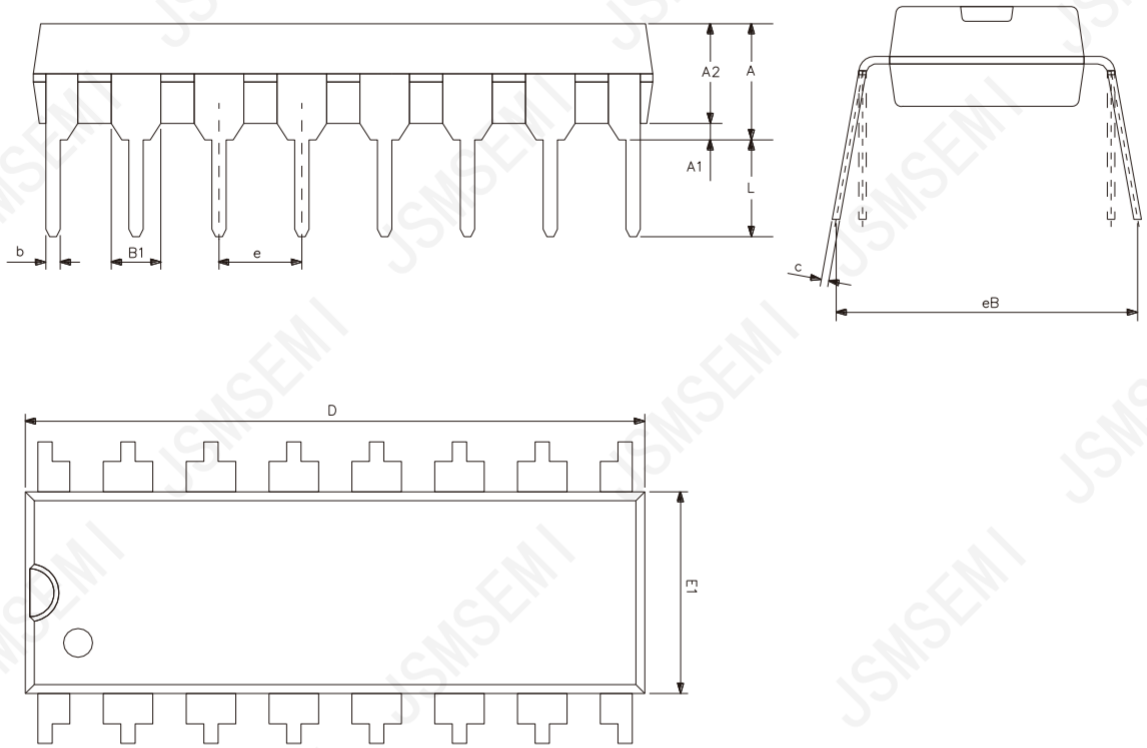
Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 12V	$0.5\times V_{DD}$	$0.5\times V_{DD}$

4.4、Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r , t_f	C_L
5V to 12V	V_{SS} or V_{DD}	≤ 20ns	50pF

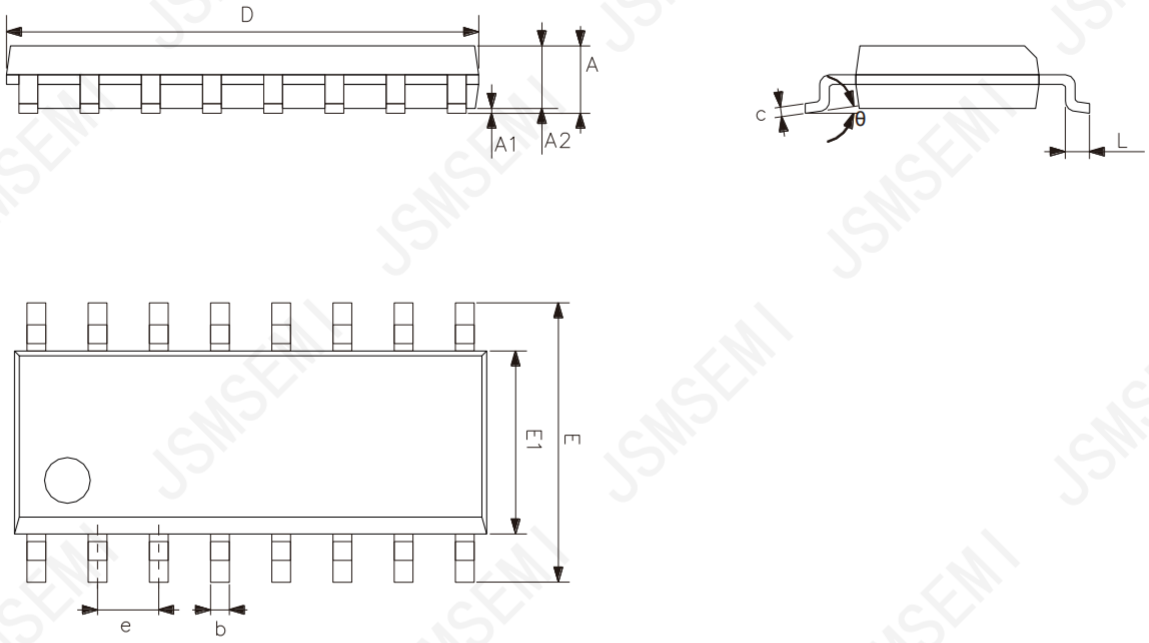
5、Package Information

5.1、DIP16



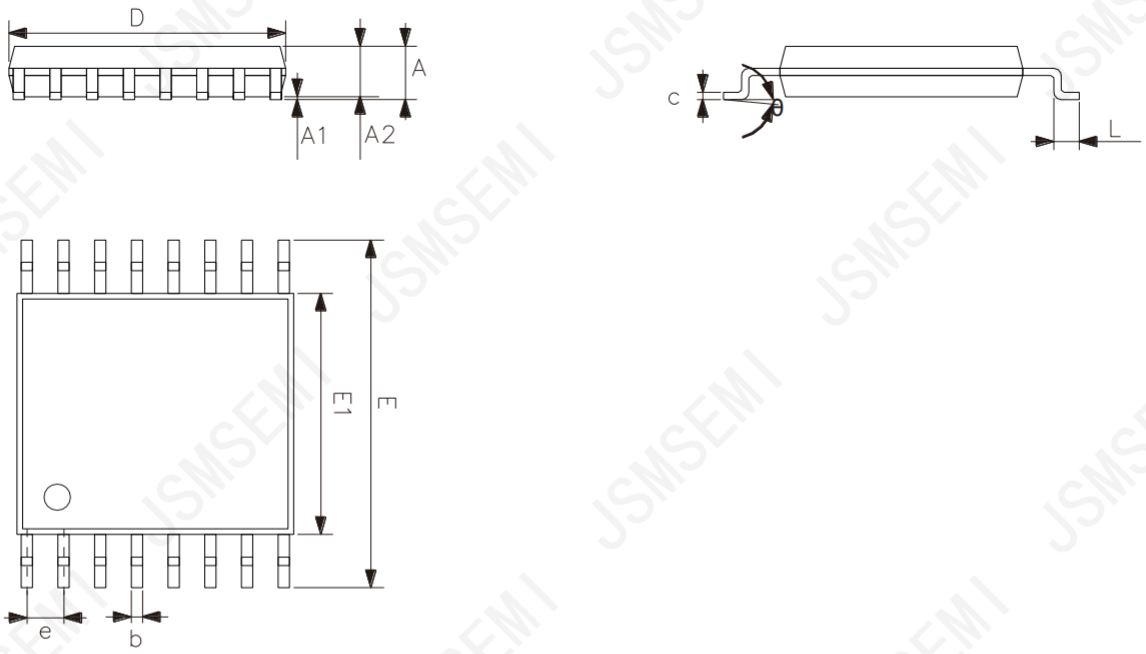
Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30

5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

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