5V DUAL RS-232 LINE DRIVER/RECEIVER

WITH±15-kV ESD PROTECTION

Features

- ESD Protection for RS-232 Bus Pins-±15kV -Human-Body Model
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standrds
- Operates at 5V VCC Supply
- Operates Up To 120 kbit/s
- External Capacitors ...4×0.1 μF
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Applications
  Battery-Powered Systems, PDAs Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment


DIP-16


SOP-16


TSSOP-16

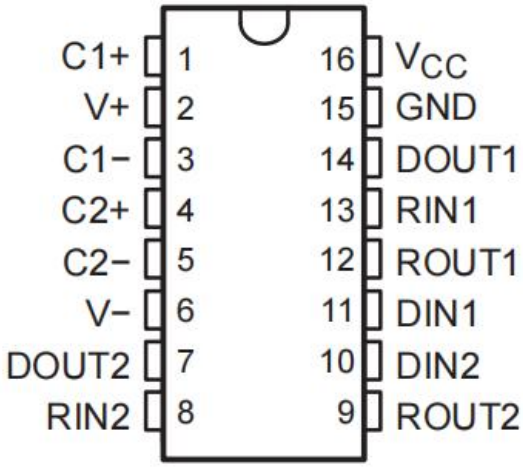
Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
SP202EIN	DIP-16	SP202	TUBE	1000pcs/Box
SP202EIM/TR	SOP-16	SP202	REEL	2500pcs/Reel
SP202EIMT/TR	TSSOP-16	SP202	REEL	2500pcs/Reel

General Description

The SP202 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The device operates at data signaling rates up to 120 kbit/s and a maximum of 30-V/μs driver output slew rate.

Pin symbols in package



Function Tables

EACH DRIVER

$INPUTD_{IN}$	$OUTPUTD_{OUT}$
L	H
H	L

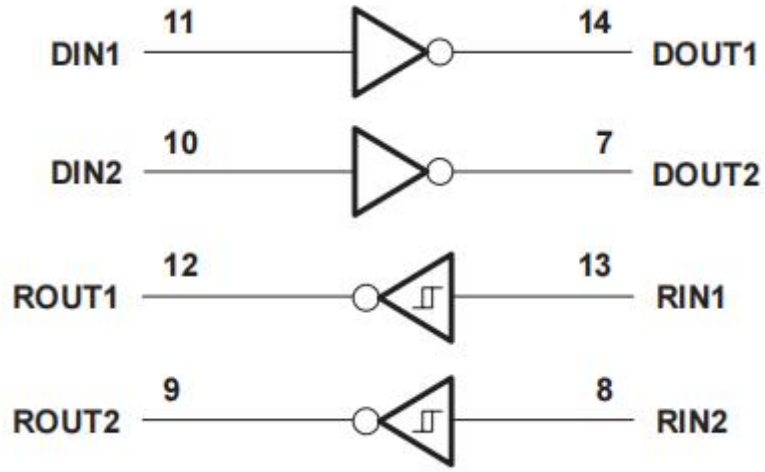
H=high level, L=low level

EACH RECEIVER

$INPUTR_{IN}$	$OUTPUTR_{OUT}$
L	H
H	L
Open	H

H = high level, L = low level, Open = input disconnected or connected driver off

logic diagram (positive logic)



absolute maximum ratings

over operating free-air temperature range (unless otherwise noted)

Condition		Min	Max	UNITS
Supply voltage range, V_{CC} (see Note 1)		-0.3	6	V
Positive charge pump voltage range, V+ (see Note 1)		V_{CC}-0.3	14	V
Negative charge pump voltage range, V− (see Note 1)		-14	0.3	V
Input voltage range, V_I	Drivers	-0.3	V_+ +0.3	V
	Receivers	-30	+30	V
Output voltage range, V_O	Drivers	V_- -0.3V	V_+ +0.3	V
	Receivers	-0.3	V_{CC} + 0.3	V
Short-circuit duration: D_{OUT}		Continuous		
Package thermal impedance, θJA (see Notes 2 and 3):	SOP package		73	°C/W
	DIP package		67	°C/W
	TSSOP package		1.8	°C/W
Operating virtual junction temperature, TJ			150	°C
Storage temperature range, Tstg		-65	150	°C
Lead Temperature (Soldering, 10 seconds)		-	260	°C

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

NOTES:

1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of TJ(max),θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) − TA)/θJA. Operating at the absolute maximum TJ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

PARAMETER			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
VIH	Driver high-level input voltage	D_{IN}	2			V
VIL	Driver low-level input voltage	D_{IN}			0.8	V
VI	Driver input voltage	D_{IN}	0		5.5	V
	Receiver input voltage		−30		30	
TA	Operating free-air temperature	SP202C	0		70	°C
		SP202I	−40		85	

NOTE 4: Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ±0.5 V.

electrical characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ICC	Supply current	No load,	VCC = 5 V		8	15	mA

All typical values are at V_{CC} = 5 V, and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1μF at V_{CC} = 5V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOH	High-level output voltage	D_{OUT} at RL = 3 kΩ to GND,D_{IN} = GND	5	9		V
VOL	Low-level output voltage	D_{OUT} at RL = 3 kΩ to GND,D_{IN} = V_{CC}	−5	−9		V
IIH	High-level input current	V_I = VCC		15	200	μA
IIL	Low-level input current	V_I at 0 V		−15	−200	μA
IOS‡	Short-circuit output current	V_{CC} = 5.5 V,V_O = 0 V		±10	±60	mA
ro	Output resistance	V_{CC}, V+, and V− = 0 V,V_O =±2 V	300			Ω

† All typical values are at VCC = 5 V, and TA = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1−C4 = 0.1μF at VCC = 5 V ± 0.5 V.

switching characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Maximum data rate	CL = 50 to1000pF, One D_{OUT} switching,	RL = 3 kΩ to 7 kΩ, See Figure 1	120			kbit/s
tPLH (D)	Propagation delay time, low- to high-level output	CL = 2500pF, All drivers loaded,	RL = 3 kΩ, See Figure 1		2		μs
tPHL (D)	Propagation delay time, High-to low-level output	CL = 2500pF, All drivers loaded,	RL = 3 kΩ, See Figure 1		2		μs
tsk(p)	Pulse skew§	CL=150pF to 2500pF,	RL = 3 KΩ to 7 kΩ, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	CL = 50pF to1000pF, V_{CC} = 5V	RL = 3 kΩ to 7 kΩ,	3	6	30	V/μs

All typical values are at VCC = 5 V, and TA = 25°C.

§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Test conditions are C1−C4 = 0.1μF at VCC = 5 V ± 0.5 V.

ESD protection

PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	Human-Body Model	±15	kV

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	I_{OH} = −1 mA	3.5V	V_{CC}−0.4 V		V
VOL	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
VIT+	Positive-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
VIT−	Negative-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
Vhys	Input hysteresis (VIT+ − VIT−)		0.2	0.5	1	V
ri	Input resistance	V_I =±3 V to ±25 V	3	5	7	kΩ

All typical values are at V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Test conditions are C1−C4 = 0.1μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

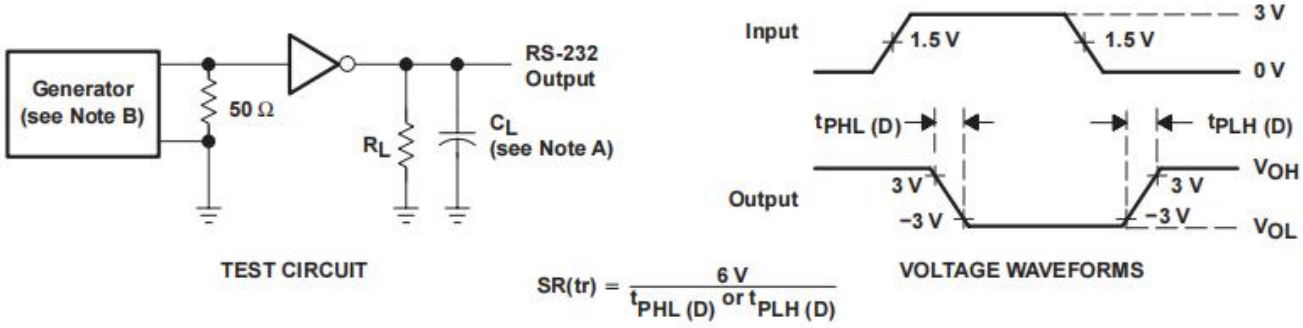
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
tPLH (R)	Propagation delay time, low- to high-level output	CL= 150 pF		0.5	10	μs
tPHL (R)	Propagation delay time, high- to low-level output	CL= 150 pF		0.5	10	μs
tsk(p)	Pulse skew‡			300		ns

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.

‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Test conditions are C1−C4 = 0.1μF, at V_{CC} = 5 V±0.5 V.

PARAMETER MEASUREMENT INFORMATION

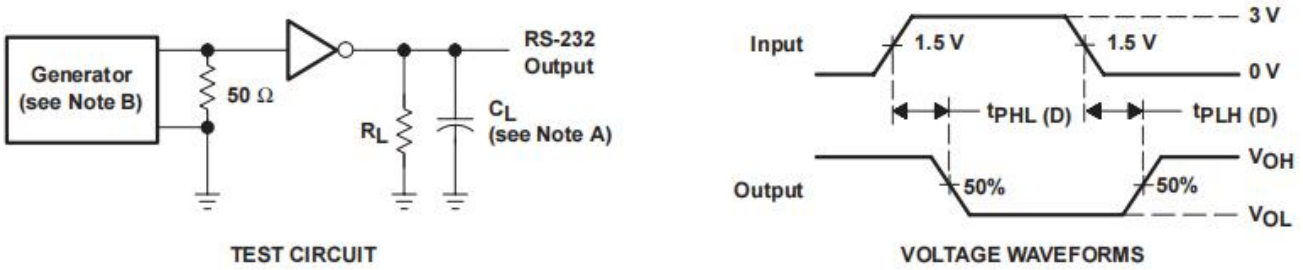


NOTES: A. CL includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 120 kbit/s, ZO = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 1. Driver Slew Rate

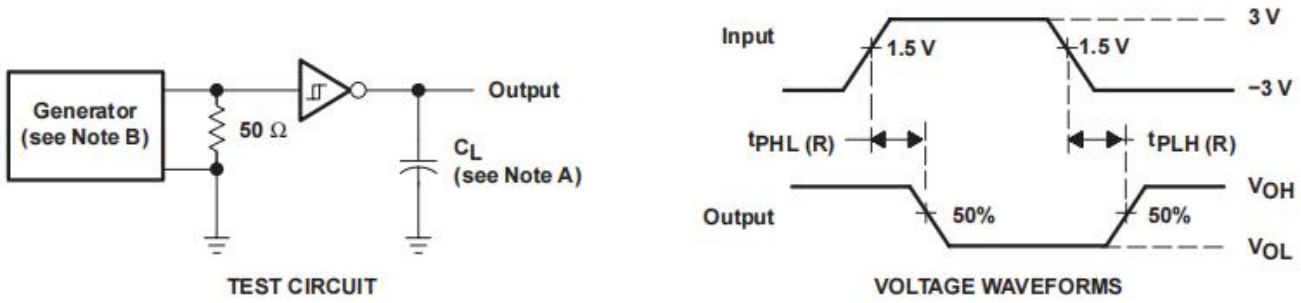
PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

C. The pulse generator has the following characteristics: PRR = 120 kbit/s, ZO = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 2. Driver Pulse Skew

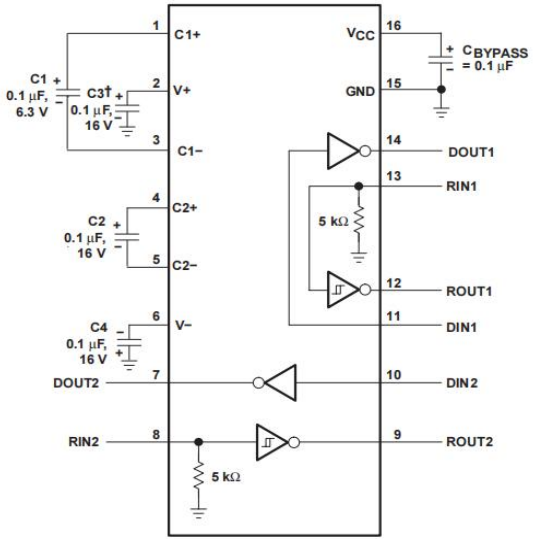


NOTES: A. CL includes probe and jig capacitance.

D. The pulse generator has the following characteristics: ZO = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

capacitor selection

The capacitor type used for C1−C4 is not critical for proper operation. The SP202 requires 0.1-μF capacitors, although capacitors up to 10μF can be used without harm. Ceramic dielectrics are suggested for the 0.1-μF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V−.

Use larger capacitors (up to 10 μF) to reduce the output impedance at V+ and V−.

Bypass V_{CC} to ground with at least 0.1 μF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1−C4).

ESD protection

SP202 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

ESD test conditions

Stringent ESD testing is performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5. Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

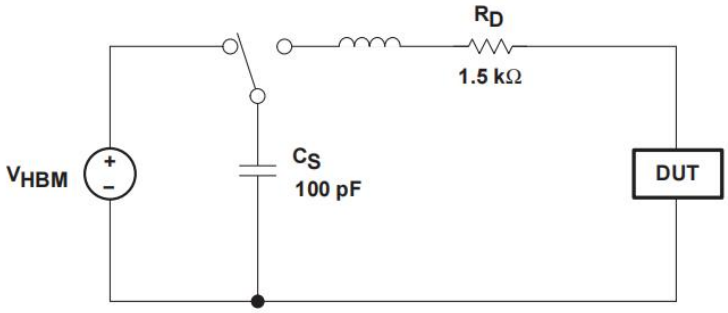


Figure 5. HBM ESD Test Circuit

APPLICATION INFORMATION

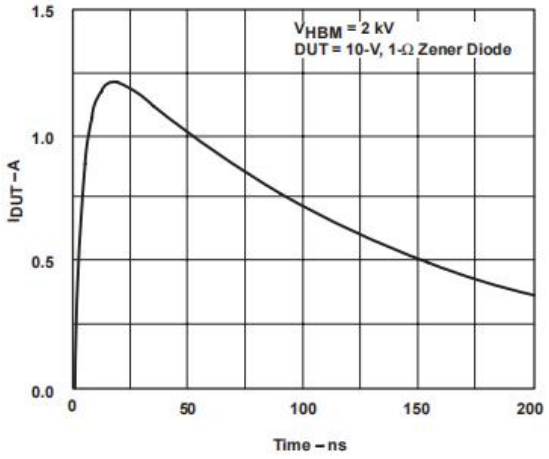


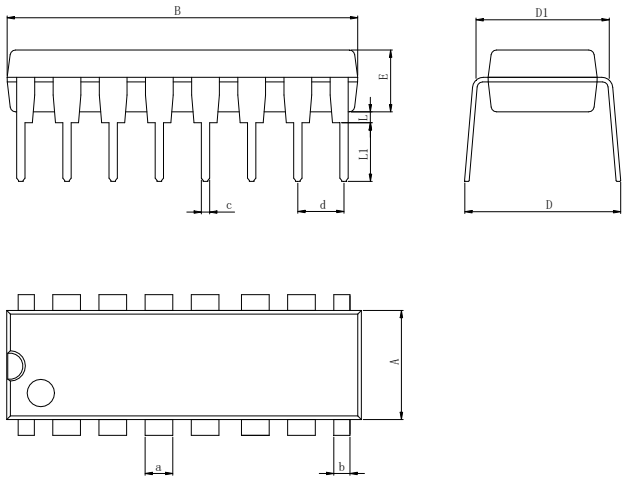
Figure 6. Typical HBM Current Waveform

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

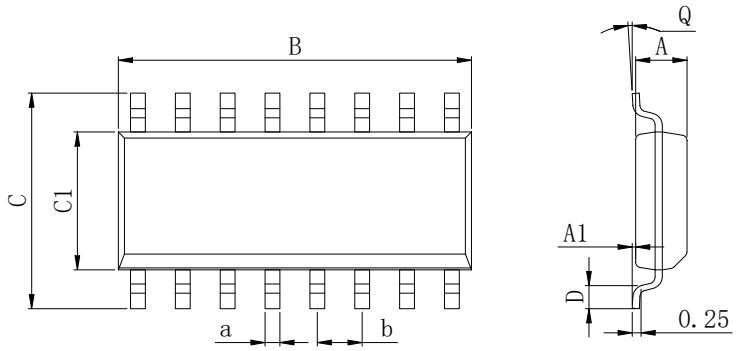
Physical Dimensions

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

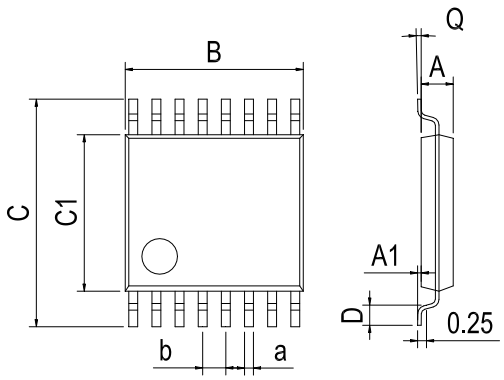
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2015-6-5	New	1-12
2023-9-15	Modify the package dimension diagram TSSOP-16、Updated DIP-16 dimension	9、10
2024-11-1	Update Lead Temperature、	3.

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety,security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.