

1. General Description

The 74LVC2GU04 is a dual unbuffered inverter. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

2. Features and Benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 3B exceeds 8000 V
 - MM JESD22-A115C Class C exceeds 550 V
 - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

74LVC2GU04

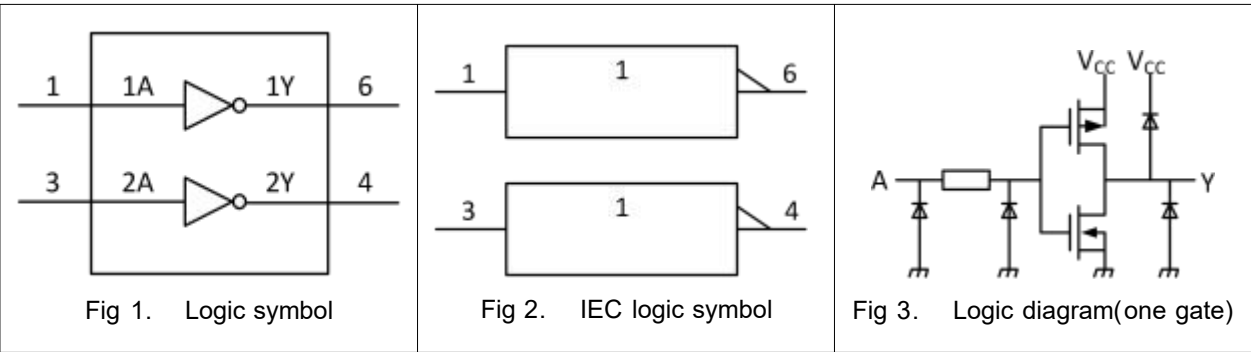
Dual unbuffered inverter

3. Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74LVC2GU04GV	SOT23-6L	SOT23 package, 6 pins 2.92 mm × 1.6 mm; 1.25 mm (Max) height	3000
74LVC2GU04GW	SOT363	SOT363 package, 6 pins 2.1 mm × 1.25 mm; 1.1 mm (Max) height	3000
74LVC2GU04GS	DFN1x1-6L	DFN1×1 package, 6 pins 1 mm × 1 mm; 0.42 mm (Max) height	5000
74LVC2GU04GM	DFN1x1.45-6L	DFN1.45×1 package, 6 pins 1.45 mm × 1 mm; 0.6 mm (Max) height	5000

4. Function Diagram



5. Pinning Information

5.1. Pin map

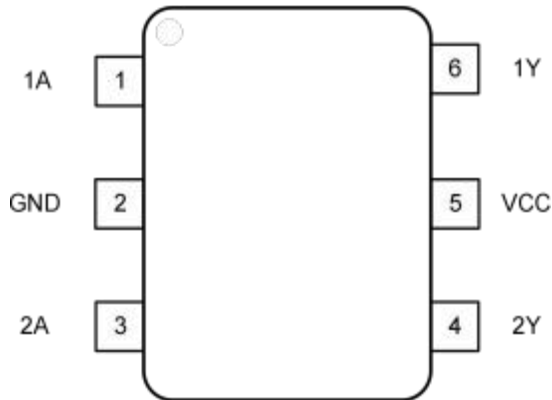


Fig 4. Top view pin configuration SOT23-6 and SOT363

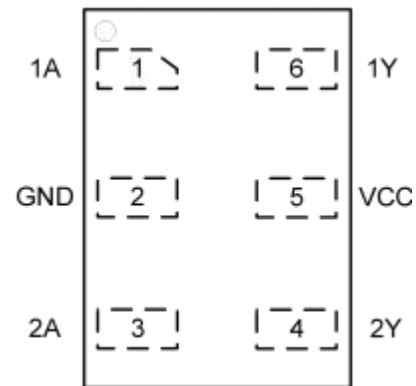


Fig 5. Top view pin configuration DFN6L

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	Data input
GND	2	Ground (0V)
2A	3	Data input
2Y	4	Data output
VCC	5	Supply voltage
1Y	6	Data output

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	H
H	L

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		± 50	mA
V_O	output voltage	Active mode [1]	-0.5	$V_{CC} + 0.5$	V
I_O	output current	$V_O = 0$ V to V_{CC}		± 50	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to + 125 °C		250	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65		5.5	V
V_I	input voltage		0		5.5	V
V_O	output voltage	Active mode	0		V_{CC}	V
T_{amb}	ambient temperature		-40		125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$			20	ns/V
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$			10	ns/V

9. Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.75V_{CC}$			$0.8V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	$0.75V_{CC}$			$0.8V_{CC}$		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	$0.75V_{CC}$			$0.8V_{CC}$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.8V_{CC}$			$0.8V_{CC}$		V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$			$0.25V_{CC}$		$0.2V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			$0.25V_{CC}$		$0.2V_{CC}$	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			$0.24V_{CC}$		$0.2V_{CC}$	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			$0.16V_{CC}$		$0.15V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$						
		$I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC} - 0.1$			$V_{CC} - 0.1$		V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2			0.95		V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9			1.7		V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2			1.9		V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3			2.0		V
		$I_O = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8			3.4		V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$						
		$I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$			0.10		0.10	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$			0.45		0.70	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$			0.30		0.45	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$			0.40		0.60	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$			0.55		0.80	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$			0.55		0.80	V
I_I	Input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$		± 0.1	± 1		± 1	μA

74LVC2GU04

Dual unbuffered inverter

I _{CC}	supply current	V _I = 5.5V or GND ; I _O = 0A ; V _{CC} = 1.65V to 5.5V		0.1	4		4	μA
C _I	input capacitance	V _{CC} = 3.3V ; V _I = GND to V _{CC}		5.3				pF

[1]All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 6 [2]						
		V _{CC} = 1.65 V to 1.95 V	0.8	1.6	3.3	0.8	3.4	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	1.4	2.6	0.7	2.7	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	1.3	2.2	0.8	2.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.7	1.3	2.0	0.7	2.1	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3V [3]		12.1				pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

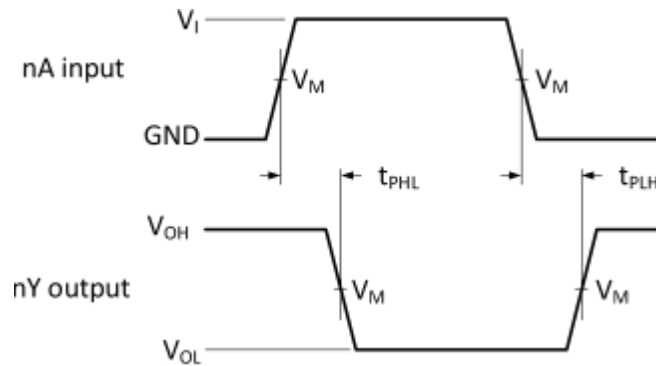
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

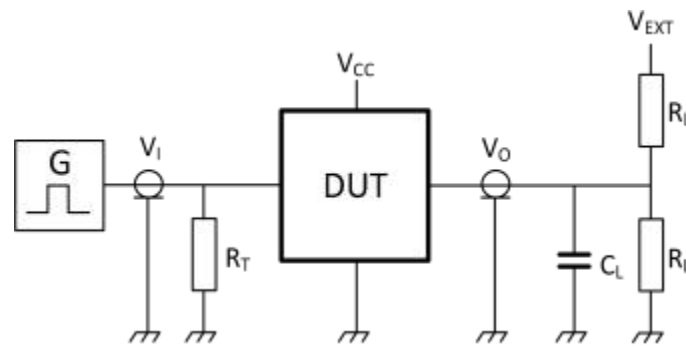
Fig 6. The input nA to output nY propagation delays

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$

74LVC2GU04

Dual unbuffered inverter



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

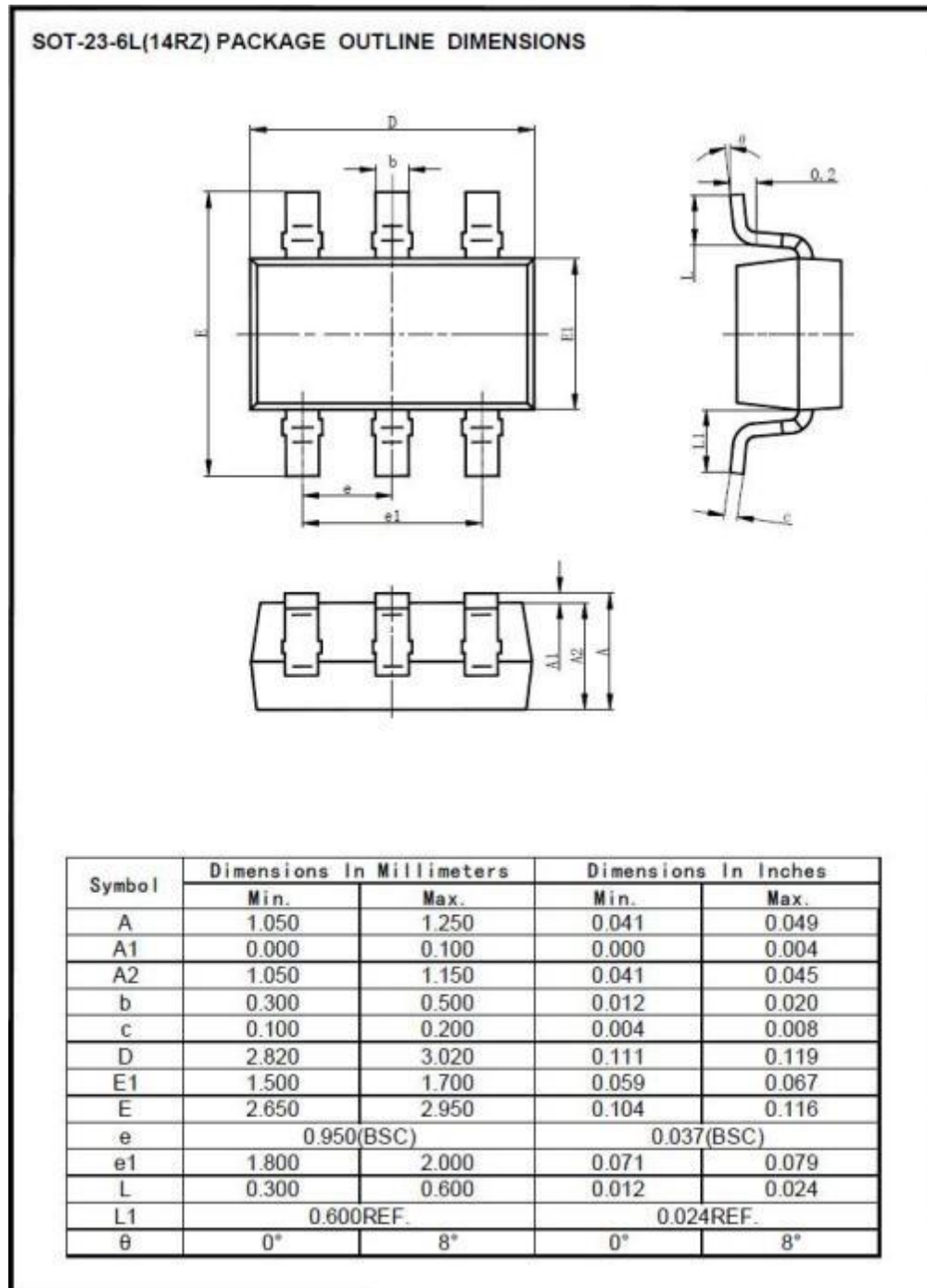
Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
3.0 V to 3.6 V	3 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

11. Package Outline

SOT23-6L

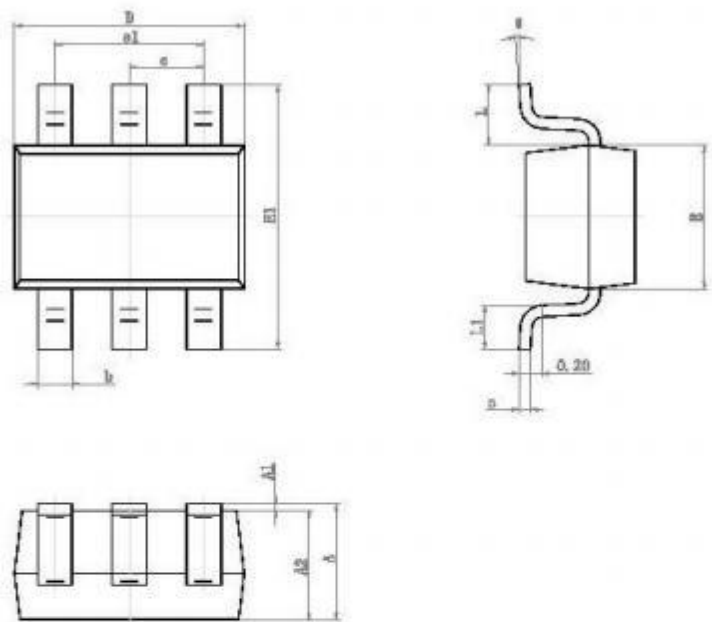


74LVC2GU04

Dual unbuffered inverter

SOT363

SOT-363 (16R) PACKAGE OUTLINE DIMENSIONS

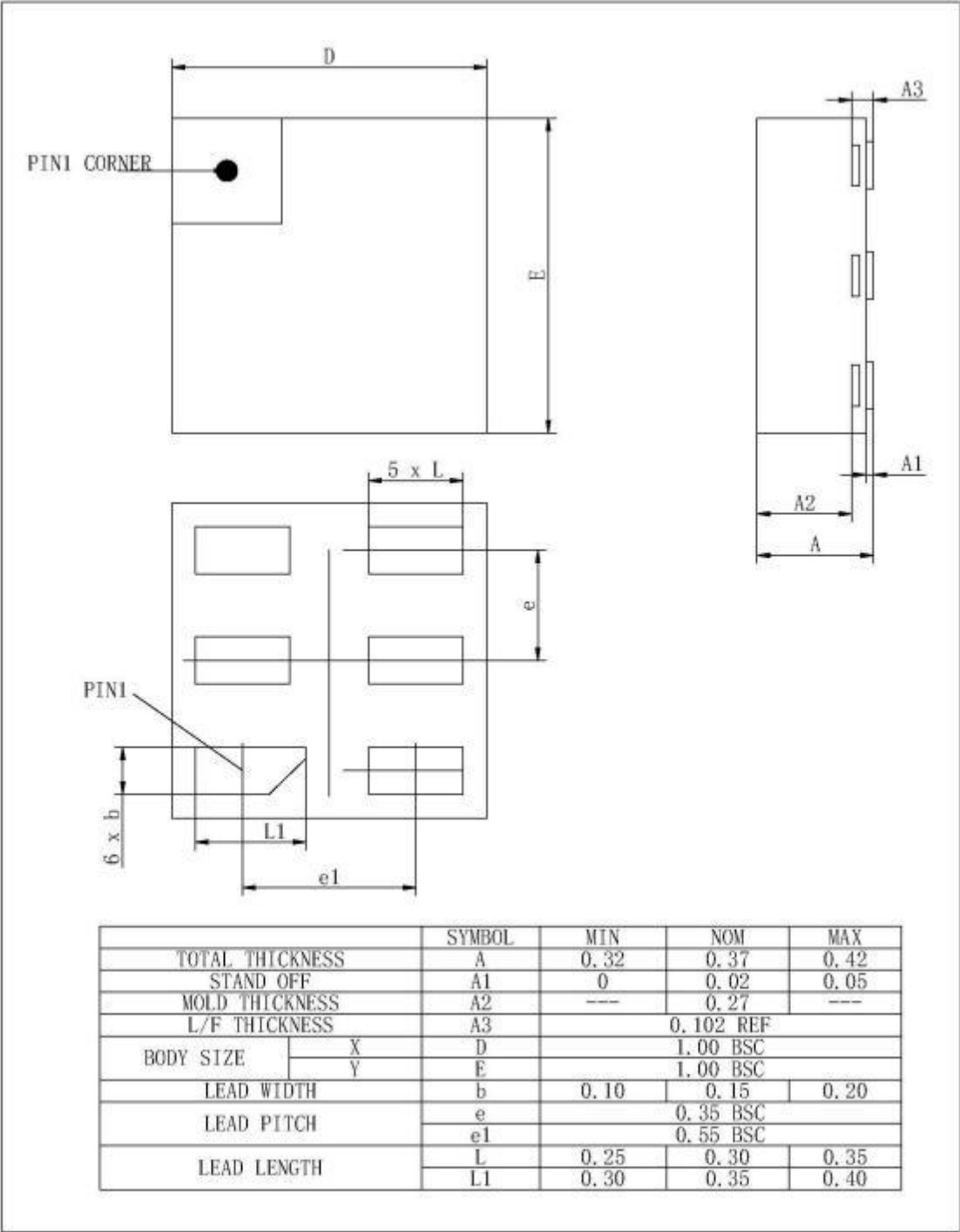


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.525 REF.		0.021 REF.	
L1	0.260	0.480	0.010	0.018
θ	0°	8°	0°	8°

74LVC2GU04

Dual unbuffered inverter

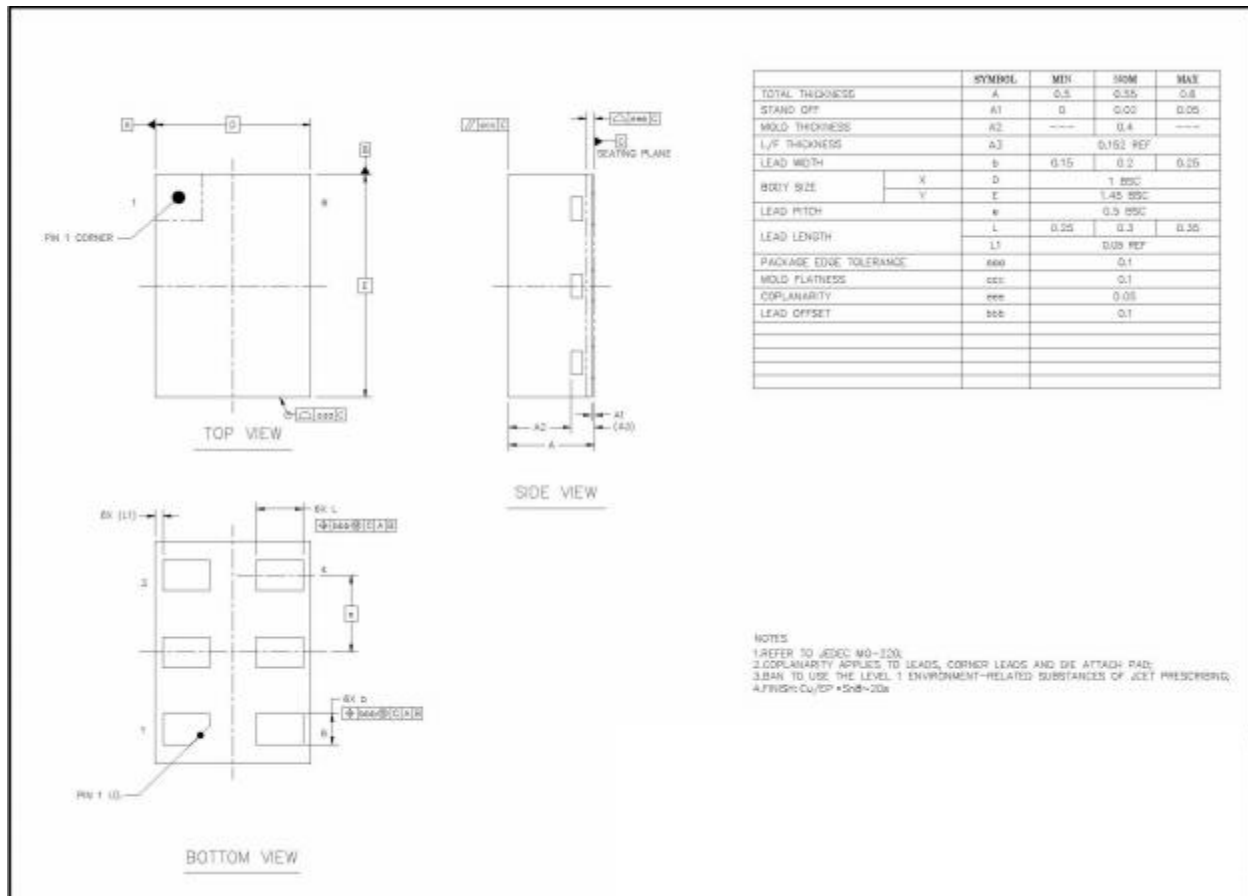
DFN1x1-6L



74LVC2GU04

Dual unbuffered inverter

DFN1x1.45-6L



12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74LVC2GU04 Rev. 1.0	Aug 08, 2024	Product datasheet		